B9949

3.3V 160-MHz 1:15 Clock Distribution Buffer

Features

- **160MHz Clock Support**
- **LVPECL or LVCMOS/LVTTL Clock Input**
- **LVCMOS/LVTTL Compatible Inputs**
- **15 Clock Outputs: Drive up to 30 Clock Lines**
- **1X and 1/2X Configurable Outputs**
- **Output Three-state Control**
- **350 ps Maximum Output-to-Output Skew**
- **Pin Compatible with MPC949**
- **Industrial Temp. Range: –40°C to +85°C**
- **52-Pin TQFP Package**

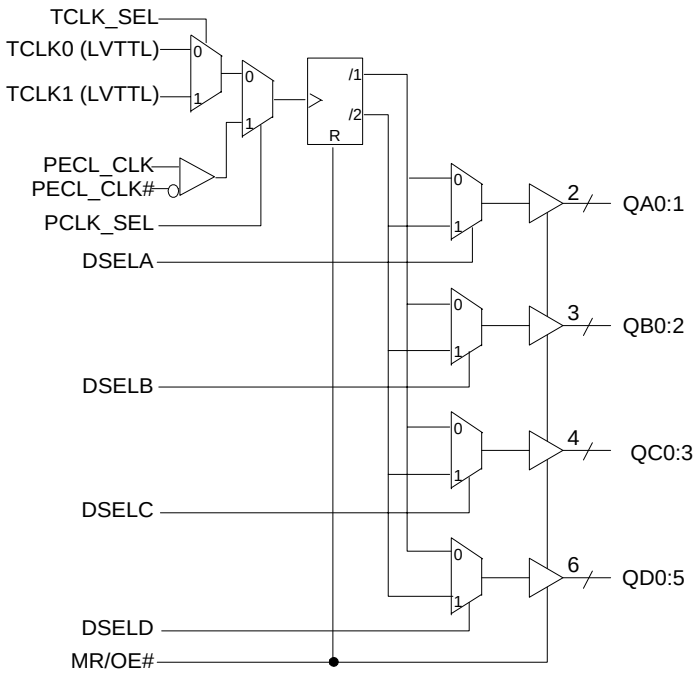
Description

The B9949 is a low-voltage clock distribution buffer with the capability to select either a differential LVPECL or LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 15 outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9949 has an effective fan-out of 1:30.

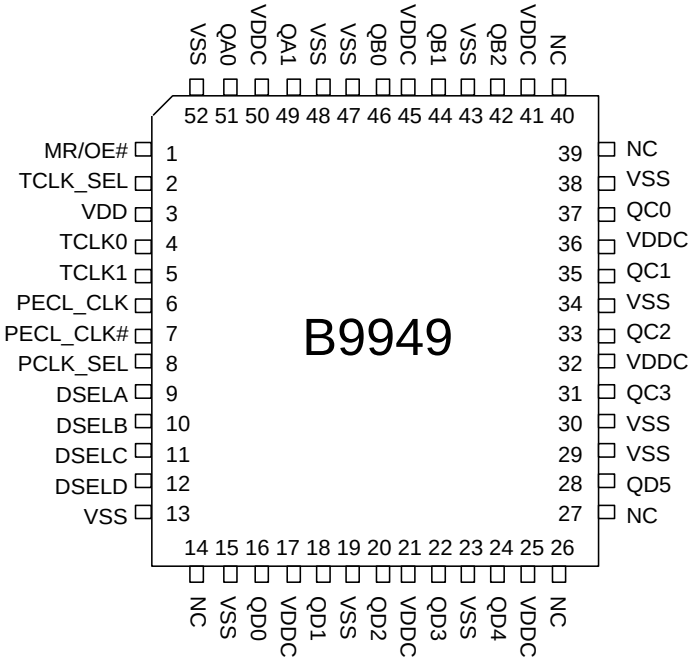
The B9949 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:D) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The B9949 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

Block Diagram



Pin Configuration



Pin Description [1]

Pin	Name	PWR	I/O	Description
6	PECL_CLK		I, PD	PECL Input Clock.
7	PECL_CLK#		I, PU	PECL Input Clock.
4, 5	TCLK(0,1)		I, PU	External Reference/Test Clock Input.
49, 51	QA(1,0)	VDDC	O	Clock Outputs.
42, 44, 46	QB(2:0)	VDDC	O	Clock Outputs.
31, 33, 35, 37	QC(3:0)	VDDC	O	Clock Outputs.
16, 18, 20, 22, 24, 28	QD(5:0)	VDDC	O	Clock Outputs.
9, 10, 11, 12	DSEL(A:D)		I, PD	Divider Select Inputs. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
2	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
8	PCLK_SEL		I, PD	PECL Select Input. When HIGH, PECL clock is selected and when LOW TCLK(0,1) is selected
1	MR_OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated.
17, 21, 25, 32, 36, 41, 45, 50	VDDC			3.3V Power Supply for Output Clock Buffers.
3	VDD			3.3V Power Supply
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	VSS			Common Ground
14, 26, 27, 39, 40,	NC			Not Connected

Note:
1. PD = Internal Pull-Down, PU = Internal Pull-Up.

Maximum Ratings[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... –40°C to +85°C

Maximum ESD protection 2KV

Maximum Power Supply: 5.5V

Maximum Input Current: ..... ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } Vout) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: V_{DDC} = 3.3V ±5%, V_{DD} = 3.3V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	PECL_CLK, Single Ended	1.49		1.825	V
		All other inputs	V_{SS}		0.8	
V_{IH}	Input High Voltage	PECL_CLK, Single Ended	2.135		2.42	V
		All other inputs	2.0		V_{DD}	
I_{IL}	Input Low Current (@V_{IL} = V_{SS})	Note 3			–100	µA
I_{IH}	Input High Current (@V_{IL} = V_{DD})				100	µA
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	Note 4	300		1000	mV
V_{CMR}	Common Mode Range PECL_CLK		V_{DD} – 2.0		V_{DD} – 0.6	V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA, Note 5			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –20 mA, V_{DDC} = 3.3V, Note 5	2.5			V
I_{DD}	Quiescent Supply Current	All V_{DDC} and V_{DD}		1	2	mA
C_{in}	Input Capacitance				4	pF

Notes:

2. The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the V_{CMR} range and the input lies within the V_{PP} specification.
5. Driving series or parallel terminated 50Ω (or 50Ω to V_{DD}/2) transmission lines.

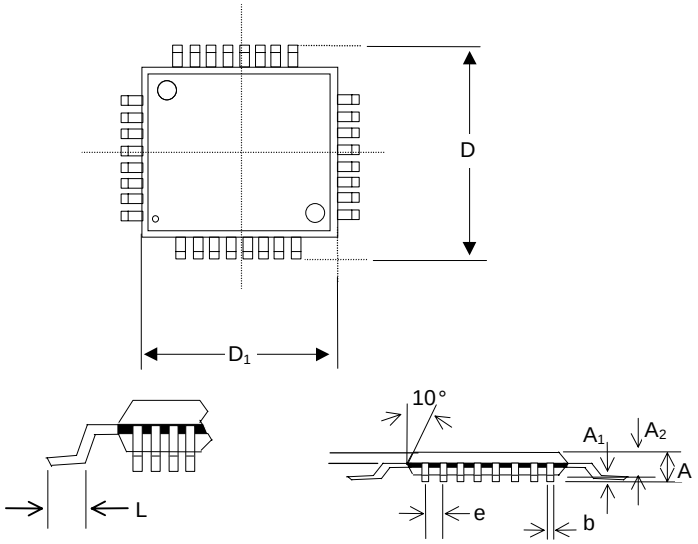
AC Parameters[6]: V_{DDC} = 3.3V ±5%, V_{DD} = 3.3V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Maximum Input Frequency[7]		160			MHz
Tpd	PECL_CLK to Q Delay[7]		4.0	-	8.6	ns
	TCLK to Q Delay[7]		4.2	-	10.5	
FoutDC	Output Duty Cycle[7, 8]	Measured at V_{DDC}/2	TCYCLE/2 – 1		TCYCLE/2 + 1	ns
tpZL, tpZH	Output Enable Time (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[7, 9]	Fin<130MHz			350	ps
Tskew (pp)	Part-to-Part Skew [10]	PECL_CLK to Q		1.5	2.75	ns
		TCLK to Q		2.0	4.0	
Tr/Tf	Output Clocks Rise/Fall Time[9]	0.8V to 2.0V	0.10		1.0	ns

Notes:

6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. Outputs loaded with 30 pF each
10. Part-to-Part Skew at a given temperature and voltage

Package Drawing and Dimensions (52 TQFP)



52-Pin TQFP Outline Dimensions

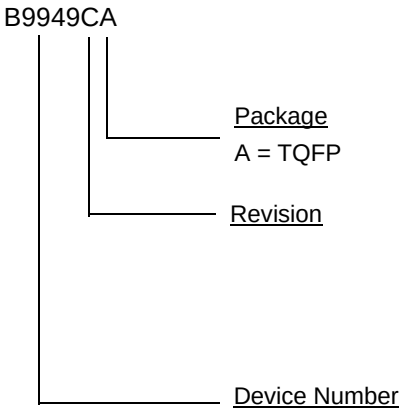
Symbol	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.472	-	-	12.00	-
D_1	-	0.394	-	-	10.00	-
b	0.009	-	0.015	0.22	-	0.38
e	0.026 BSC			0.65 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
B9949CA[11]	52 PIN TQFP	Industrial, –40°C to +85°C

Note:
11. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
B9949CA,
Date Code, Lot #



Document Tital: B9949 3.3V, 160-MHz, 1:15 Clock Distribution Buffer Document Number: 38-07081				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107117	06/06/01	IKA	Convert from IMI to Cypress
*A	108062	07/03/01	NDP	Changed Commercial to Industrial
*B	109807	02/01/02	DSG	Convert from Word Doc to Adobe Framemaker
*C	122766	12/14/02	RBI	Add power up requirements to maximum ratings information