QUAD 2-INPUT MULTIPLEXER; 3-STATE

FEATURES

- **Non-inverting data path**
- **3-state outputs interface directly with system bus**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT257 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE}.(1I_1.S + 1I_0.\overline{S})$
$2Y = \overline{OE}.(2I_1.S + 2I_0.\overline{S})$
$3Y = \overline{OE}.(3I_1.S + 3I_0.\overline{S})$
$4Y = \overline{OE}.(4I_1.S + 4I_0.\overline{S})$

The "257" is identical to the "258" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	$C_L = 15$ pF $V_{CC} = 5$ V	11 14	13 17	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	45	45	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

| PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 13, 10	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 12, 9	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage
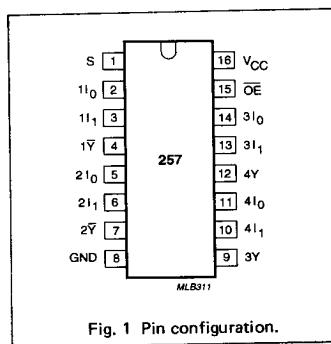
Fig. 1 Pin configuration.
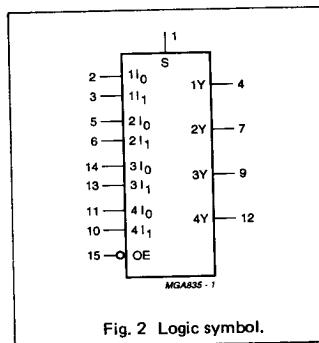
Fig. 2 Logic symbol.
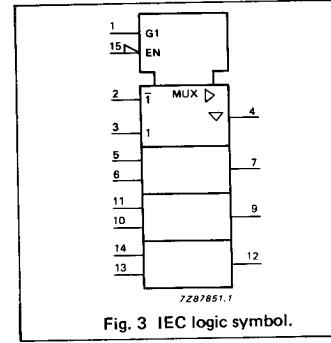
Fig. 3 IEC logic symbol.
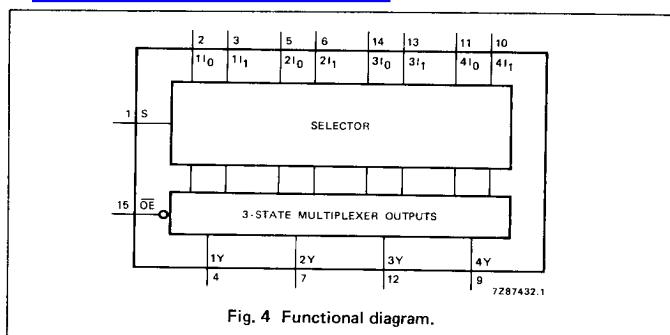
"74HC257D-T"

Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	'H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
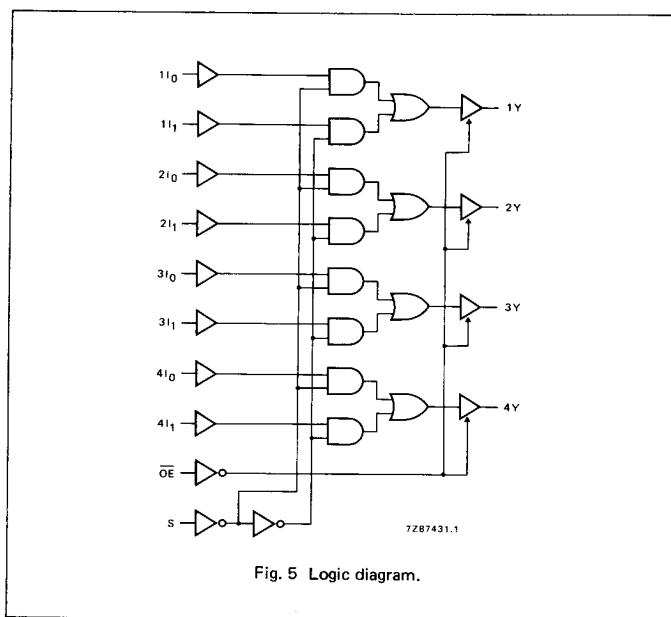
Fig. 5 Logic diagram.

"74HC257D-T"

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	V_{CC} V	WAVEFORMS
$t_{PHL}/$ t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY	36 13 10	110 22 19			140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ t_{PLH}	propagation delay S to nY	47 17 14	150 30 26			190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
$t_{PZH}/$ t_{PZL}	3-state output enable time $\overline{OE}$ to nY	33 12 10	150 30 26			190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
$t_{PHZ}/$ t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	41 15 12	150 30 26			190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ t_{TLH}	output transition time	14 5 4	60 12 10			75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

"74HC257D-T"

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nl_0	0.40
nl_1	0.40
$\overline{OE}$	1.35
S	0.70

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT							UNIT	V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay nl_0 to nY; nl_1 to nY		16	30		38		45	ns	4.5	Fig. 6
$t_{PHL}/$ t_{PLH}	propagation delay S to nY		20	35		44		53	ns	4.5	Fig. 6
$t_{PZH}/$ t_{PZL}	3-state output enable time $\overline{OE}$ to nY		15	30		38		45	ns	4.5	Fig. 7
$t_{PHZ}/$ t_{PLZ}	3-state output disable time $\overline{OE}$ to nY		16	30		38		45	ns	4.5	Fig. 7
$t_{THL}/$ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

"74HC257D-T"
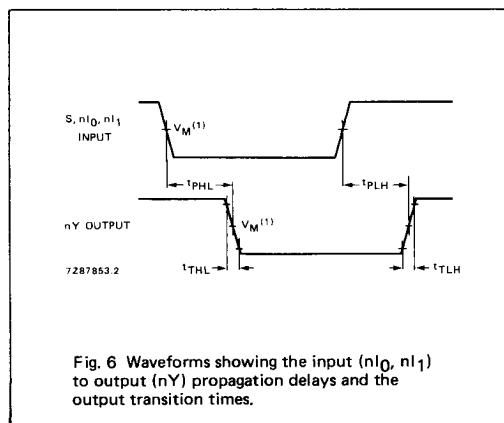
AC WAVEFORMS

Fig. 6 Waveforms showing the input (nI_0, nI_1) to output (nY) propagation delays and the output transition times.
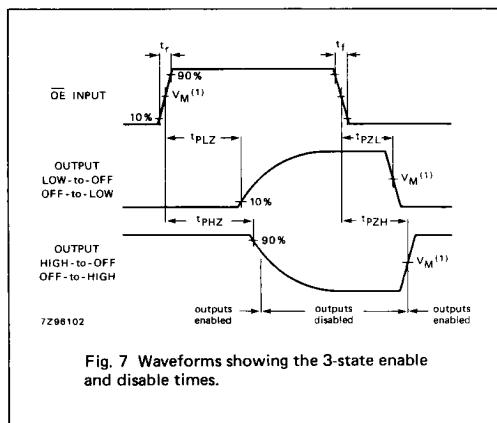
Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = $ GND to V_{CC}.
    HCT: $V_M = 1.3$ V; $V_I = $ GND to 3 V.