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Signetics

查询"54F30245/B3A"供应商

54F30245 Transceiver

Octal Transmission Line/Backplane
Transceiver, NINV (30 Ω O.C. w/ Enable + 3-State)

Military Logic Products

Product Specification

DESCRIPTION

The 54F30245 is a high current Octal Transceiver and has non-inverting paths.

The B outputs are open collector with 130mA I_{OL} while the A outputs are 3-State with 20mA I_{OL}. The transceiver is designed to deal with the low impedance transmission line effects found on printed circuit boards when fast edge rates are used.

The 130mA I_{OL} provides ample power to achieve TTL switching on the incident wave.

FEATURES

- High-impedance NPN base inputs for reduced loading
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- Choice of outputs
Open collector (B₀ - B₇) and 3-States (A₀ - A₇)
- Open collector outputs sink 130mA
- 130mA I_{OL} Ideal for low impedance applications and transmission line effects with impedance as low as 30Ω
- 3-State outputs sink 20mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (Improves speed and noise immunity)
- Flow through pinout structure facilitates PC board layout

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

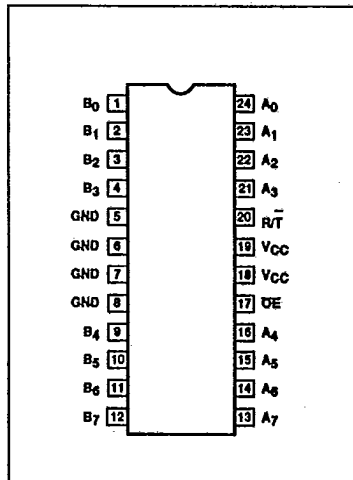
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A ₀ - A ₇	Data Inputs	3.5/0.12	70μA/70μA
B ₀ - B ₇	Data Inputs	3.5/1.0	70μA/0.6mA
OE	Output Enable Inputs (Active Low)	1.0/0.033	20μA/20μA
R/T	Receive/Transmit Input	1.0/0.033	20μA/20μA
A ₀ - A ₇	Data Outputs (3-State)	150/33.3	3mA/20mA
B ₀ - B ₇	Data Outputs (OC*)	OC*/216.6	OC*/130mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC* = Open Collector

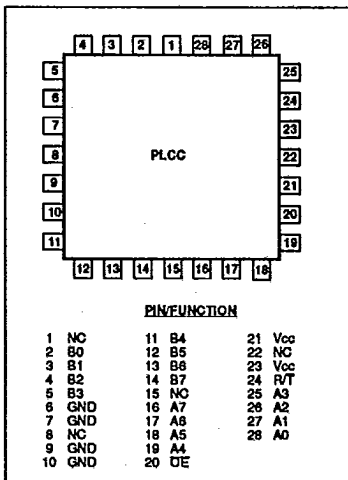
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dip	54F30245/BLA
24-Pin Ceramic Flat Pack	54F30245/BKA
28-Pin Ceramic LLCC	54F30245/B3A

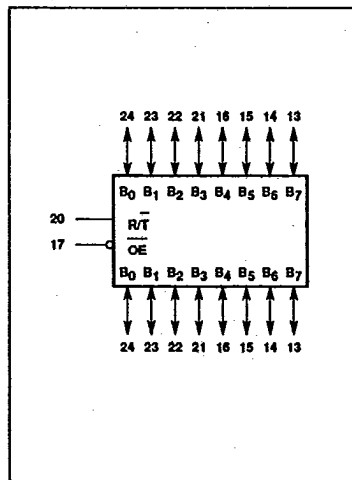
PIN CONFIGURATION



LLCC PIN CONFIGURATION



LOGIC SYMBOL

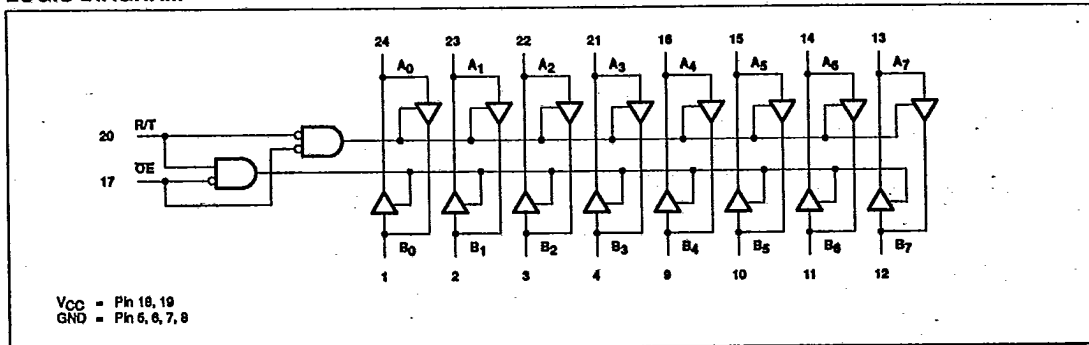


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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			
OE	R/T	A _n	B _n
L	H	A = B	Inputs
L	L	Inputs	B = A
H	X	Z	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I _O	Current applied to output in Low output state	B ₀ - B ₇	260
		A ₀ - A ₇	40
T _{STG}	Storage temperature range	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	High-level output voltage			4.5	V
I _{OH1}	High-level output current			-1	mA
I _{OH2}	High-level output current			-3	mA
I _{OL}	Low-level output current			130	mA
				20	mA
T _A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT
				Min	Typ ²	Max	
I _{OH}	High-level output current	B ₀ - B ₇	V _{CC} = Min, V _{IL} = Max, V _{IH} = Min, V _{OH} = Max			250	μA
V _{OH}	High-level output voltage	A ₀ - A ₇ R/T, OE	V _{CC} = Min, V _{IL} = Max, V _{IH} = Min	I _{OH2} = -3mA	2.4		V
				I _{OH1} = -1mA	2.5	3.4	V
V _{OL}	Low-level output voltage	A ₀ - A ₇ R/T, OE	V _{CC} = Min, V _{IL} = Max, V _{IH} = Min	I _{OL} = 20mA	.35	.50	V
				I _{OL} = 100mA	.40	.50	V
V _{OL}	Low-level output voltage	B ₀ - B ₇	V _{CC} = Min, V _{IL} = Max, V _{IH} = Min	I _{OL1} = 130mA ⁴		.80	V
V _{IK}	Input clamp voltage		V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	R/T, OE	V _{CC} = 0.0V, V _I = 7.0V			100	μA
		A _n , B _n	V _{CC} = Max, V _I = 5.5V			1.0	mA
I _{IH1}	High-level input current	R/T, OE	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IH3}	High-level input current	B ₀ - B ₇	V _{CC} = Max, V _I = 2.7V			70	μA
I _{IL}	Low-level input current	R/T, OE	V _{CC} = Max, V _I = 0.5V			-20	μA
		B ₀ - B ₇				-600	μA
I _{OZH} + I _{IH}	Off-state output current, High-level voltage applied	A ₀ - A ₇	V _{CC} = Max, V _O = 2.7V			70	μA
I _{OZL} + I _{IL}	Off-state output current, Low-level voltage applied	A ₀ - A ₇	V _{CC} = Max, V _O = 0.5V			-70	μA
I _{OS}	Short circuit output current ³	A ₀ - A ₇	V _{CC} = Max	-60		-150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = Max		45	70	mA
		I _{CCL}			85	135	mA
		I _{CCZ}			55	75	mA

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable conditions and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.
4. I_{OL1} is the current necessary to guarantee the High-to-Low transition in a 30Ω transmission line on the incident wave.

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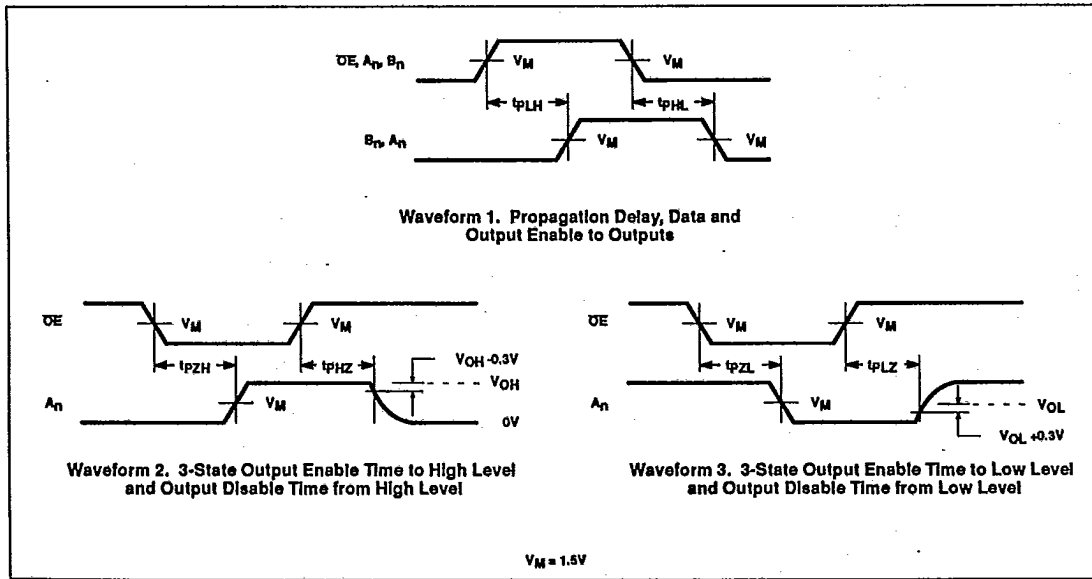
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AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			Min	Typ	Max	Min	Max	
*t _{PLH} t _{PHL}	Propagation delay A _n to B _n	Waveform 1	7.5 3.0	9.5 5.5	13.5 6.5	7.0 3.0	13.5 9.5	ns
t _{PLH} t _{PHL}	Propagation delay B _n to A _n	Waveform 1	2.0 1.0	3.5 2.5	6.5 5.5	1.5 1.0	7.0 5.5	ns
t _{PLH} t _{PHL}	Propagation delay OE to B _n	B _n outputs Waveform 1	7.0 3.5	9.5 5.5	12.5 8.5	7.0 3.5	13.0 9.5	ns
t _{PZH} t _{PZL}	Output Enable time from High-to-Low	A _n outputs Waveform 2	2.5	4.5	7.5	2.0	8.5	ns
t _{PZH} t _{PZL}	Output Enable time from High-to-Low	A _n outputs Waveform 3	2.0	4.0	8.0	1.5	8.5	
t _{PHZ} t _{PLZ}	Output Enable time from High-to-Low	A _n outputs Waveform 2	1.5	3.5	6.5	1.0	7.5	ns
t _{PHZ} t _{PLZ}	Output Enable time from High-to-Low	A _n outputs Waveform 3	1.0	3.5	6.5	1.0	7.0	

* See Figure A for Open Collector Output Information

AC WAVEFORMS



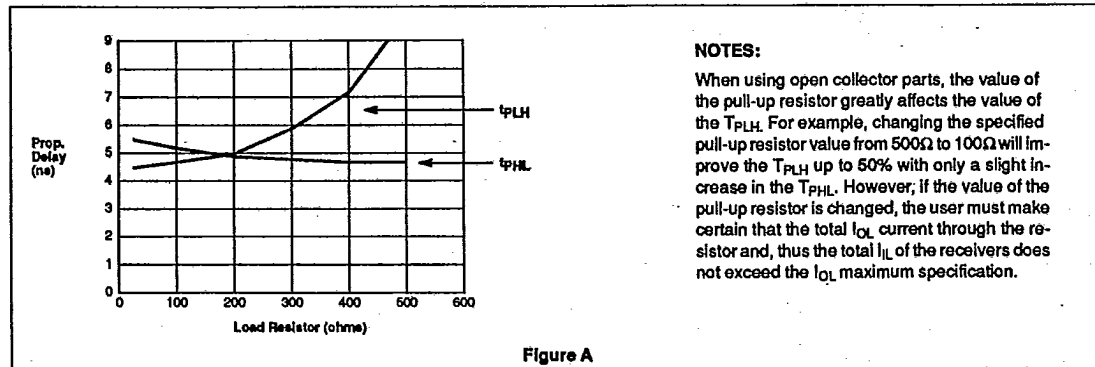
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TYPICAL PROPAGATION DELAYS vs. LOAD RESISTOR FOR OPEN COLLECTOR OUTPUTS



TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs and Open Collector Outputs

Input Pulse Definitions

TEST POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
t_{PHL}	closed
All other	open

DEFINITIONS:
 R_L = Load Resistor; see AC Characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
 V_X = Unlocked pins must be held at: $\leq 0.3V$; $\geq 2.7V$ or open per Function Table.

INPUT PULSE CHARACTERISTICS

Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$