查询"5962-89545012A"供应商

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: [illegible]

DRAWING APPROVAL DATE: 13 MARCH 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, 8-BIT BIDIRECTIONAL BINARY COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89545

SHEET 1 OF 16

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1197

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89545	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F579	8-bit bidirectional binary counter, with three-state outputs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input current range	-30 to +5.0 mA
Voltage applied to output in high output state	-0.5 to $+V_{CC}$
Current applied to output in low output state	40 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	825 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage (V_{IH})	2.0 V
Low level input voltage (V_{IL})	0.8 V
Case temperature (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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1.4 Recommended operating conditions - Continued. 2/

Minimum setup time, I/O_n to CP ($t_{S(H)}$, $t_{S(L)}$):
T_C = +25°C - 3.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 4.0 ns
Minimum hold time, I/O_n to CP ($t_{h(H)}$, $t_{h(L)}$):
T_C = +25°C - 0.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 0.0 ns

Minimum setup time, $\overline{PE}$, $\overline{SR}$, or $\overline{CS}$ to CP, ($t_{S(H)}$):
T_C = +25°C - 9.5 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 11.0 ns

Minimum setup time, $\overline{PE}$, $\overline{SR}$, or $\overline{CS}$ to CP, ($t_{S(L)}$):
T_C = +25°C - 9.5 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 13.0 ns

Minimum hold time, $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP, ($t_{h(H)}$, $t_{h(L)}$):
T_C = +25°C - 0.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 0.0 ns

Minimum setup time, $\overline{CEP}$ or $\overline{CET}$ to CP, ($t_{S(H)}$):
T_C = +25°C - 5.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 7.5 ns

Minimum setup time, $\overline{CEP}$ or $\overline{CET}$ to CP, ($t_{S(L)}$):
T_C = +25°C - 9.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 11.5 ns

Minimum hold time $\overline{CEP}$ or $\overline{CET}$ to CP, ($t_{h(H)}$, $t_{h(L)}$):
T_C = +25°C - 0.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 0.0 ns
Minimum clock pulse width, ($t_{W(H)}$, $t_{W(L)}$):
T_C = +25°C - 4.5 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 6.0 ns

Minimum $\overline{MR}$ pulse width ($t_{W(L)}$):
T_C = +25°C - 3.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 3.0 ns
Minimum recovery time (t_{REC}):
T_C = +25°C - 4.0 ns
T_C = -55°C, +125°C - - - - - - - - - - - - - - - - - - 5.0 ns

2/ See figure 4, waveform 5.

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specifications and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.2.5 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage $\overline{TC}$	V_{OH1}	V_{CC} = 4.5 V, V_{IL} = 0.8 V V_{IH} = 2.0 V, I_{OH} = -1.0 mA		1, 2, 3	2.5		V
High level output voltage, I/O_n	V_{OH2}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.8 V	I_{OH} = -3.0	1, 2, 3	2.4		V
			I_{OH} = -1.0	1, 2, 3	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 20 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V		1, 2, 3		0.50	V
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3		-1.2	V
Input current at maximum input voltage	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 5.5 V	I/O_n	1, 2, 3		1.0	mA
		V_{CC} = 5.5 V V_{IN} = 7.0 V	all others	1, 2, 3		100	µA
High level input current, except I/O_n	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3		20	µA
Low level input current, except I/O_n	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.5 V		1, 2, 3		0.6	mA
Off state current high level voltage applied to I/O_n	I_{OZH}	V_{CC} = 5.5 V, V_{IN} = 2.7 V, V_{IH} = 2.0 V		1, 2, 3		70	µA
Off state current low level voltage applied to I/O_n	I_{OZL}	V_{CC} = 5.5 V, V_{IN} = 0.5 V, V_{IH} = 2.0 V		1, 2, 3		-600	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND 1/		1, 2, 3	-60	-150	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C < T_C < +125^{\circ}C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Supply current (total)	I_{CCH}	V_{CC} = 5.5 V		1, 2, 3		135	mA
	I_{CCL}			1, 2, 3		145	mA
	I_{CCZ}			1, 2, 3		150	mA
Functional tests		See 4.3.1c		7, 8			
Maximum clock frequency	f_{MAX}	See waveform 1 2/		9 10,11	100 80		MHz
Propagation delay CP to I/O_n	t_{PLH1}	V_{CC} = 5.0 V C_L = 50 pF R_L = 500Ω See figure 4	See waveform 1	9 10,11	5.0 4.5	10.5 23.0	ns
	t_{PHL1}			9 10,11	5.0 5.0	10.5 12.5	ns
Propagation delay CP to $\overline{TC}$	t_{PLH2}		See waveform 1	9 10,11	5.5 5.0	10.0 19.5	ns
	t_{PHL2}			9 10,11	5.5 5.0	10.0 12.0	ns
Propagation delay $\overline{U/D}$ to $\overline{TC}$	t_{PLH3}		See waveform 4	9 10,11	3.5 3.5	8.0 12.5	ns
	t_{PHL3}			9 10,11	4.5 4.5	8.0 10.0	ns
Propagation delay $\overline{CET}$ to $\overline{TC}$	t_{PLH4}		See waveform 3	9 10, 11	3.5 3.5	7.0 9.5	ns
	t_{PHL4}			9 10,11	3.5 3.5	8.0 9.0	ns
Propagation delay $\overline{MR}$ to I/O_n	t_{PHL5}		See waveform 2	9 10,11	5.0 5.0	9.0 11.0	ns

See footnotes at end of table

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Output disable time from high to low level $\overline{CS}$, $\overline{PE}$, to I/O_n	t_{PHZ1}	V_{CC} = 5.0 V C_L = 50 pF R_L = 500Ω See figure 4	See waveform 6	9 10,11	3.0 3.0	7.5 10.0	ns
	t_{PLZ1}		See waveform 7	9 10,11	6.5 5.5	9.5 12.0	ns
Output enable time to high or low level $\overline{CS}$, $\overline{PE}$, to I/O_n	t_{PZH2}		See waveform 6	9 10,11	5.0 3.5	10.5 12.5	ns
	t_{PZL2}		See waveform 7	10,11 10,11	6.5 5.5	10.5 13.0	ns
Output disable time from high to low level $\overline{OE}$ to I/O_n	t_{PHZ3}		See waveform 6	9 10,11	1.0 1.0	4.0 8.0	ns
	t_{PLZ3}		See waveform 7	9 10,11	2.5 2.0	7.0 10.0	ns
Output enable time to high or low level $\overline{OE}$ to I/O_n	t_{PZH4}		See waveform 6	9 10,11	4.0 3.5	8.5 11.0	ns
	t_{PZL4}		See waveform 7	9 10,11	5.0 4.5	9.5 11.5	ns

1/ Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus, sample-and-hold techniques, or both are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

2/ This parameter is guaranteed but not tested to the specified limits in table I.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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Case outlines	R and S	2
Terminal number	Terminal symbol	
1	CP	$\overline{CET}$
2	I/O_0	$\overline{CEP}$
3	I/O_1	$\overline{SR}$
4	I/O_2	$\overline{MR}$
5	I/O_3	CP
6	GND	I/O_0
7	I/O_4	I/O_1
8	I/O_5	I/O_2
9	I/O_6	I/O_3
10	I/O_7	GND

Case outlines	R and S	2
Terminal number	Terminal symbol	
11	$\overline{OE}$	I/O_4
12	$\overline{CS}$	I/O_5
13	$\overline{PE}$	I/O_6
14	$U/\overline{D}$	I/O_7
15	$\overline{TC}$	$\overline{OE}$
16	V_{CC}	$\overline{CS}$
17	$\overline{CET}$	$\overline{PE}$
18	$\overline{CEP}$	$U/\overline{D}$
19	$\overline{SR}$	$\overline{TC}$
20	$\overline{MR}$	V_{CC}

FIGURE 1. Terminal connections.

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Inputs									Operating mode
$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low to High clock transition

(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be low voltage level at the same time.

FIGURE 2. Truth table.

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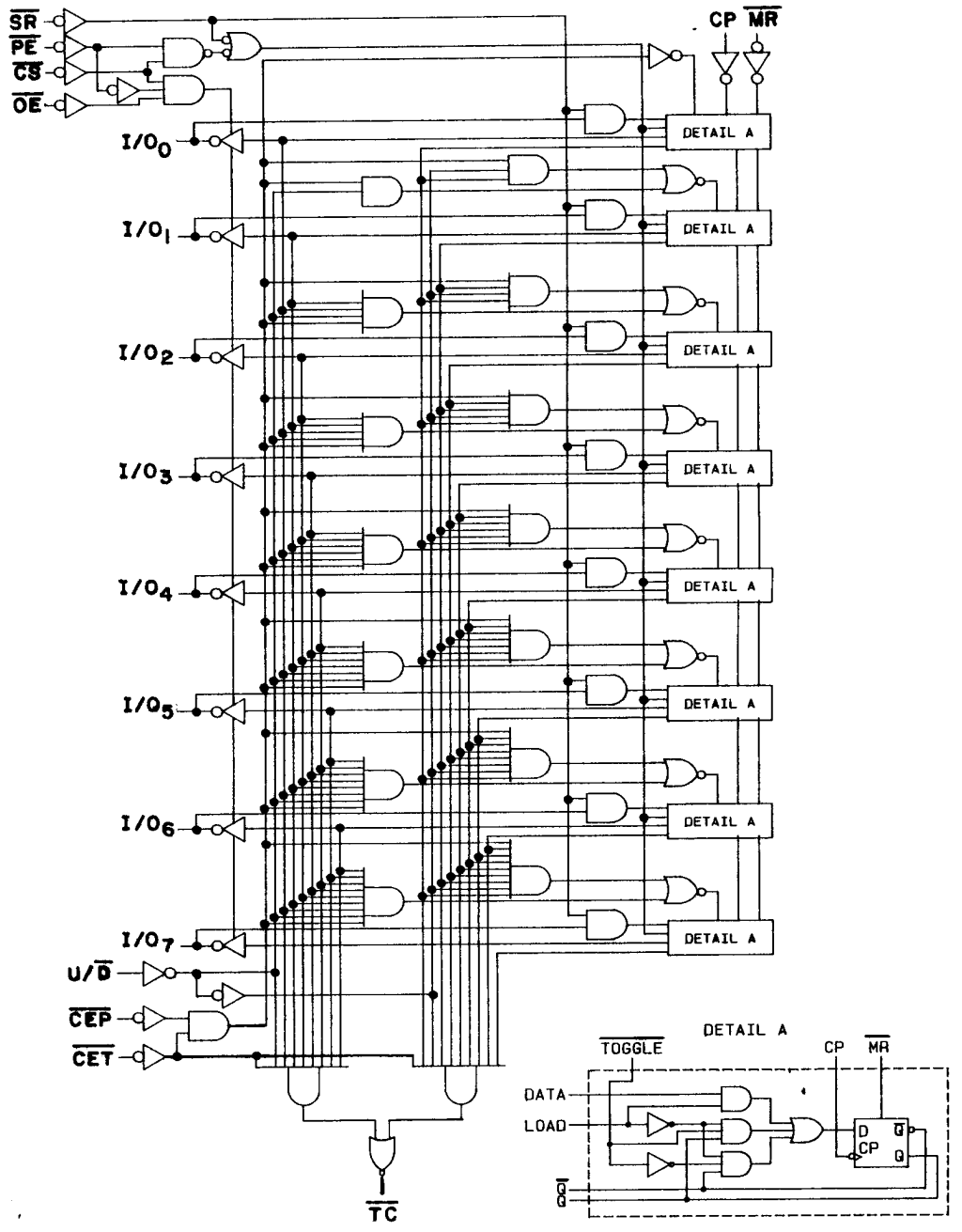

FIGURE 3. Logic diagram.

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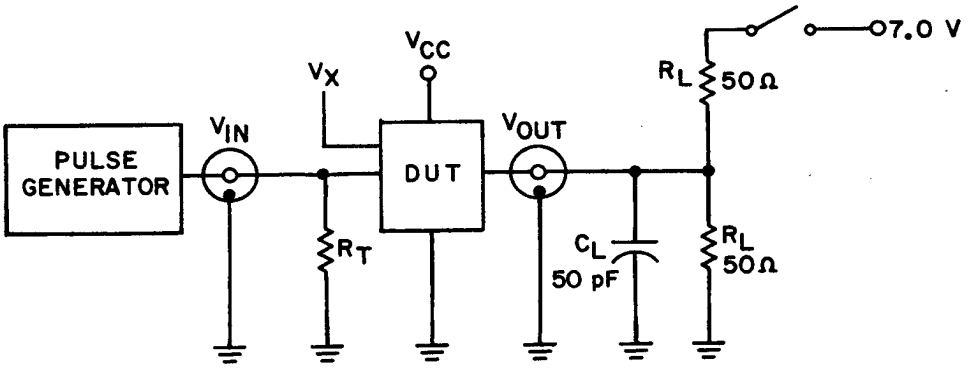
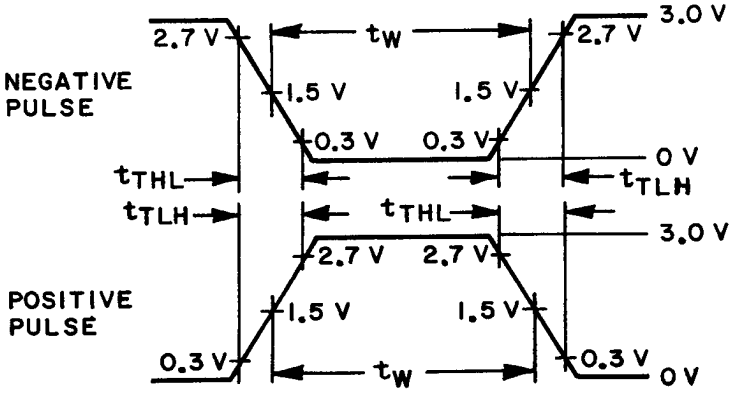


Switch position

Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
All other	Open



NOTES:
1. Input pulse characteristics: PRR = 1 MHz, t_W = 500 ns, t_{TLH} = t_{THL} ≤2.5 ns, duty cycle = 50 percent.
2. R_T = Termination resistance should be equal to Z_{OUT} of pulse generator.
3. V_X = Unclocked pins must be held at ≤0.8 V, ≥2.7 V or open.

FIGURE 4. Test circuit and switching waveforms.

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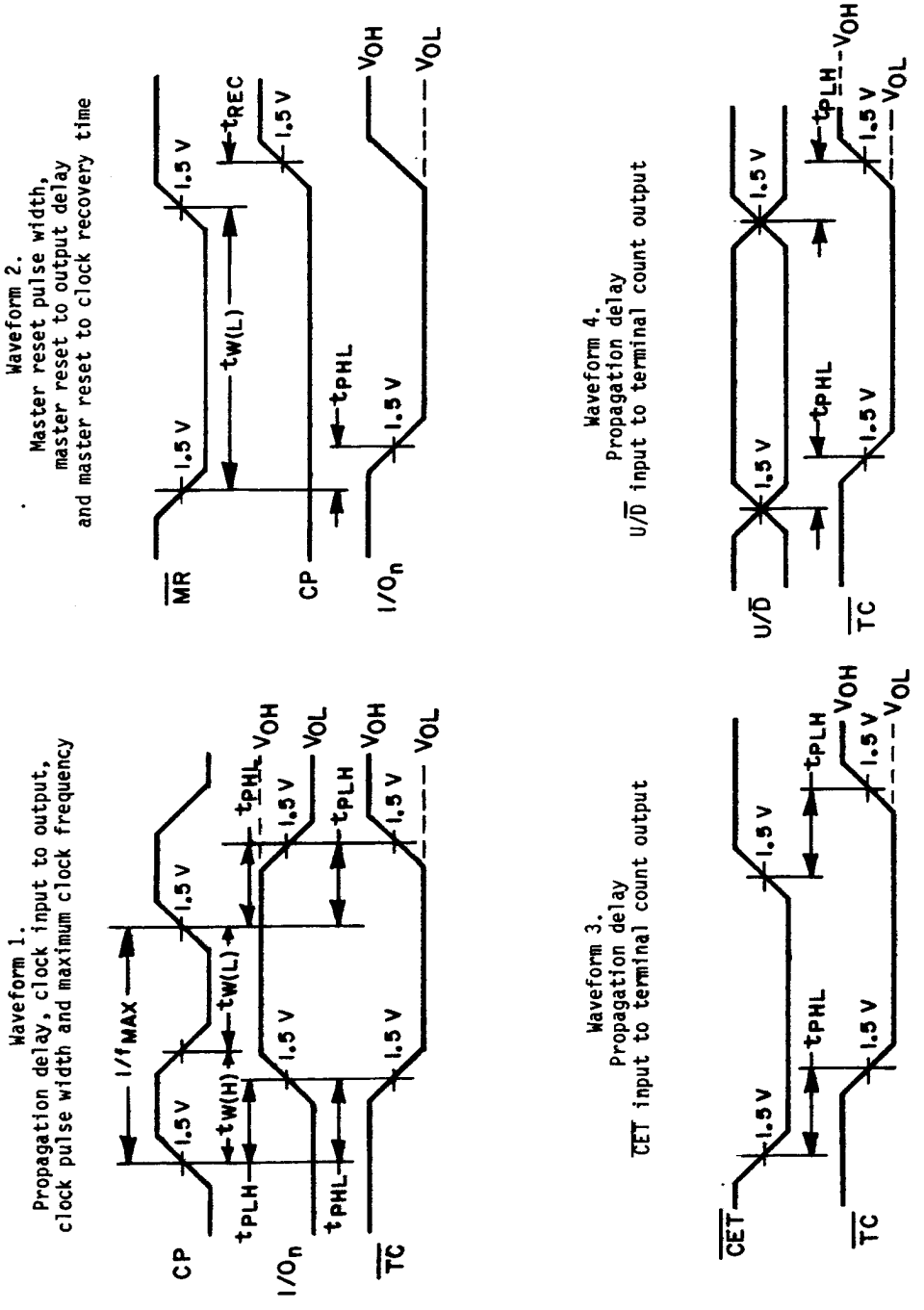

FIGURE 4. Test circuit and switching waveforms - Continued.

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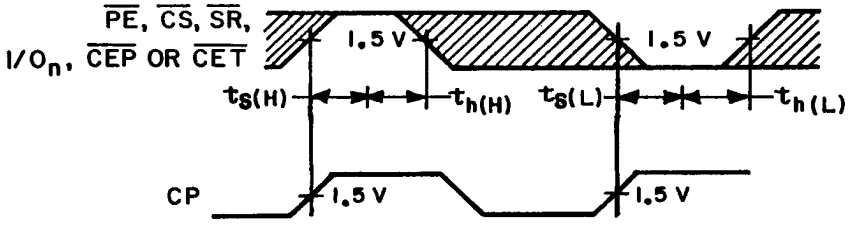
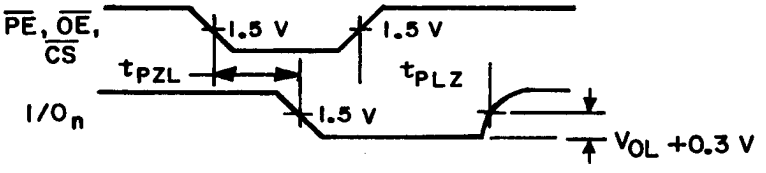
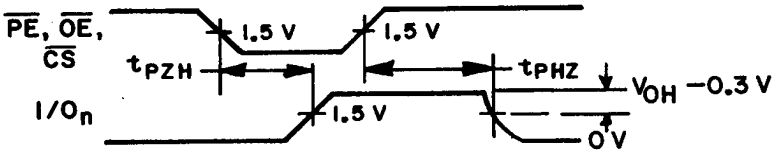
Waveform 5.
Data setup and hold times



Waveform 6.
Three-state output enable time to high level
and output disable time from high level



Waveform 7.
Three-state output enable time to low level
and output disable time from low level



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

FIGURE 4. Test circuit and switching waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 and 8 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Group C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-89545012RX	18324	54F579/BRA
5962-89545012SX	18324	54F579/BSA
5962-89545012X	18324	54F579/B2A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834

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