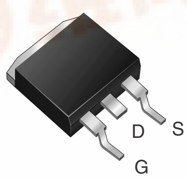
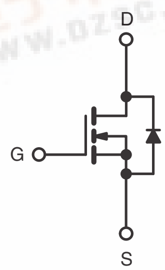
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.40
Q_g (Max.) (nC)	43	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	23	
Configuration	Single	

D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* COMPLIANT
HALOGEN FREE Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION			
Package	D²PAK (TO-263)	D²PAK (TO-263)	D²PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF630S-GE3	SiHF630STRL-GE3[a]	SiHF630STRR-GE3[a]
Lead (Pb)-free	IRF630SPbF	IRF630STRLPbF[a]	IRF630STRRPbF[a]
	SiHF630S-E3	SiHF630STL-E3[a]	SiHF630STR-E3[a]
SnPb	IRF630S	IRF630STRL[a]	IRF630STRR[a]
	SiHF630S	SiHF630STL[a]	SiHF630STR[a]

Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	9.0	A
		T_C = 100 °C		5.7	
Pulsed Drain Current[a]			I_{DM}	36	
Linear Derating Factor				0.59	W/°C
Linear Derating Factor (PCB Mount)[e]				0.025	
Single Pulse Avalanche Energy[b]			E_{AS}	250	mJ
Repetitive Avalanche Current[a]			I_{AR}	9.0	A
Repetitive Avalanche Energy[a]			E_{AR}	7.4	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	74	W
Maximum Power Dissipation (PCB Mount)[e]	T_A = 25 °C			3.0	

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Peak Diode Recovery dV/dt[c]		dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 4.6 mH, R_g = 25 Ω, I_{AS} = 9.0 A (see fig. 12).
c. I_{SD} ≤ 9.0 A, dI/dt ≤ 120 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).
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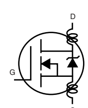
THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount)[c]	R_{thJA}	-	-	40	°C/W
Maximum Junction-to-Ambient	R_{thJA}	-	-	62	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	1.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.24	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 160V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 5.4 A[b]	-	-	0.40	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 5.4 A[b]		3.8	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	800	-	pF
Output Capacitance	C_{oss}			-	240	-	
Reverse Transfer Capacitance	C_{rss}			-	76	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 5.9 A, V_{DS} = 160 V see fig. 6 and 13[b]	-	-	43	nC
Gate-Source Charge	Q_{gs}			-	-	7.0	
Gate-Drain Charge	Q_{gd}			-	-	23	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 5.9 A R_g = 12 Ω, R_D= 16 Ω see fig. 10[b]		-	9.4	-	ns
Rise Time	t_r			-	28	-	
Turn-Off Delay Time	$t_{d(off)}$			-	39	-	
Fall Time	t_f			-	20	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	

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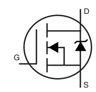
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.0	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	36	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 9.0 A, V_{GS} = 0 V[b]	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 5.9 A, dI/dt = 100 A/μs[b]	-	170	340	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.1	2.2	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR-4 or G-10 material).

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

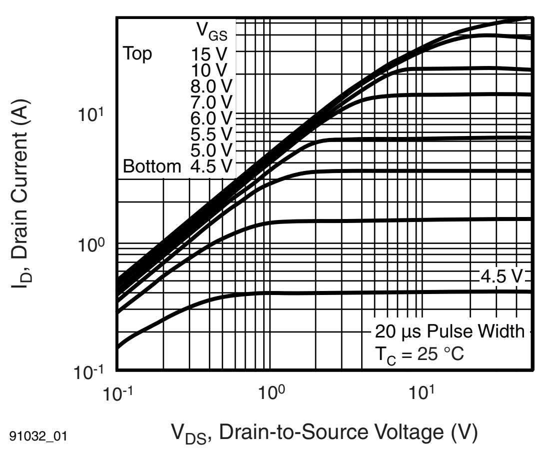


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

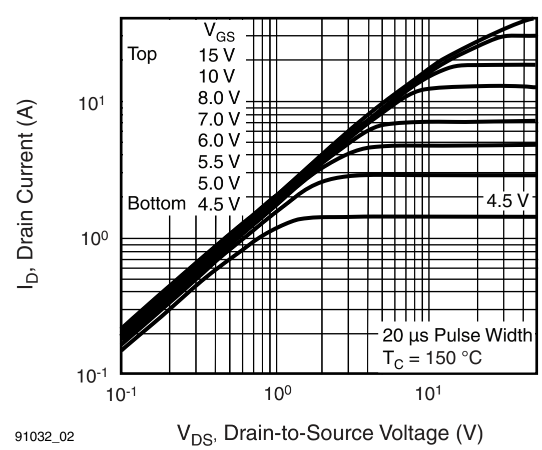


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

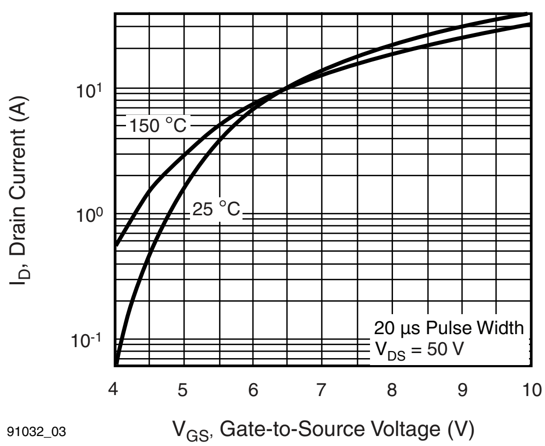


Fig. 3 - Typical Transfer Characteristics

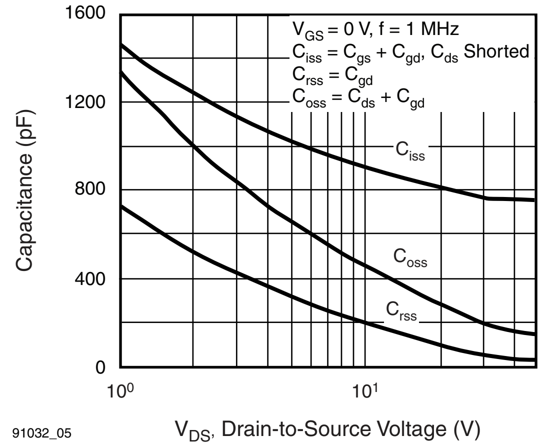


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

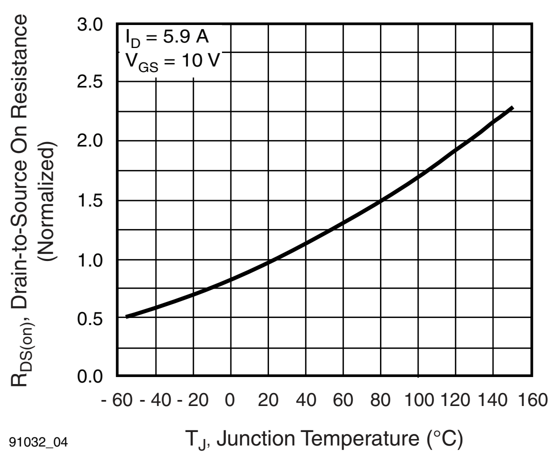


Fig. 4 - Normalized On-Resistance vs. Temperature

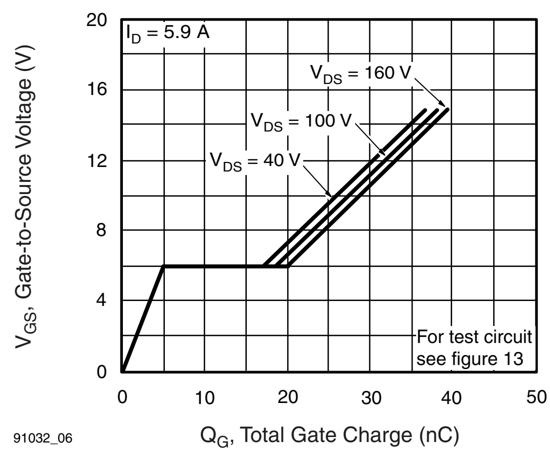


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

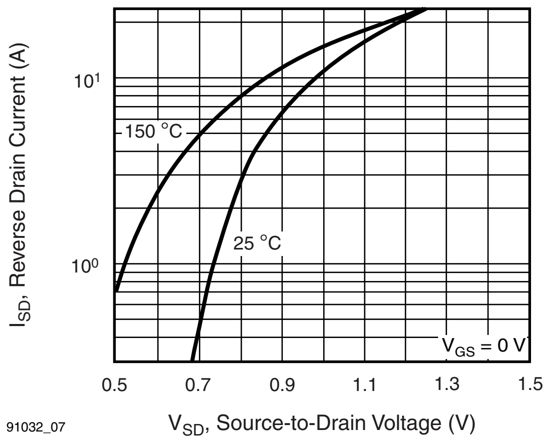


Fig. 7 - Typical Source-Drain Diode Forward Voltage

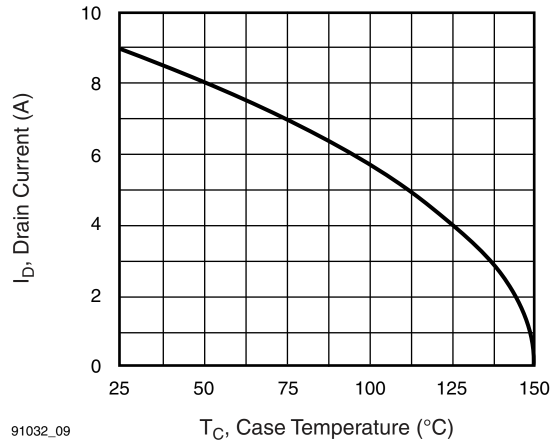


Fig. 9 - Maximum Drain Current vs. Case Temperature

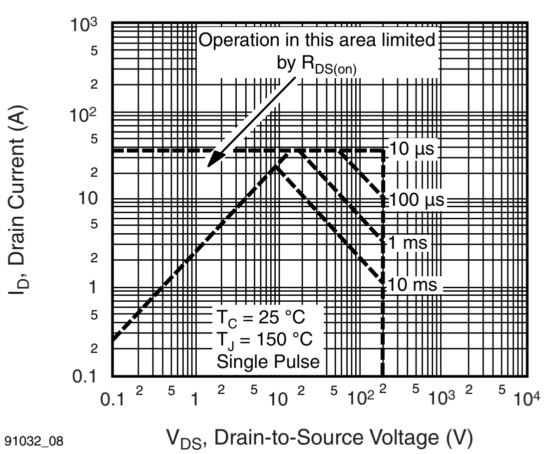


Fig. 8 - Maximum Safe Operating Area

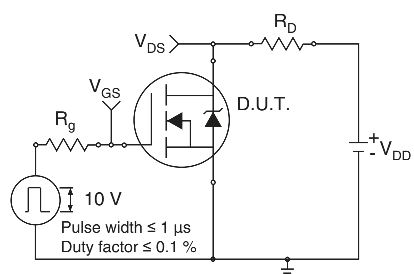


Fig. 10a - Switching Time Test Circuit

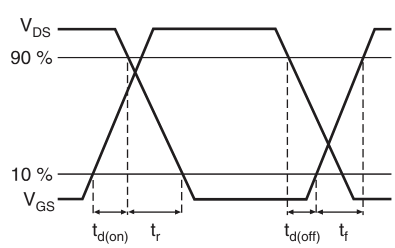


Fig. 10b - Switching Time Waveforms

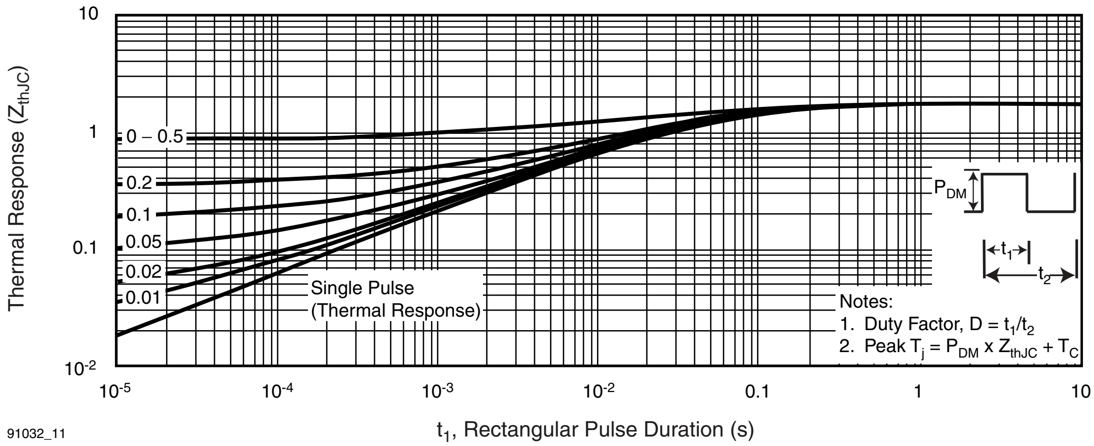


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

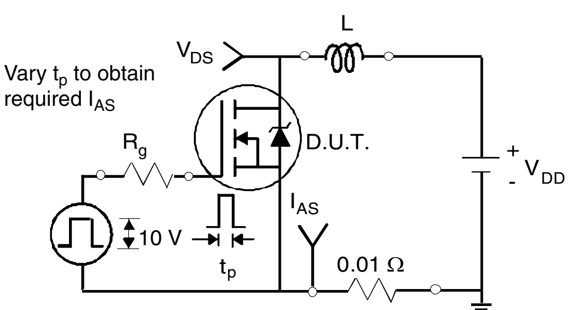


Fig. 12a - Unclamped Inductive Test Circuit

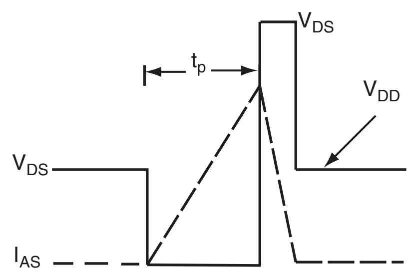


Fig. 12b - Unclamped Inductive Waveforms

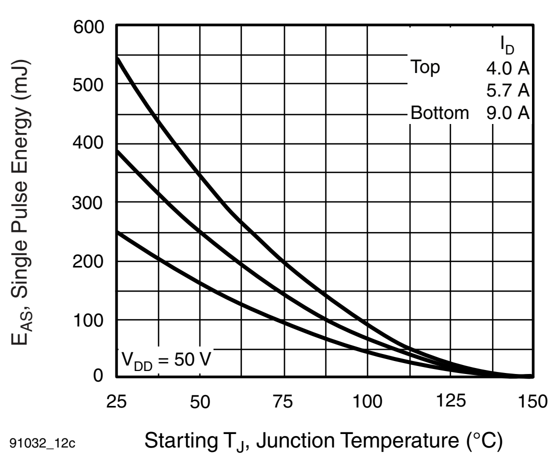


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

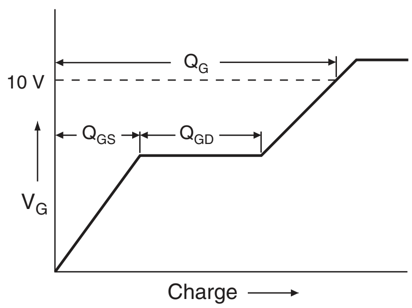


Fig. 13a - Basic Gate Charge Waveform

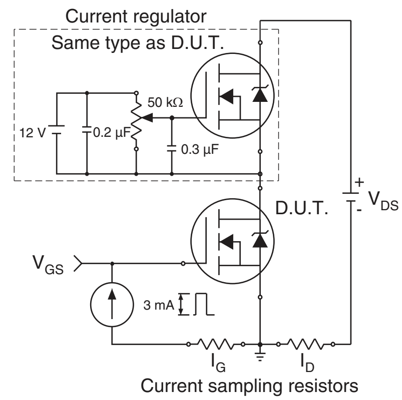
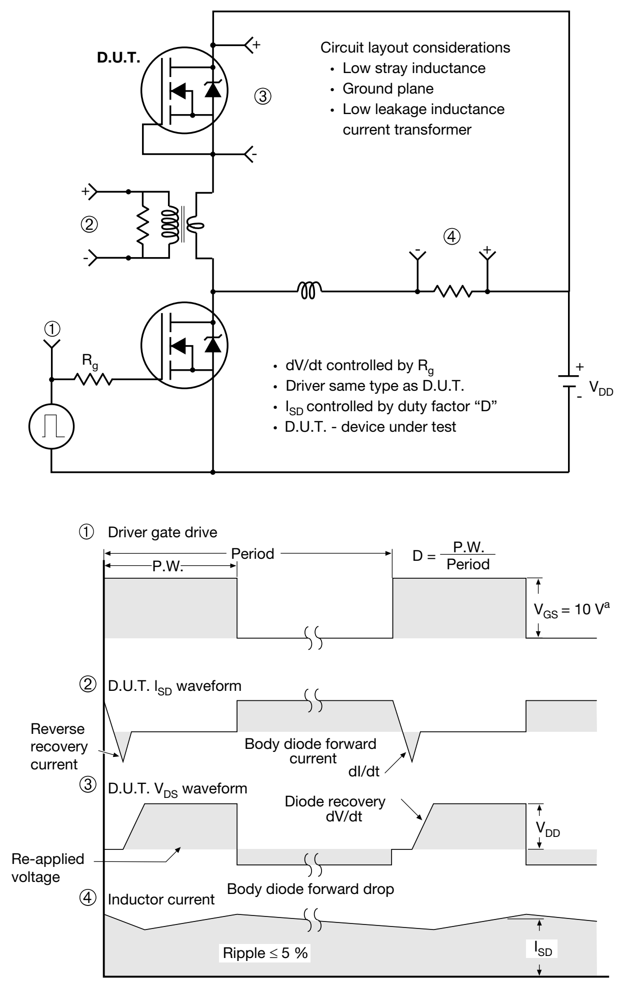


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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