REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17																	
REV STATUS				REV																
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Rajesh Pithadia	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Rajesh Pithadia APPROVED BY Raymond Monnin DRAWING APPROVAL DATE 97-04-29 REVISION LEVEL	MICROCIRCUIT, DIGITAL, 3.3 V PHASE LOCK LOOP CLOCK DRIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON SIZE A | CAGE CODE 67268 | **5962-97540** SHEET 1 OF 17

DSCC FORM 2233
APR 97

5962-E203-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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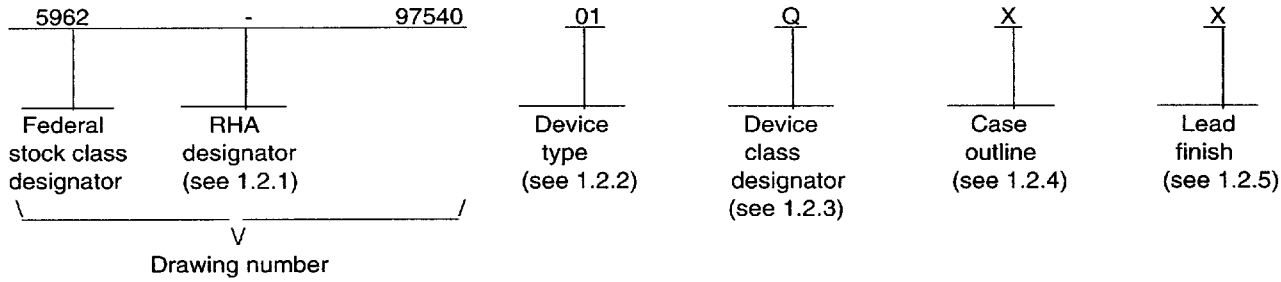
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54CDC586	3.3 V Phase Lock Loop Clock Driver with 3-State Outputs, TTL Compatible Inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDFP1-F56	56	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +4.6 V dc
DC input voltage range (V_{IN})	-0.5 V dc to +7.0 V dc 4/
Voltage range applied to any output in the high state or power-off state (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc 4/
Current into any output in the low state, I_O	+64 mA
DC input clamp current (I_{IK}) (V_{IN} < 0.0)	-20 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0)	-50 mA
Maximum power dissipation at T_A = +55°C (in still air) (P_D)	1.2 W 5/
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/ 6/

Supply voltage range (V_{CC})	+3.0 V dc to +3.6 V dc
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	+0.8 V
Input voltage range (V_{IN})	+0.0 V dc to 5.5 V dc
Maximum high level output current (I_{OH})	-32 mA
Maximum low level output current (I_{OL})	+32 mA
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ The input and output negative-voltage ratings may be exceeded provided that the input and output clamp-current ratings are observed.
5/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
6/ Unused inputs must be held high or low to prevent them from floating.
7/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Conditions 2/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 3/		Unit
					Min	Max	
Input clamp voltage	V_{IK}	V_{CC} = 3 V, I_I = -18 mA	1, 2, 3	01		-1.2	V
High-level output voltage (3006)	V_{OH} 4/	V_{CC} = 3 V to 3.6 V, I_{OH} = -100 µA	1, 2, 3	01	V_{CC} - 0.2		V
		V_{CC} = 3 V, I_{OH} = -32 mA			2		
Low-level output voltage (3007)	V_{OL} 4/	V_{CC} = 3 V, I_{OL} = 100 µA	1, 2, 3	01		0.2	V
		V_{CC} = 3 V, I_{OL} = 32 mA				0.5	
Input current high (3010)	I_{IH} 5/	V_{CC} = 0 V or 3.6 V, V_I = 3.6 V	1, 2, 3	01		+10.0	µA
		V_{CC} = 3.6 V, V_I = V_{CC} or GND				+1.0	
Input current low (3009)	I_{IL} 6/	V_{CC} = 0 V or 3.6 V, V_I = 3.6 V	1, 2, 3	01		-10.0	µA
		V_{CC} = 3.6 V, V_I = V_{CC} or GND				-1.0	
Three-state output leakage current high (3021)	I_{OZH}	V_{CC} = 3.6 V, V_{OUT} = 3 V	1, 2, 3	01		+10.0	µA
Three-state output leakage current low (3020)	I_{OZL}	V_{CC} = 3.6 V, V_{OUT} = 0 V	1, 2, 3	01		-10.0	µA
Quiescent supply current (3005)	I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_{IN} = V_{CC} or GND, outputs high	1, 2, 3	01		1.0	mA
		V_{CC} = 3.6 V, I_O = 0, V_{IN} = V_{CC} or GND, outputs low				1.0	
		V_{CC} = 3.6 V, I_O = 0, V_{IN} = V_{CC} or GND, outputs disabled				1.0	
Input capacitance (3012)	C_{IN}	T_C = +25 C, V_{CC} = 3.0 V, See 4.4.1c	4	01		4.0	pF
Output capacitance (3012)	C_{OUT}	T_C = +25 C, V_{CC} = 3.0 V, See 4.4.1c	4	01		8.0	pF
Functional tests (3014)	7/	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 3.0 V, Verify output V_{OUT}, See 4.4.1b	7, 8	01	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Conditions 2/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 3/		Unit
					Min	Max	
Clock frequency	f_{CLK}	VCO is operating at four times the CLKIN frequency. V_{CC} = 3.0 V	9, 10, 11	01	25.0	50.0	MHz
		VCO is operating at double the CLKIN frequency. V_{CC} = 3.0 V			50.0	100.0	
Input clock duty cycle	-----	V_{CC} = 3.0 V	9, 10, 11	01	40	60	%
Stabilization time	8/	After SEL1, SEL0, V_{CC} = 3.0 V	9, 10, 11	01		50.0	µs
		After $\overline{OE}$ ↓				50.0	
		After power up, V_{CC} = 3.0 V				50.0	
		After CLKIN, V_{CC} = 3.0 V				50.0	
Maximum operating frequency	f_{MAX} 9/	C_L = 30 pF minimum See figure 4 V_{CC} = 3.0 V	9, 10 ,11	01	100.0		MHz
Duty cycle to Y	----- 9/	C_L = 30 pF minimum See figure 4 V_{CC} = 3.0 V	9, 10, 11	01	42	58	%
Propagation delay	$t_{phase\ error}$ 9/ 10/	C_L = 30 pF minimum See figure 4 CLKIN ↑ to Y V_{CC} = 3.0 V	9, 10, 11	01	-900	200	ps
Output skew	$t_{sk(o)}$ 9/ 10/	C_L = 30 pF minimum See figure 4 V_{CC} = 3.0 V	9, 10, 11	01		0.75	ns
Process skew	$t_{sk(pr)}$ 9/ 10/	C_L = 30 pF minimum See figure 4 V_{CC} = 3.0 V	9, 10, 11	01		1.1	ns
Rise time	t_r 9/	C_L = 30 pF minimum See figure 4 V_{CC} = 3.0 V	9, 10, 11	01		1.4	ns
Fall time	t_f 9/	C_L = 30 pF minimum See figure 4 V_{CC} = 3.0 V	9, 10, 11	01		1.4	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883, utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{CC} test, where the output terminals shall be open. When performing the I_{CC} test, the current meter shall be placed in the circuit such that all current flows through the meter. The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}. For all other inputs $V_{IN} = V_{CC}$ or GND.

5/ For input under test, $V_{IN} = 3.6$ V. For all other inputs, $V_{IN} = V_{CC}$ or GND.

6/ For input under test, V_{IN} = GND. For all other inputs, $V_{IN} = 3.6$ V.

7/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs, $L \le V_{IL}$ max, $H \ge V_{IH}$ min, where V_{IL} max and V_{IH} min are listed in section 1.4 herein.

8/ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

9/ The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

10/ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are valid only for equal loading of all outputs.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	30	GND
2	AV_{CC}	31	GND
3	AGND	32	3Y1
4	FBIN	33	V_{CC}
5	AGND	34	GND
6	SEL0	35	3Y2
7	SEL1	36	V_{CC}
8	GND	37	GND
9	GND	38	3Y3
10	1Y1	39	V_{CC}
11	V_{CC}	40	GND
12	GND	41	GND
13	1Y2	42	4Y1
14	V_{CC}	43	V_{CC}
15	GND	44	GND
16	1Y3	45	4Y2
17	V_{CC}	46	V_{CC}
18	GND	47	GND
19	GND	48	4Y3
20	2Y1	49	V_{CC}
21	V_{CC}	50	$\overline{CLR}$
22	GND	51	TEST
23	2Y2	52	$\overline{OE}$
24	V_{CC}	53	AV_{CC}
25	GND	54	NC
26	2Y3	55	CLKIN
27	V_{CC}	56	NC
28	NC		
29	NC		

FIGURE 1. Terminal connections.

Output configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2X FREQENCY	1X FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

Note: n = 1, 2, 3.

Output configuration A is valid when any output configured as 1x frequency output is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at one-half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as CLKIN.

Output configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1X FREQENCY	2X FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

Note: n = 1, 2, 3.

Output configuration B is valid when any output configured as 1x frequency output is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of CLKIN.

FIGURE 2. Truth tables.

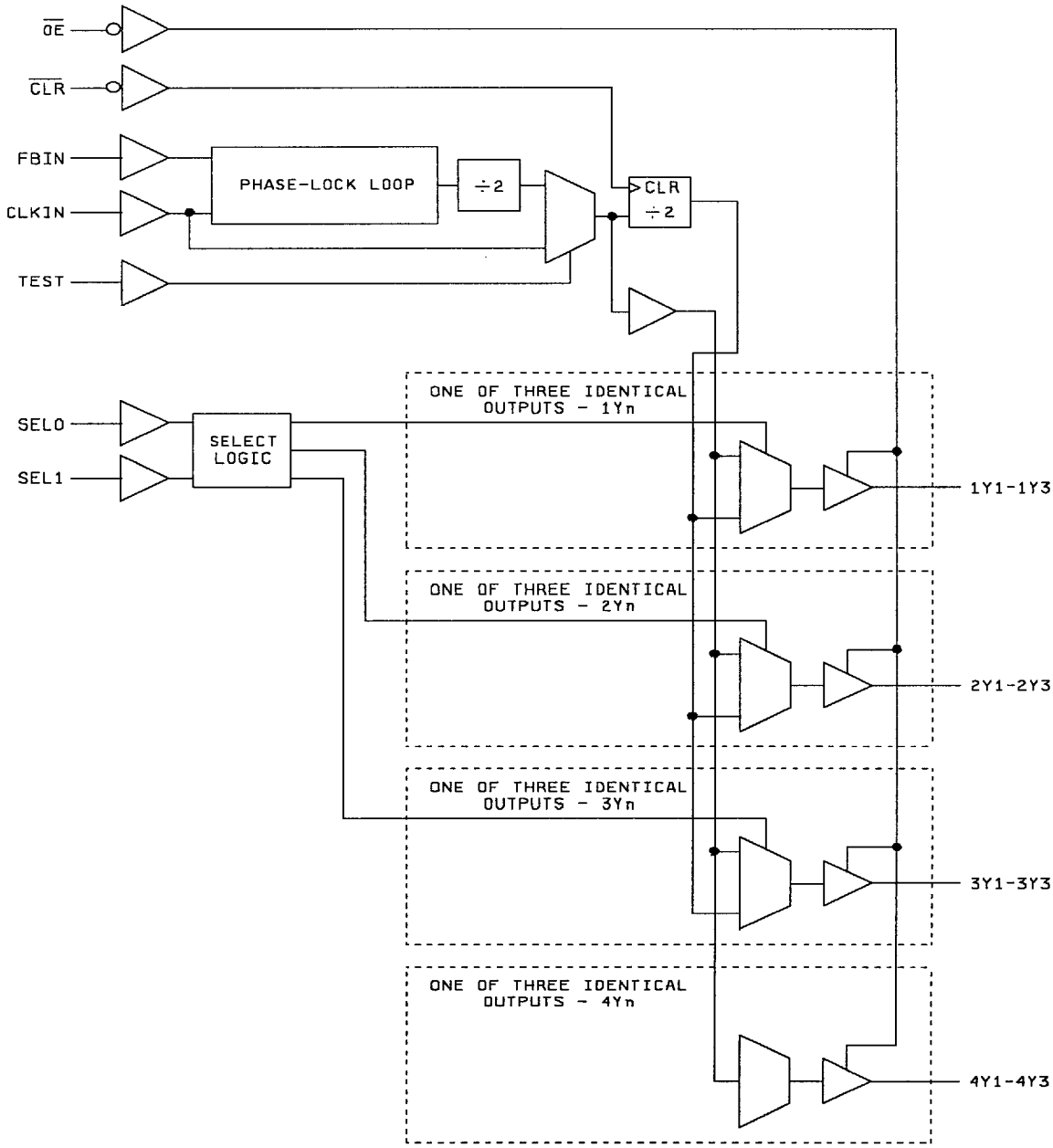
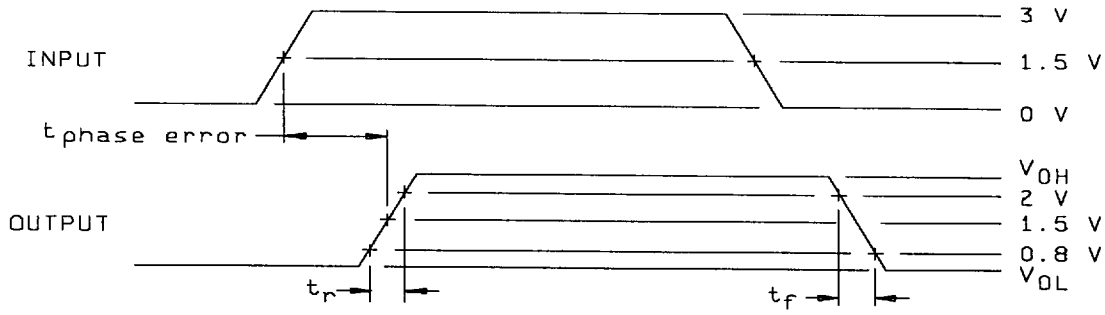
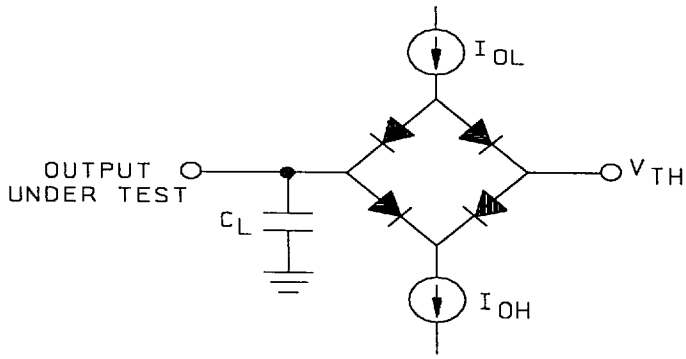


FIGURE 3. Block diagram.



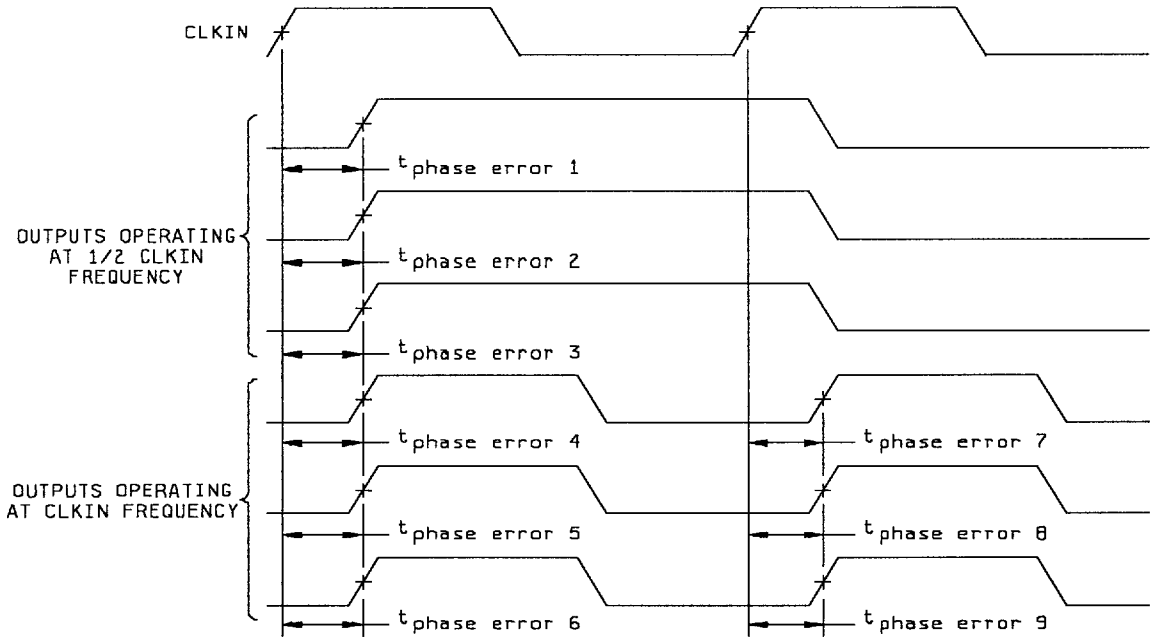
PROPAGATION DELAY TIMES



Parameter	I_{OL}	I_{OH}	V_{TH}	C_L
$t_{phase\ error}$	32 mA	32 mA	1.5 V	20 pF
t_r, t_f	16 mA	16 mA	1.5 V	20 pF

NOTES: 1. C_L includes probe and jig capacitance.
2. The outputs are measured one at a time with one transition per measurement.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

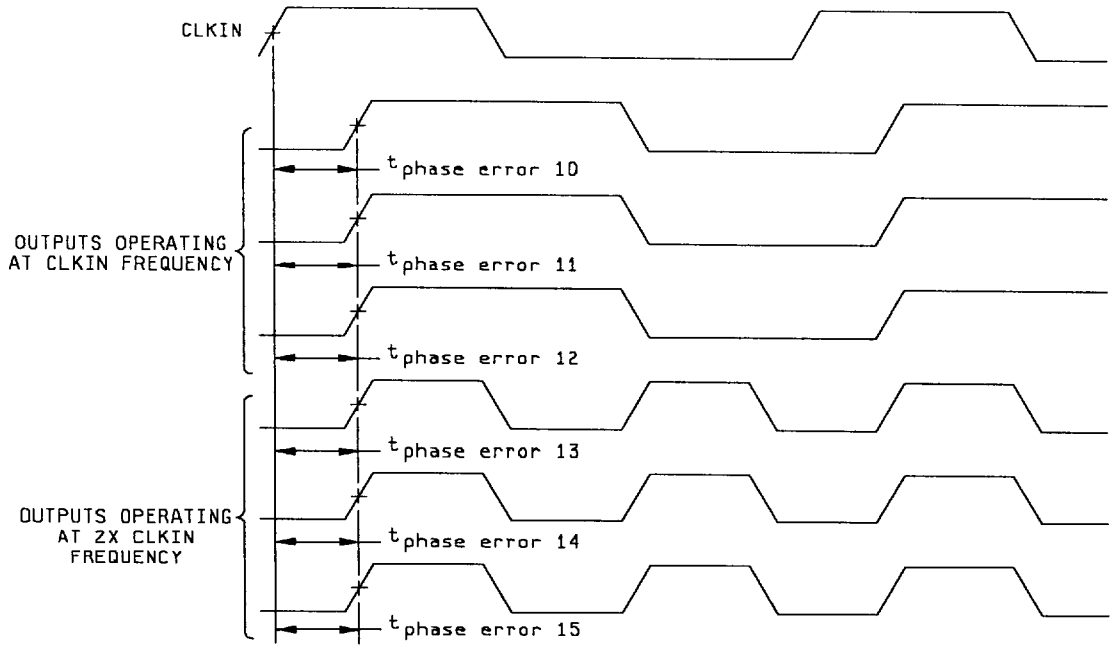
FIGURE 4. Test circuit and switching waveforms.



NOTES: 1. Output skew, $t_{sk(o)}$, is calculated as the greater of:
   a. The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, ...6)
   b. The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

2. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
   a. The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, ...6) across multiple devices under identical operating conditions.
   b. The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions.

FIGURE 4. Test circuit and switching waveform - Continued.



NOTES: 1. Output skew, $t_{sk(o)}$, is calculated as the greater of:
   a. The difference between the fastest and slowest of $t_{\text{phase error n}}$ (n = 10, 11, ...15)

2. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
   a. The difference between the maximum and minimum $t_{\text{phase error n}}$ (n = 10, 11, ...15) across multiple devices under identical operating conditions.

FIGURE 4. Test circuit and switching waveforms - Continued.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----	----	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1,2, 3,7, 8,9,10,11	2/ 1, 2, 3,7, 8,9,10,11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

For C_{IN} and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-04-29

Approved sources of supply for SMD 5962-97540 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9754001QXA	01295	SNJ54CDC586WD

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.