MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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Military 56824

Advance Information

DSPRAM™
8K x 24 Bit Fast Static RAM

The 56824 is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high performance silicon-gate CMOS technology. This device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to Motorola's Military 56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic. This device can also be used as three 8K x 8 SRAMs by holding V/$\overline{S}$ low.

The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, which is useful in low-power applications. A single on-chip multiplexer selects A_{12} or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program memory select scalar operands. By connecting 56001 program memory select ($\overline{PS}$) to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource regardless of operand type. Refer to the application diagrams at the end of this data sheet for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

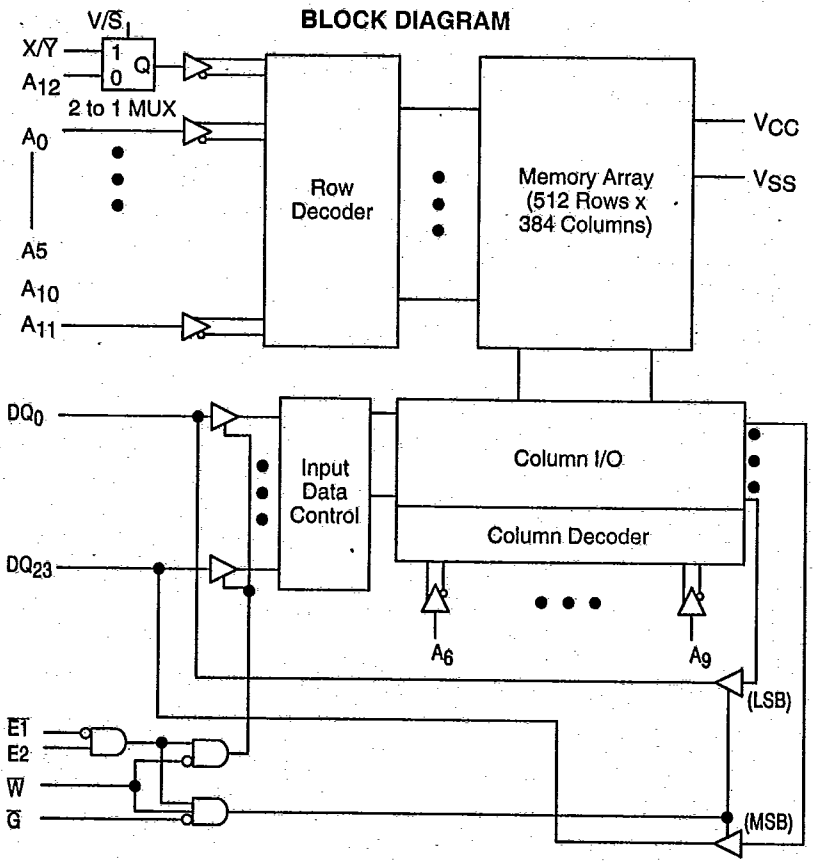
DSPRAM™

AVAILABLE AS
1) JAN: N/A
2) SMD: N/A
3) 883: 56824 - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CLCC: U

XX = Speed in ns (25, 30, 35)

- Single 5.0 V ± 10% Power Supply
- Fast Access Times: 25/30/35 ns
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- On-Chip Single Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three-State Outputs
- Low-Power Standby Mode
- Fully TTL Compatible

BLOCK DIAGRAM



PIN NAMES	
A_0 - A_{11}	Address Inputs
A_{12}, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexed Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Select
$\overline{G}$	Output Enable
DQ_0 - DQ_{23}	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of this device, all V_{SS} pins must be connected to ground.

DSPRAM is a trademark of Motorola, Inc.

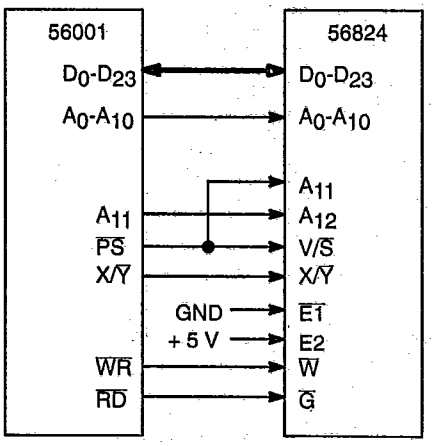
This document contains information on a new product. Specifications and information herein are subject to change without notice.

T-46-23-12

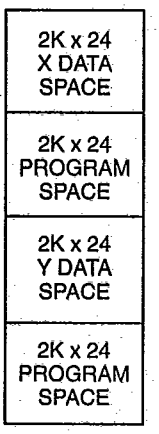
Truth Table							
$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	I/O Status	Supply Current
H	X	X	X	X	Not Selected	High - Z	I_{SB}
X	L	X	X	X	Not Selected	High - Z	I_{SB}
L	H	H	H	X	Output Disable	High - Z	I_{CC}
L	H	L	H	H	Read Using X/$\overline{Y}$	Data Out	I_{CC}
L	H	L	H	L	Read Using A_{12}	Data Out	I_{CC}
L	H	X	L	H	Write Using X/$\overline{Y}$	Data In	I_{CC}
L	H	X	L	L	Write Using A_{12}	Data In	I_{CC}

X = Don't Care

56001/56824 One-Chip Memory Solution
(4K Program/2K X-Data/2K Y-Data)

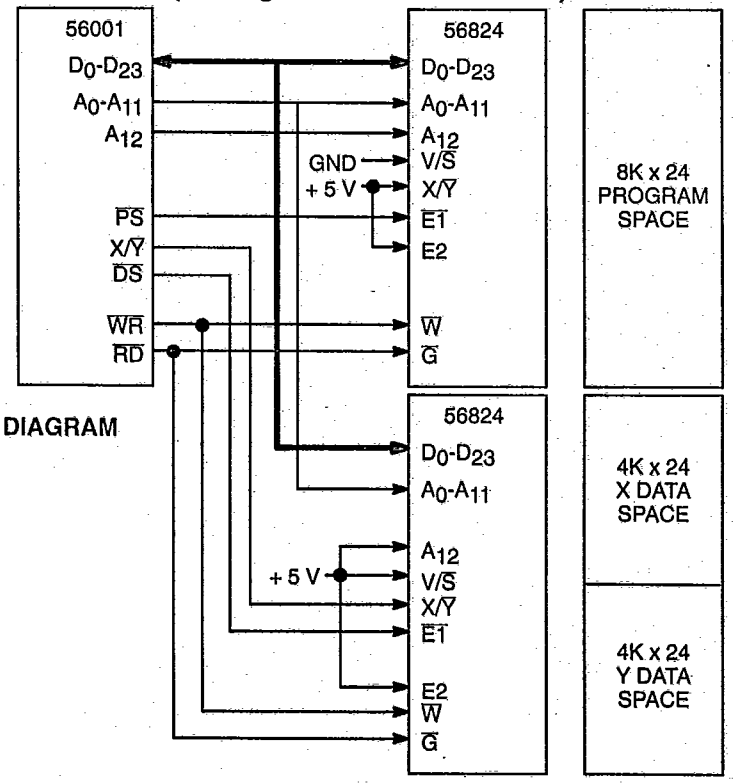


BLOCK DIAGRAM



MEMORY MAP

56001/56824 Two-Chip Memory Solution
(8K Program/4K X-Data/4K Y-Data)



BLOCK DIAGRAM

MEMORY MAP

NOTE: E2 may be connected to a 56001 high-order address bit to eliminate internal/external memory overlap.

BLOCK DIAGRAM

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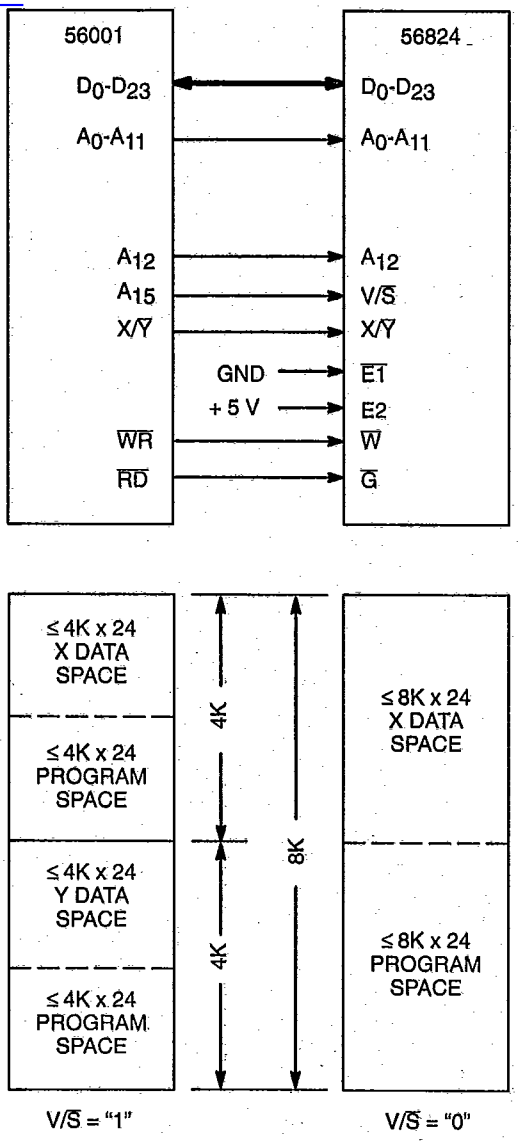
56001/56824 Dynamically Repartitioned Memory Solution



MEMORY MAPS

The DSPRAM may be dynamic repartitioned by connecting 56001 address A_{15} to V/S. This allows for software control of the relative sizes of the program and X and/or Y data spaces.