Monolithic Power Systems

# MP1527
## 2A, 1.3MHz Step-Up Converter

## General Description

The MP1527 is a 2A, fixed frequency step-up converter in a tiny 16 lead QFN package. The high 1.3MHz switching frequency allows for smaller external components producing a compact solution for medium-to-high current step-up, flyback, and SEPIC applications.

The MP1527 regulates the output voltage up to 25V at efficiency as high as 93%. Soft-start, timer-latch fault circuitry, cycle-by-cycle current limiting, and input undervoltage lockout prevent overstressing or damage to external circuitry at startup and output short-circuit conditions. Fixed frequency operation eases control of noise making the MP1527 optimal for noise sensitive applications such as mobile handsets and wireless LAN PC cards. Current-mode regulation and external compensation components allow the MP1527 control loop to be optimized over wide variety of input voltage, output voltage and load current conditions.

The MP1527 is offered in a tiny 4mm x 4mm 16 lead QFN and 14 lead TSSOP packages.

## Features

- 2A Peak Current Limit
- Internal 150mΩ Power Switch
- $V_{IN}$ Range of 2.6V to 25V
- >93% Efficiency
- Zero Current Shutdown Mode
- Under Voltage Lockout Protection
- Timer-Latch Fault Detection
- Soft Start Operation
- Thermal Shutdown
- Tiny 4mm x 4mm 16 pin QFN Package
- **Evaluation Board Available**

## Applications

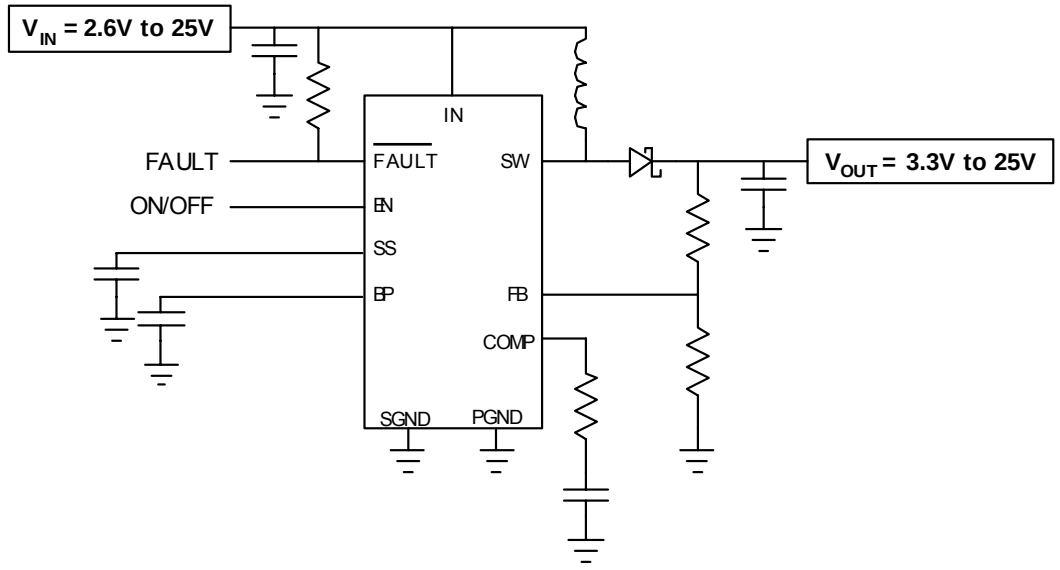
- SOHO Routers, PCMCIA Cards, Mini PCI
- Handheld Computers, PDAs
- Cell Phones, Digital and Video Cameras
- Small LCD Display

## Ordering Information

| Part Number | Package | Temperature |
|---|---|---|
| MP1527DR | QFN16 (4x4) | -40° to +85°C |
| MP1527DM | TSSOP14 | -40° to +85°C |
| EV0034 | MP1527DR Evaluation Board | |

* For Tape & Reel, add suffix –Z (e.g. MP1527DR–Z)
For Lead Free, add suffix –LF (e.g. MP1527DR–LF–Z)

## Figure 1: Typical Application Circuit



## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Input Supply Voltage $V_{IN}$ | -0.3V to 27V |
| SW Pin Voltage $V_{SW}$ | -0.3V to 27V |
| Voltage at All Other Pins | -0.3V to 6V |
| Storage Temperature | -55°C to +150°C |

## Recommended Operating Conditions

| | |
|---|---|
| IN Input Supply Voltage $V_{IN}$ | 2.6V to 25V |
| Step Up Output Voltage | 3.3V to 25V |
| Operating Temperature | -40°C to +85°C |

## Package Thermal Characteristics

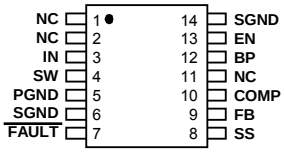
| | |
|---|---|
| Thermal Resistance $\Theta_{JA}$ (TSSOP14) | 90°C/W |
| Thermal Resistance $\Theta_{JA}$ (QFN16) (Note 2) | 46°C/W |

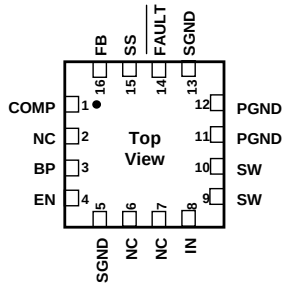
## Electrical Characteristics ($V_{IN}$ = 5.0V, $T_A$ = 25°C unless specified otherwise)

| Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| IN Shutdown Supply Current | $V_{EN}$≤0.3V | | 0.5 | 1.0 | μA |
| IN Operating Supply Current | $V_{EN}$>2V, $V_{FB}$=1.1V | | 0.9 | 1.2 | mA |
| BP Output Voltage | $V_{IN}$ = 2.6V to 25V | | 2.4 | | V |
| IN Undervoltage Lockout Threshold | $V_{IN}$ Rising | 2.1 | | 2.4 | V |
| IN Undervoltage Lockout Hysteresis | | | 100 | | mV |
| EN Input Low Voltage | | | | 0.3 | V |
| EN Input High Voltage | | 1.5 | | | V |
| EN Input Hysteresis | | | 100 | | mV |
| EN Input Bias Current | | | 100 | | nA |
| SW Switching Frequency | | 1.0 | 1.3 | 1.5 | MHz |
| SW Maximum Duty Cycle | $V_{FB}$ = 1.1V | 85 | 90 | | % |
| Error Amplifier Voltage Gain | | | 400 | | V/V |
| Error Amplifier Transconductance | | | 300 | | μA/V |
| COMP Maximum Output Current | Sourcing and Sinking | | 30 | | μA |
| FB Regulation Threshold | | 1.196 | 1.22 | 1.244 | V |
| FB Input Bias Current | $V_{FB}$=1.22V | | -100 | | nA |
| SS Charging Current | During Soft-Start | | 2 | | μA |
| $\overline{\text{FAULT}}$ Input Threshold Voltage | | | 1.2 | | V |
| $\overline{\text{FAULT}}$ Output Low Voltage | $V_{FB}$ < 1.0V | | 0.2 | | V |
| SW On Resistance | $V_{IN}$ =5V | | 150 | | mΩ |
| | $V_{IN}$ =3V | | 225 | | mΩ |
| SW Current Limit | (Note 3) | 2.0 | 3.0 | | A |
| SW Leakage Current | $V_{SW}$ = 25V | | 0.5 | | μA |
| Thermal Shutdown | | | 160 | | °C |

Note 1: Exceeding these ratings may damage the device.
Note 2: Measured on approximately 1" square of 1oz copper.
Note 3: Guaranteed by design. Not tested.

## Pin Descriptions




### Table 1: Pin Description

| QFN Pin | TSSOP Pin | Name | Function |
|---|---|---|---|
| 1 | 10 | COMP | Compensation Node. COMP is the output of the internal transconductance error amplifier. Connect a series RC network from COMP to SGND to compensate the regulator control loop. |
| 2, 6, 7 | 1, 2, 11 | NC | No Connect |
| 3 | 12 | BP | Output of the internal 2.4V low dropout regulator. Connect a 10nF bypass capacitor between BP and SGND. Do not apply an external load to BP. |
| 4 | 13 | EN | Regulator On/Off Control Input. A logic high input ($V_{EN}$>1.5V) turns on the regulator, a logic low puts the MP1527 into low current shutdown mode. |
| 5, 13 | 6, 14 | SGND | Signal Ground |
| 8 | 3 | IN | Input Supply |
| 9, 10 | 4 | SW | Output Switching Node. SW is the drain of the internal n-channel MOSFET. Connect the inductor and rectifier to SW to complete the step-up converter. |
| 11, 12 | 5 | PGND | Power Ground |
| 14 | 7 | $\overline{\text{FAULT}}$ | Fault Input/Output. $\overline{\text{FAULT}}$ is an Input/Output that indicates that the MP1527 detected a fault and shuts the regulator off once a fault is indicated. Connect the $\overline{\text{FAULT}}$ input/outputs together for all MP1527 regulators to force all regulators off when any one regulator detects a fault. Once a fault is detected, cycle EN or the input power to restart the regulator. Pull $\overline{\text{FAULT}}$ to the input voltage through a 100kΩ resistor. Up to 20 $\overline{\text{FAULT}}$ input/outputs can be connected in parallel. |
| 15 | 8 | SS | Soft-Start Input. Connect a 10nF to 22nF capacitor from SS to SGND to set the soft-start and fault timer periods. SS sources 2μA to an external soft-start capacitor during start-up and when a fault is detected. As the voltage at SS increases to 1.2V, the voltage at COMP is clamped to 0.7V above the voltage at SS limiting the startup current. Under a fault condition, SS ramps at the same rate as in soft-start. When the voltage at SS reaches 1.2V, $\overline{\text{FAULT}}$ is asserted and the regulator is disabled. The external capacitor at SS is discharged to ground when not in use or when under voltage lockout or thermal shutdown occurs. |
| 16 | 9 | FB | Regulation Feedback Input. Connect to external resistive voltage divider from the output voltage to FB to set output voltage. |

## Typical Operating Characteristics (Circuit of Figure 9: Unless Otherwise Specified)

**Figure 2: MP1527 responding to $\overline{FAULT}$ being driven low**

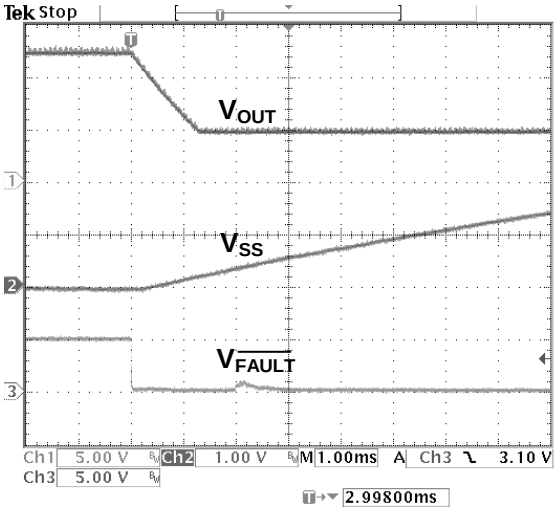



**Figure 3: MP1527 responding to an overload**

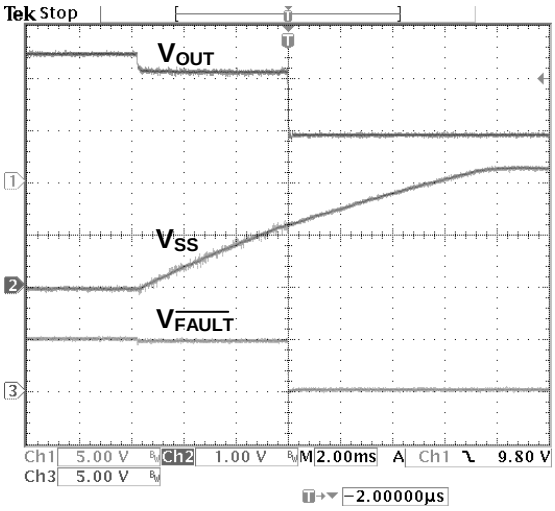



**Figure 4: MP1527 starting from EN being driven low-to-high**

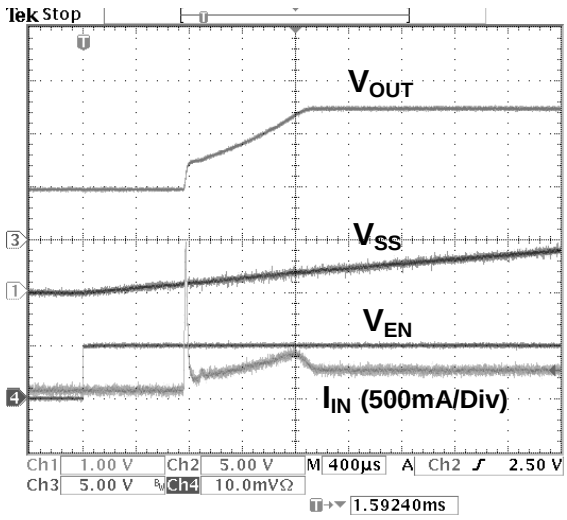



**Figure 5: Transient Load Response. Load driven from 50mA to 500mA**

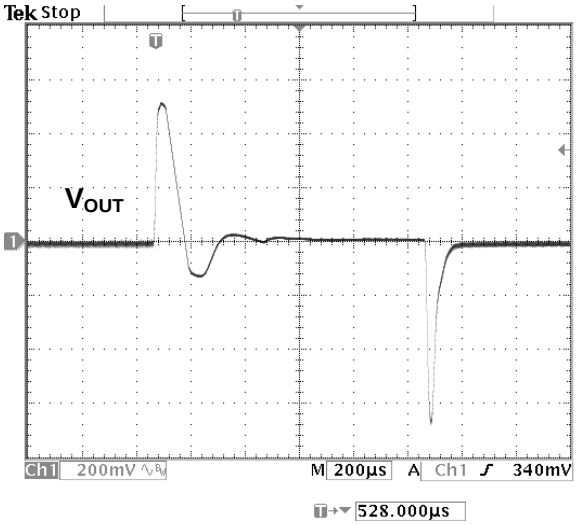


**Figure 6: Quiescent Current versus Input Voltage (Bootstrapped)**

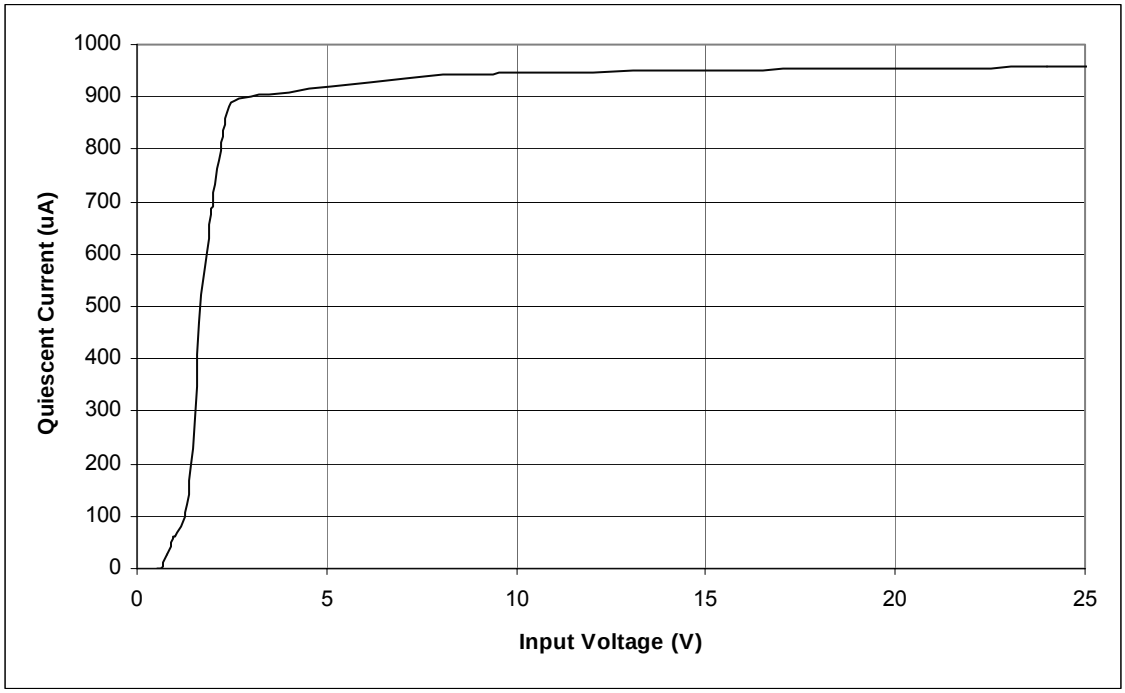



**Figure 7: Efficiency vs. Load Current (Bootstrapped)**

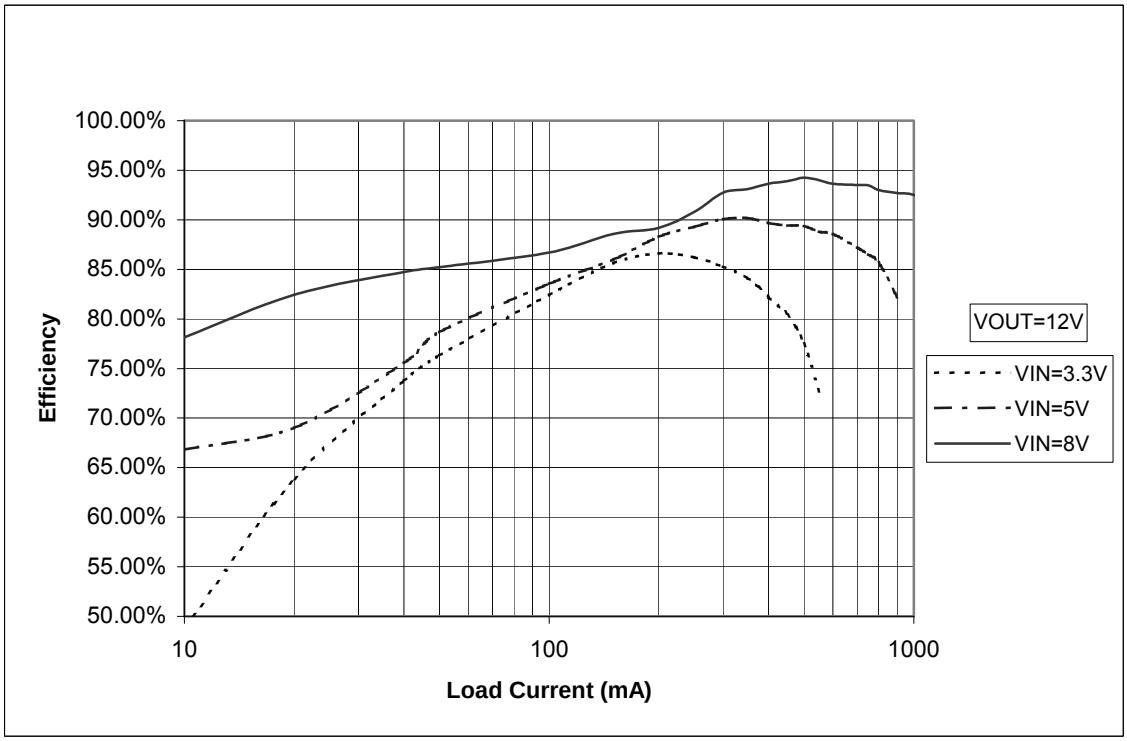


**Figure 8: Efficiency vs. Load Current (Non-Bootstrapped)**

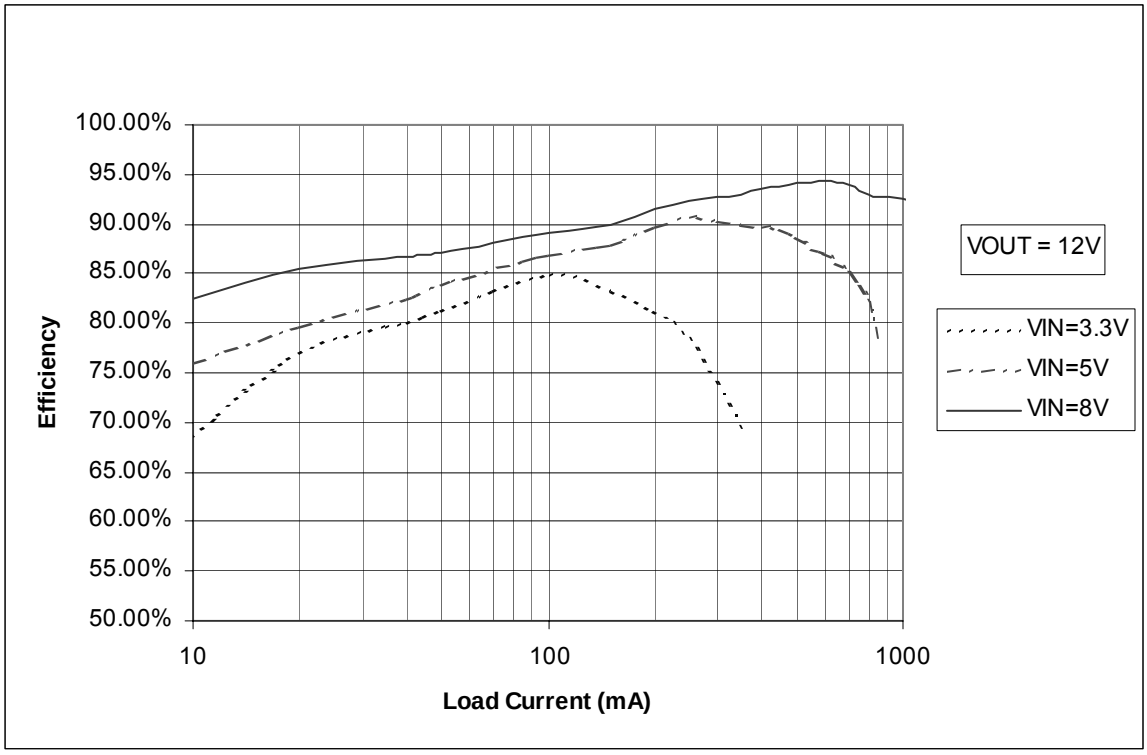



**Figure 9: $V_{IN}$ = 5V, $V_{OUT}$ = 12V @ 500mA Load**

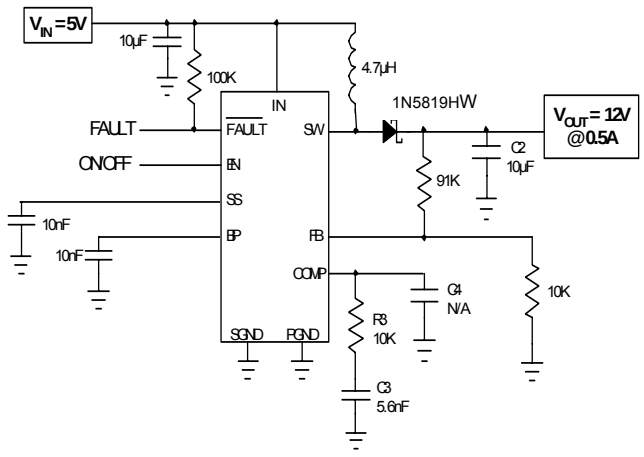



**Figure 10: Driving Multiple Strings of White LEDs**

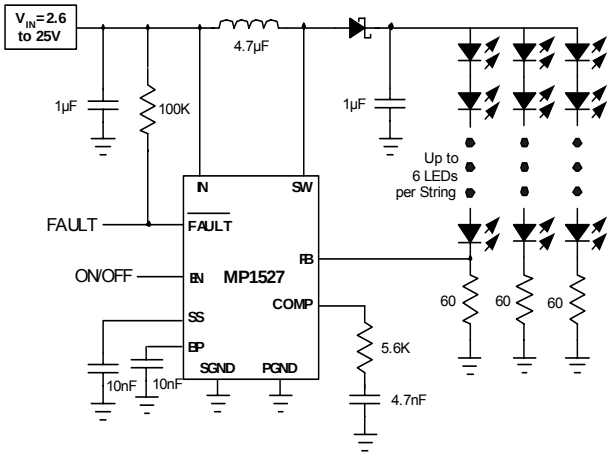
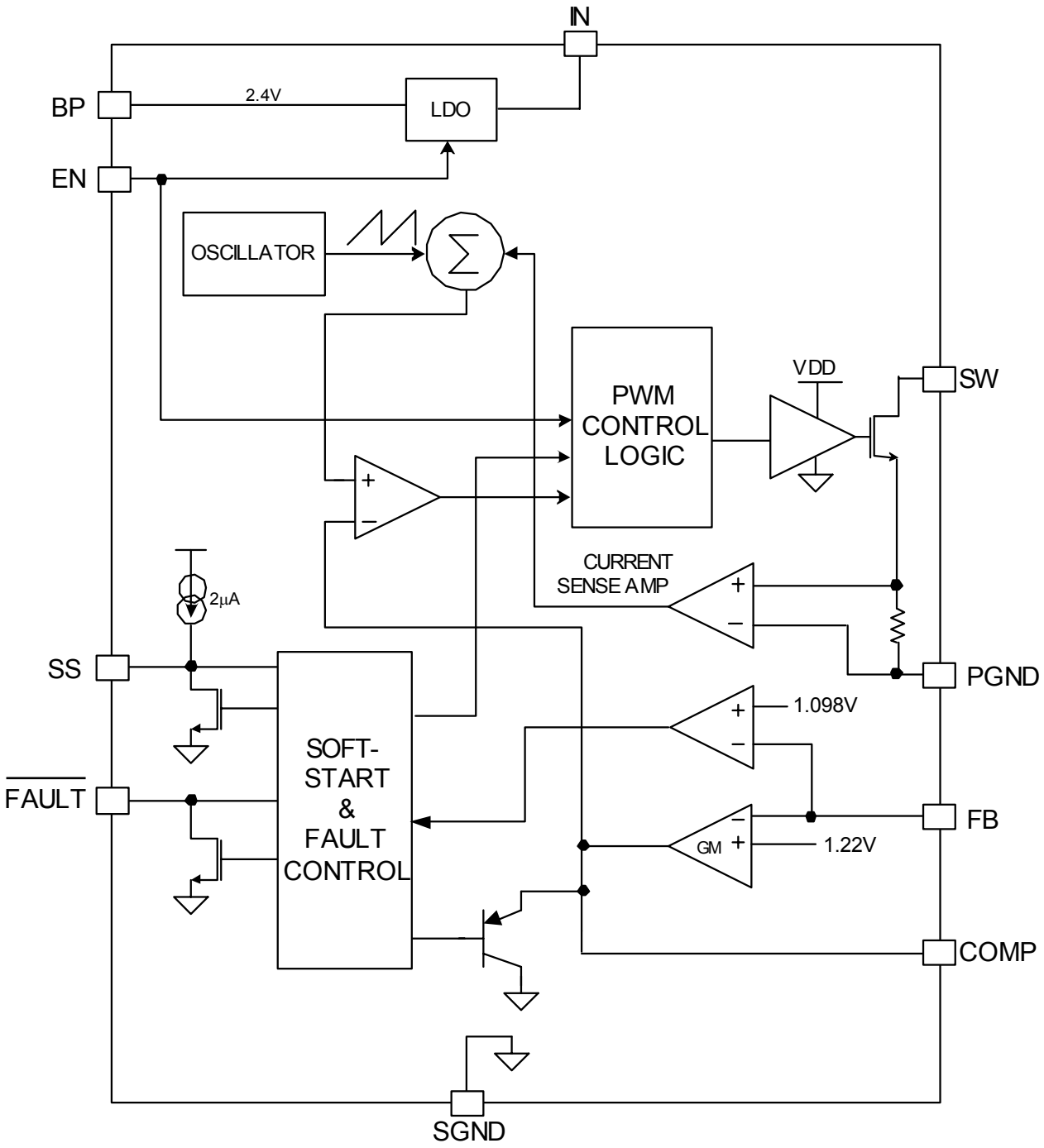


**Figure 11: Functional Block Diagram**



## Functional Description

The MP1527 uses a 1.3MHz fixed-frequency, current-mode regulation architecture to regulate the output voltage. The MP1527 measures the output voltage through an external resistive voltage divider and compares that to the internal 1.22V reference to generate the error voltage at COMP. The current-mode regulator compares voltage at the COMP pin to the inductor current to regulate the output voltage. The use of current-mode regulation improves transient response and control loop stability.

At the beginning of each cycle, the n-channel MOSFET switch is turned on, forcing the inductor current to rise. The current at the source of the switch is internally measured and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage at COMP. When the inductor current rises sufficiently, the PWM comparator turns off the switch forcing the inductor current to the output capacitor through the external rectifier. This forces the inductor current to decrease. The peak inductor current is controlled by the voltage at COMP, which in turn is controlled by the output voltage. Thus the output voltage controls the inductor current to satisfy the load.

### Internal Low-Dropout Regulator

The internal power to the MP1527 is supplied from the input voltage (IN) through an internal 2.4V low-dropout linear regulator, whose output is BP. Bypass BP to SGND with a 10nF or greater capacitor to insure the MP1527 operates properly. The internal regulator can not supply any more current than is required to operate the MP1527, therefore do not apply any external load to BP.

### Soft-Start

The MP1527 includes a soft-start timer that limits the voltage at COMP during start-up to prevent excessive current at the input. This prevents premature termination of the source voltage at startup due to input current overshoot at startup. When power is applied to the MP1527, or with power applied when enable is asserted, a 2μA internal current source charges the external capacitor at SS. As the capacitor charges, the voltage at SS rises. The MP1527 internally clamps the voltage at COMP to 0.7V above the voltage at SS. This limits the inductor current at start-up, forcing the input current to rise slowly to the current required to regulate the output voltage during soft-start.

The soft-start period is determined by the equation:

$$t_{SS} = 2.75 * 10^5 * C_{SS}$$

Where $C_{SS}$ (in F) is the soft-start capacitor from SS to SGND, and $t_{SS}$ (in seconds) is the soft-start period.

Determine the capacitor required for a given soft-start period by the equation:

$$C_{SS} = 3.64 * 10^{-6} * t_{SS}$$

Use values for $C_{SS}$ between 10nF and 22nF to set the soft-start period.

### Fault Timer-Latch Function

The MP1527 includes an output fault detector and timer-latch circuitry to disable the regulator in the event of an undervoltage, overcurrent, or thermal overload. Once the soft-start is complete, the fault comparator monitors the voltage at FB. If the voltage falls below the 1.098V fault threshold, the capacitor at SS charges through an internal 2μA current source. If the fault condition remains long enough for the capacitor at SS to charge to 1.2V, the $\overline{\text{FAULT}}$ output is pulled low and the power switch is turned off, disabling the output.

The fault time-out period is determined by the equation:

$$t_{FAULT} = 6*10^5 * C_{SS}$$

If multiple MP1527 regulators are used in the same circuit, the $\overline{FAULT}$ input/outputs can be connected together. Should any one regulator indicate a fault, it pulls all FAULT input/outputs low, disabling all regulators. This insures that all outputs are disabled should any one output detect a fault. Pull-up $\overline{FAULT}$ to the input voltage (IN) through a 100KΩ resistor. The leakage current at $\overline{FAULT}$ is less than 250nA, so up to 20 $\overline{FAULT}$ input/outputs can be connected together through a single 100KΩ pull-up resistor. To reduce current draw when $\overline{FAULT}$ is active, a higher value pull-up resistor may be used. Calculate the pull-up resistor value by the equation:

$$100k\Omega \le R_{PULL-UP} \le 2M\Omega / N$$

Where N is the number of $\overline{FAULT}$ input/outputs connected together.

## Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 1.22V feedback threshold voltage. Use 10KΩ for the low-side resistor of the voltage divider. Determine the high side resistor by the equation:

$$R_H = (V_{OUT} - V_{FB}) / (V_{FB} / R_L)$$

where $R_H$ is the high-side resistor, $R_L$ is the low-side resistor, $V_{OUT}$ is the output voltage and $V_{FB}$ is the feedback regulation threshold.

For $R_L$ = 10KΩ and $V_{FB}$ = 1.22V, then

$$R_H (K\Omega) = 8.20* (V_{OUT} – 1.22V)$$

## Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Use an input capacitor value greater than 4.7µF. The capacitor can be electrolytic, tantalum or ceramic. However since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with RMS current rating greater than the inductor ripple current (see Selecting The Inductor to determine the inductor ripple current).

To insure stable operation place the input capacitor as close to the IC as possible. Alternately a smaller high quality ceramic 0.1µF capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP1527.

## Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristic of the output capacitor also affects the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \approx \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{LOAD}}{C2 \times f_{SW}}$$

Where $V_{RIPPLE}$ is the output ripple voltage, $V_{IN}$ and $V_{OUT}$ are the DC input and output voltages respectively, $I_{LOAD}$ is the load current, $f_{SW}$ is the switching frequency, and C2 is the capacitance of the output capacitor.

In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance

at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} \approx \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C2\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}}$$

Where $R_{ESR}$ is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. A 4.7µF-22µF ceramic capacitor is suitable for most applications.

## Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal n-channel switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

A 4.7µH inductor is recommended for most applications. However, a more exact inductance value can be calculated. A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent loss of regulation due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions. Calculate the required inductance value by the equation:

$$L = \frac{V_{IN}\times(V_{OUT} - V_{IN})}{V_{OUT}\times f_{SW}\times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT}\times I_{LOAD(MAX)}}{V_{IN}\times \eta}$$

$$\Delta I = (30\% - 50\%) I_{IN(MAX)}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, and η is efficiency.

## Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. To reduce losses due to diode forward voltage and recovery time, use a Schottky diode with the MP1527. The diode should be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current.

## Compensation

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are $f_{P1}$ set by the output capacitor and load resistance and $f_{P2}$ set by the compensation capacitor C3. The zero $f_{Z1}$ is set by the compensation capacitor C3 and the compensation resistor R3. These are determined by the equations:

$$f_{P1} = 1 / (\pi * C2 * R_{LOAD})$$

$$f_{P2} = G_{EA} / (2\pi * A_{VEA} * C3)$$

$$f_{Z1} = 1 / (2\pi * C3 * R3)$$

Where $R_{LOAD}$ is the load resistance, $G_{EA}$ is the error amplifier transconductance, and $A_{VEA}$ is the error amplifier voltage gain.

The DC loop gain is:

$$A_{VDC} = A_{VEA} * G_{CS} * (V_{IN} / V_{OUT}) * R_{LOAD} * (V_{FB} / V_{OUT})$$

or

$$A_{VDC} = A_{VEA} * G_{CS} * V_{IN} * V_{FB} * R_{LOAD} / (V_{OUT})^2$$

Where $G_{CS}$ is the current sense gain, $V_{IN}$ is the input voltage, $V_{FB}$ is the feedback regulation threshold, and $V_{OUT}$ is the regulated output voltage.

There is also a right-half-plane zero ($f_{RHPZ}$) that exists in all continuous mode (continuous mode means that the inductor current does not drop to zero on each cycle) step-up converters. The frequency of the right half plane zero is:

$$f_{RHPZ} = V_{IN}^2 * R_{LOAD} / (2\pi * L * V_{OUT}^2)$$

where L is the value of the inductor.

To stabilize the regulation control loop, the crossover frequency (The frequency where the loop gain drop to 0dB or gain of 1, indicated as $f_C$) should be at least one decade below the right-half-plane zero and should be at most 75KHz. $f_{RHPZ}$ is at its lowest frequency at maximum output load current ($R_{LOAD}$ is at a minimum)

The crossover frequency is calculated by the equation:

$$f_C = A_{VDC} * f_{P1} * f_{P2} / f_{Z1}$$

or

$$f_C = G_{CS} * G_{EA} * V_{IN} * V_{FB} * R3 / (2\pi * C2 * V_{OUT}^2)$$

The known values are:

$G_{CS}$ = 4.3S
$G_{EA}$ = 400μS
$V_{FB}$ = 1.22V

Putting in the known constants:

$$f_C = 3.3x10^{-4} * V_{IN} * R3 / (C2 * V_{OUT}^2)$$

If the frequency of the right-half-pane zero $f_{RHPZ}$ is less than 750KHz, then the crossover frequency should be 1/10 of $f_{RHPZ}$, and determine the compensation resistor (R3) with equation (1). If $f_{RHPZ}$ is greater than or equal to 750KHz, set the crossover frequency to 75KHz with equation (2).

For $f_C = f_{RHPZ} / 10$, then

$$R3 = V_{IN} * R_{LOAD-MIN} * C2 / (10 G_{CS} * G_{EA} * V_{FB} * L)$$

The minimum load resistance ($R_{LOAD-MIN}$) is equal to the regulated output voltage ($V_{OUT}$) divided by the maximum load current $I_{LOAD-MAX}$. Substituting that into the above equation:

$$R3 = V_{IN} * V_{OUT} * C2 / (10 G_{CS} * G_{EA} * V_{FB} * L * I_{LOAD-MAX})$$

Putting in the known constant values:

$$(1)\ R3 \approx 48 * V_{IN} * V_{OUT} * C2 / (L * I_{LOAD-MAX})$$

For $f_C$ = 75KHz,

$$f_C = (G_{CS} * G_{EA} * V_{IN} * V_{FB} * R3) / (2\pi * C2 * V_{OUT}^2)$$

Solving for R3,

$$R3 = (2\pi * f_C * C2 * V_{OUT}^2 / (G_{CS} * G_{EA} * V_{IN} * V_{FB})$$

Using 75KHz for $f_C$ and putting in the other known constants:

$$(2)\ R3 \approx 2.2x10^8 * C2 * V_{OUT}^2 / V_{IN}$$

The value of the compensation resistor is limited to 10KΩ to prevent overshoot on the output at turn-on. So if the value calculated for R3 from either equation (1) or equation (2) is greater than 10kΩ, use 10KΩ for R3.

Choose C3 to set the zero frequency $f_{Z1}$ to one-fourth of the crossover frequency $f_C$:

$$f_{Z1} = f_C / 4$$

or

$$1 / (2\pi * C3 * R3) = G_{CS} * G_{EA} * V_{IN} * V_{FB} * R3 / (8\pi * C2 * V_{OUT}^2)$$

Solving for C3:

$$C3 = 4 * C2 * V_{OUT}^2 / (G_{CS} * G_{EA} * V_{IN} * V_{FB} * R3^2)$$

Entering the known values gives:

$$C3 \approx 1.9x10^3\ C2\ V_{OUT}^2 / (V_{IN}\ R3^2)$$

In some cases, if an output capacitor with high capacitance and high equivalent series resistance (ESR) is used, then a second compensation capacitor (from COMP to SGND) is required to compensate for the zero introduced by the output capacitor ESR. The extra capacitor is required if the ESR zero is less than 4x the crossover frequency. The ESR zero frequency is:

$$f_{ZESR} = 1 / (2\pi*C2*R_{ESR})$$

The second compensation capacitor is required if:

$$4*f_C \geq f_{ZESR}$$

or

$$4*G_{CS}*G_{EA}*V_{IN}*V_{FB}*R3 / (2\pi*C2*V_{OUT}^2) \geq 1 / (2\pi*C2*R_{ESR})$$

Simplifying:

$$(8.4x10^{-3}*V_{IN}*R3*R_{ESR}) / V_{OUT}^2 \geq 1$$

If this is the case, calculate the second compensation capacitor by the equation:

$$R3*C4 = C2*R_{ESR}$$

or

$$C4 = (C2*R_{ESR}) / R3$$

**Example**

Given:
Input Voltage ($V_{IN}$): 5V
Output Voltage ($V_{OUT}$): 12V
Maximum Load Current ($I_{LOAD-MAX}$): 500mA
Output Capacitor (C2): 10µF (ESR=10mΩ Maximum)
Inductor Value (L): 4.7µH

Find the frequency of the right-half-plane zero:

$f_{RHPZ} = V_{IN}^2 / (2\pi*L*V_{OUT}*I_{LOAD-MAX})$
$f_{RHPZ} = (5V)^2 /$
$(2\pi*4.7\mu H*12V*500mA)=141KHz$

The frequency of the right-half-plane zero is less than 750khz, so use equation (1) to determine the compensation resistor R3:

$$R3 \approx 48*V_{IN}*V_{OUT}*C2 / (L*I_{LOAD-MAX})$$

$$R3 \approx 48*5*12*10\mu F/(4.7\mu H*500mA) = 12.3K\Omega$$

(use 10KΩ)

Find the compensation capacitor C3:

$$C3 \approx 1.9x10^3*C2*V_{OUT}^2 / (V_{IN}*R3^2)$$

$$C3 \approx 1.9x10^3*10\mu F\ (12V)^2 / (5 * 10K\Omega^2) = 5.4nF$$

(use the nearest standard value, 5.6nF)

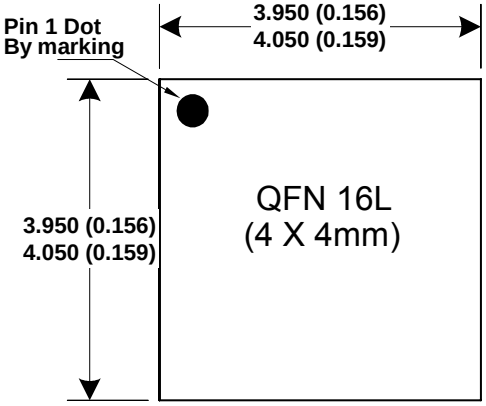
Determine if the second compensation capacitor is required:

$$8.4x10^{-3} * 5V * 5.6K\Omega * 10m\Omega / 12V^2 = 0.016 \leq 1$$

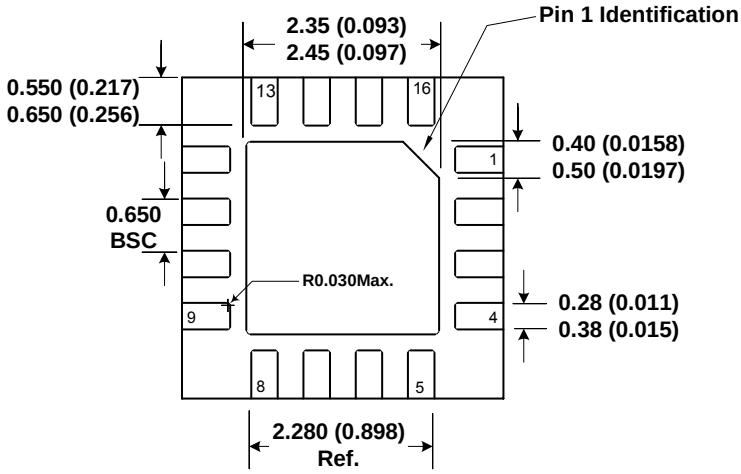
Therefore no second compensation capacitor is required.

## Packaging

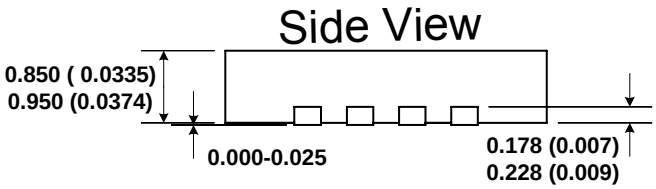
### QFN16 (4x4)



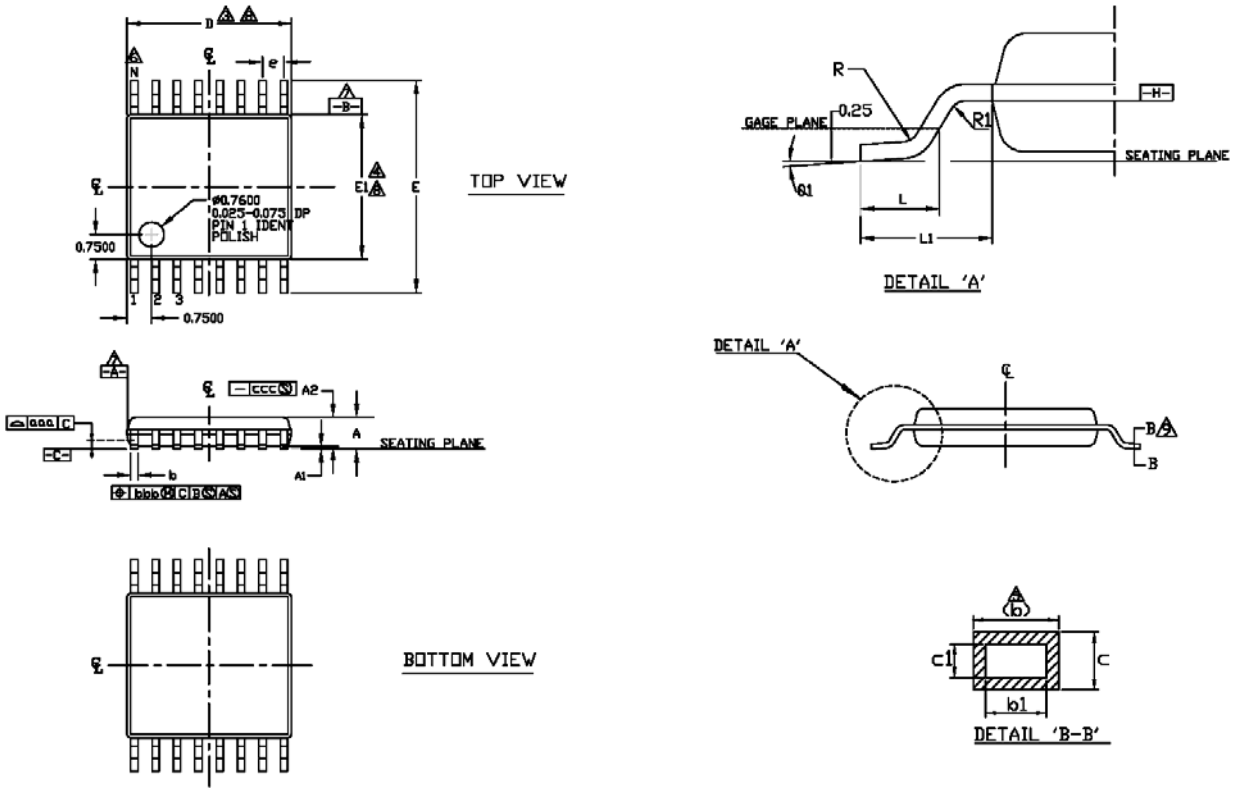

Top View




Btm View



## TSSOP14




| SYMBOL | 14L TSSOP | | |
|---|---|---|---|
| | MIN | NOM. | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| D | 4.9 | 5.0 | 5.1 |
| E1 | 4.3 | 4.4 | 4.5 |
| E | 6.2 | 6.4 | 6.6 |
| L | 0.45 | 0.60 | 0.75 |
| R | 0.09 | — | — |
| R1 | 0.09 | — | — |
| b | 0.19 | — | 0.30 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.09 | — | 0.20 |
| c1 | 0.09 | — | 0.16 |
| θ1 | 0° | — | 8° |
| L1 | 1.0 REF | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.05 | | |
| ddd | 0.20 | | |
| e | 0.65 BSC | | |
| N | 14 | | |
| Ref. | Jedec MO-153 Issue C Variation AB-1 | | |

## Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONNING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH ,PROTUSIONS OR GATE BURRS.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERNAL FLASH OR PROTUSION.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.
6. "N" IS THE MAXIMUM NUMBER OF LEAD TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
8. DIMENSIONS 'D' AND 'E1' ARE TO BE DETERMINED AT DATUM PLANE -H-
9. CROSS SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.
10. REFER TO JEDEC MO-153 ISSUE C.