Texas Instruments

Quad Channel (Half X4 Lane) PCIe Redriver/Equalizer

Check for Samples: SN65LVPE504

FEATURES

- **4 Identical Channel PCIe Equalizer/Redriver**
- **Support for Both PCIe Gen I (2.5Gbps) and Gen II (5.0 Gbps) Speed**
- **Selectable Equalization, De-emphasis, and Output Swing**
- **Per Channel Receive Detect (Lane Detection)**
- **Selectable Receiver Electrical Idle Threshold Control**
- **Low Operating Power Modes**
  - **Supports Three Low-Power Modes to Enable up to 80% Lower Operating Power**
- **Excellent Jitter and Loss Compensation Capability to 50" of 4-mil SL on FR4**
- **Small Foot Print – 42 Pin 9 × 3.5 TQFN Package**
- **High Protection Against ESD Transient**
  - **HBM: 6,000 V**
  - **CDM: 1,000 V**
  - **MM: 200 V**

APPLICATIONS

- **PC MB, Docking Station, Server, Communication Platform, Backplane and Cabled Application**

DESCRIPTION

The SN65LVPE504 is a quad channel, half four lane PCIe redriver and signal conditioner supporting data rates of up to 5.0Gbps. The device complies with PCIe spec revision 2.1, supporting electrical idle and power management modes.

Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE504 is designed to minimize the signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion PCIe signal will experience. Both equalization and de-emphasis levels for all 4 channels are controlled by the setting of signal control pins EQ, DE and OS.

See Table 1 for EQ, DE and OS setting details.

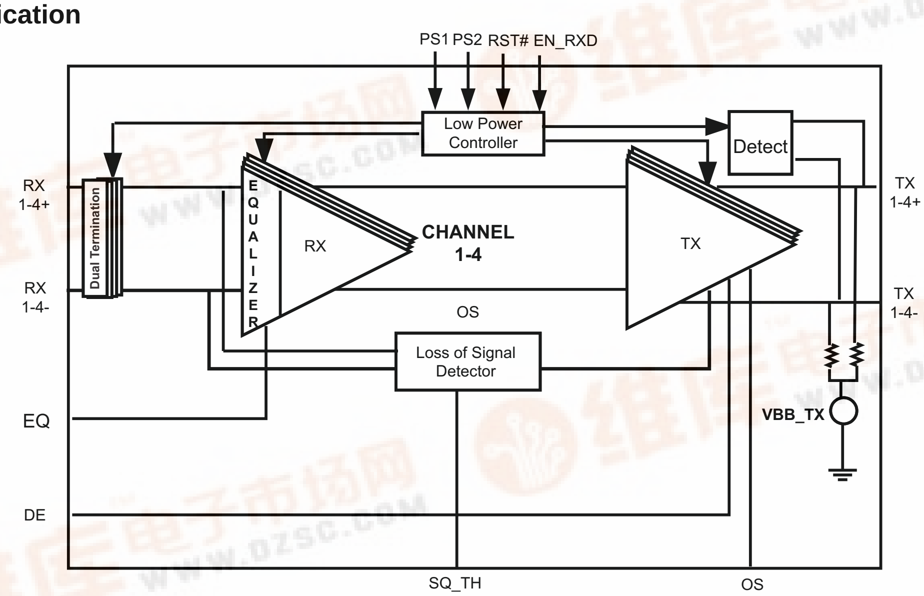


Figure 1. Data Flow Block Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DEVICE OPERATION

Device PowerOn

Device initiates internal power-on reset after Vcc has stabilized. External reset can also be applied at anytime by toggling $\overline{RST}$ pin. External reset is recommended after every device power-up. After 50µs (MAX) from the application of $\overline{RST}$, device samples the state of EN_RXD, if it is set H device will enter Rx.Detect state where each of the four channels will perform Rx.Detect function (as described in PCIe spec). If EN_RXD is set L, automatic RX detect function is disabled and all channels are enabled with their termination set to Z_{RX_DC}.

Receiver Detection

While EN_RXD pin is H and device is not in reset state ($\overline{RST}$ is H), LVPE504 performs RX.Detect on all its 4 channels indefinitely until remote termination is detected on at least one channel. When termination is detected on ≥ 1 CH, RX.Detect cycle is limited to 5 more tries on the other channels. At the end of 5^{th} try those channels which failed to detect remote termination will be turned off to save power and their Rx termination is set to $Z_{RX\text{-}HIGH}$. In the event device detects only three channels, all four channels are enabled.

Automatic Rx detection feature on all four channels can be forced off by driving EN_RXD low. In this state all four channels input termination are set to Z_{RX_DC}.

Standby Mode

This is low power state triggered by $\overline{RST}$ = L. In standby mode receiver termination resistor for each of the four channels is switched to $Z_{RX\text{-}HIGH}$ of >50 kΩ and transmitters are pulled to Hi-Z state. Device power is reduced to <10mW (TYP). To get device out of standby mode $\overline{RST}$ is toggled L-H.

Electrical Idle Support

A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. LVPE504 detects an electrical idle state when RX± input voltage of the associated channel falls below V_{EID_TH} min and stays in this state for at least 20ns. After detection of an electrical idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds V_{EID_TH} max, normal operation is restored and output start passing input signal. Electrical idle exit and entry time is specified at < 8 ns (MAX).

Electrical idle support is independent for each channel, however to lower active power it is possible to slave electrical idle function from channel 1 to CH2-CH4. This mode is selected by driving PS2 to H.

Power Save Features

Device supports three power save modes as below:

1. Standby Mode

   This mode can be enabled from any state (Rx detect or active) by driving $\overline{RST}$ L. In this state all 4 channels have their termination set to $Z_{RX\text{-}HIGH}$ and outputs are at Hi-Z. Device power is 10mW (MAX).

2. Auto Low Power Mode

   This mode is enabled when PS1 pin is tied H and device has been in active mode, i.e., past Rx detect state for >250ms (TYP). In this mode anytime $Vin_{diff\_p\text{-}p}$ falls below selected V_{EID_TH} for a *given channel* and stays below V_{EID_TH} for >1µs, the associated CH enters auto low power (ALP) mode where power/CH is reduced by >80% of normal operating power/CH. A CH will exit ALP mode whenever $Vin_{diff\_p\text{-}p}$ exceeds max V_{EID_TH} for that channel. Exit latency from ALP state is 30ns max. To use this mode link latency will need to account for the ALP exit time for N_FTS. ALP mode is handled by each channel independently based on its input differential signal level, unless slave mode is activated (PS2=H) when CH1 controls SQ detect of other channels based on its signal level.

3. Slave Power Mode

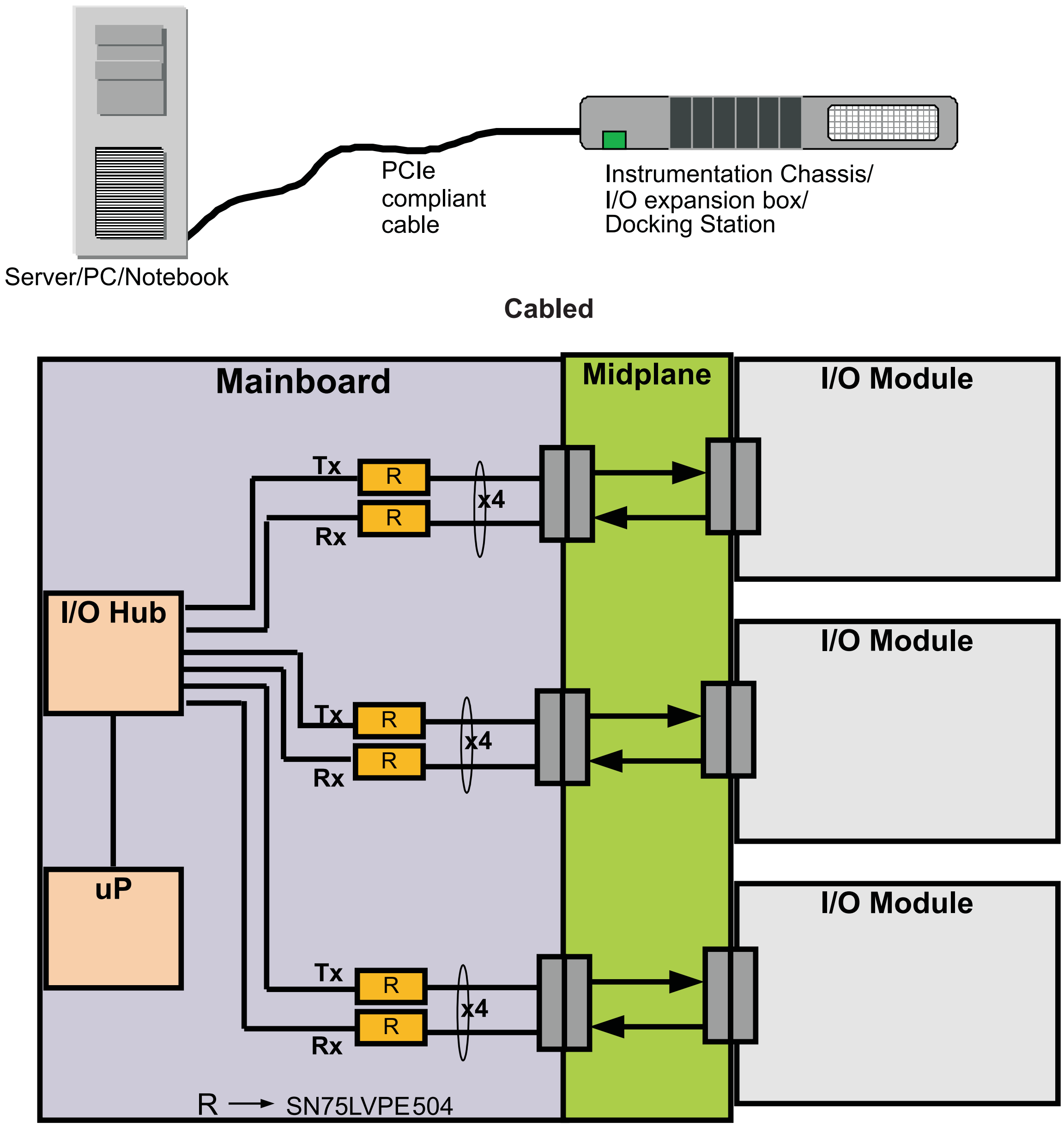
   This mode is activated by driving PS2 high. Under normal operation squelch detection is handled by each channel independently. In slave mode SQ detection for CH2, CH3 and CH4 are turned off and squelch function is slaved to that of CH1. By turning off squelch detection circuitry for three of the four channels device saves power. To use this feature user must ensure all channels operate simultaneously

Squelch Control

Controls electrical idle detect threshold level. Three levels are supported as shown in Table 1.

Beacon Support

With its broadband design, the SN65LVPE504 supports low frequency Beacon signal (as defined by PCIe 2.1 spec) used to indicate wake-up event to the system by a downstream device when in L2 power state. All requirements for a beacon signal as specified in PCI Express specification 2.1 must be met for device to pass beacon signals.



Backplane

Figure 2. LVPE504 Typical Applications

DEVICE INFORMATION

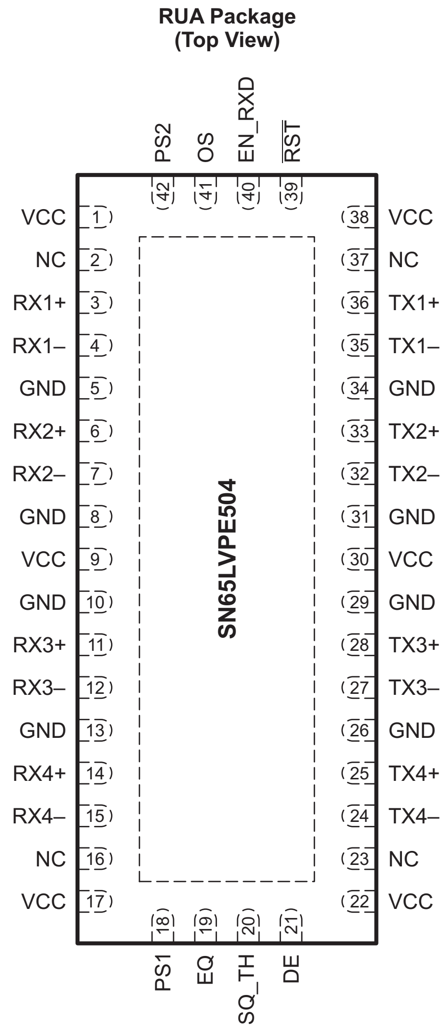


Figure 3. Flow-Through Pin-Out

PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O PINS			
3	RX1+	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 4. These pins are tied to an internal voltage bias by dual termination resistor circuit
4	RX1–		
6	RX2+		
7	RX2–		
11	RX3+		
12	RX3–		
14	RX4+		
15	RX4–		
36	TX1+	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 4. These pins are internally tied to voltage bias by termination resistors
35	TX1–		
33	TX2+		
32	TX2–		

PIN FUNCTIONS (continued)

PIN NO.	PIN NAME	I/O TYPE	DESCRIPTION
HIGH SPEED DIFFERENTIAL I/O PINS (continued)			
28	TX3+	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 4. These pins are internally tied to voltage bias by termination resistors
27	TX3–		
25	TX4+		
24	TX4–		
DEVICE CONTROL PIN			
40	EN_RXD	I, LVCMOS	Sets device operation modes per Table 1. Internally pulled to VCC
42	PS2	I, LVCMOS	Tying pin to VCC slaves CH2-4 electrical idle and Rx.Detect function to CH1. Internally pulled to GND
18	PS1	I, LVCMOS	Select auto-low power save mode per Table 1. Internally pulled to GND
20	SQ_TH (1)	I, LVCMOS	Squelch threshold level select pin for electrical idle detect per Table 1 Internally pulled to VCC/2
39	$\overline{RST}$	I, LVCMOS	Reset device, input active Low. Internally pulled to VCC
SIGNAL CONDITIONING PINS (1)			
21	DE	I, LVCMOS	Selects de-emphasis settings for CH 1-CH 4 per Table 1. Internally pulled to Vcc/2
19	EQ	I, LVCMOS	Selects equalization settings for CH 1-CH 4 per Table 1. Internally pulled to Vcc/2
41	OS	I, LVCMOS	Selects output amplitude for CH 1-CH 4 per Table 1. Internally pulled to Vcc/2
POWER PINS			
1,9,17,22,30,38	VCC	Power	Positive supply should be 3.3V ± 10%
5,8,10,13, 26,29,31,34û	GND	Power	Supply ground

(1) Internally biased to Vcc/2 with >200kΩ pull-up/pull-down. When 3-state pins are left as NC, board leakage at the pin pad must be < 1 µA otherwise drive to Vcc/2 to assert mid-level state.

Table 1. Control Pin Settings

OUTPUT SWING (CH1-CH4) at 5Gbps		SQUELCH THRESHOLD (CH1-CH4)	
OS	**TRANSITION BIT AMPLITUDE (TYP mVpp)**	**SQ_TH**	**MIN DIFFERENTIAL INPUT (CH1-CH4)**
0	800	0	47 mVpp
NC (***default***)	929	NC (***default***)	61 mVpp
1	1047	1	83 mVpp

OUTPUT DE-EMPHASIS (CH1-CH4) at 5Gbps				INPUT EQUALIZATION (CH1-CH4)	
DE	**OS = NC**	**OS = 0**	**OS = 1**	**EQ**	**Equalization dB (at 5Gbps)**
NC (***default***)	–3.4dB	–2.1dB	–4.6dB	0	0
0	–6.2dB	–4.9dB	–7.2dB	NC	7 (***default***)
1	–10.3dB	–9.2dB	–11dB	1	15

EN_RXD	DEVICE FUNCTION
0	Set input termination to Rx_DC
1	Perform Rx detect after power up

$\overline{RST}$	DEVICE FUNCTION
0	Device in standby state, inputs set to Hi-Z
1	Device in active mode

PS1	DEVICE FUNCTION
0	Auto-low power mode disabled (***default***)
1	Auto-low power mode enabled

PS2	DEVICE FUNCTION
0	Electrical Idle and Rx Detect independent for CH1-CH4 (***default***)
1	CH2-CH4 Electrical Idle and Rx Detect slaved to CH1

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN65LVPE504RUAR	LVPE504	42-pin RUA Reel (large)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to VCC + 0.5	V
Electrostatic discharge	Human body model(3)	±6000	V
	Charged-device model(4)	±1000	V
	Machine model(5)	±200	V
Continuous power dissipation		See Thermal Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC		SN65LVPE504 TQFN (42 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	12	
θ_{JB}	Junction-to-board thermal resistance	10	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	4.7	

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage	3	3.3	3.6	V
$C_{COUPLING}$	AC Coupling capacitor	75		200	nF
	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

under recommended operating conditions

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{CC}	Supply current	$\overline{RST}$, DEx, EQx, OS = NC, EN_RXD = NC, K28.5 pattern at 5 Gbps, VID = 1000mVp-p		174	190	mA
ICC_{Slave}		PS2 = Vcc; $\overline{RST}$, DEx, EQx, OS = NC, EN_RXD = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000mV_{p-p}		161	175	
ICC_{ALP}		When auto-low power conditions are met, PS1 = V_{CC}		27	32	
ICC_{ALP_Slave}		PS1, PS2 = VCC and link in EID state		14	18	
$ICC_{NO\_CONNECT}$		EN_RXD = 1 No termination detected on any CH		2.5		
ICC_{stdby}		$\overline{RST}$ = GND			0.1	
	Maximum data rate				5	Gbps
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input, Refer to Figure 7		1		µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity, Refer to Figure 7			30	ns
t_{ENB}	Device enable time	$\overline{RST}$ 0 → 1		5	50	µs
t_{DIS}	Device disable time	$\overline{RST}$ 1 → 0		0.1	2	µs
$T_{RX.Detect}$	Rx.Detect start event	EN_RXD = 1, Time to start Rx Detect after power up		6		µs
CONTROL LOGIC						
V_{IH}	High level Input Voltage		1.4		Vcc	V
V_{IL}	Low Level Input Voltage		–0.3		0.5	V
V_{HYS}	Input Hysteresis			150		mV
I_{IH}	High Level Input Current	OS, EQ, DE, SQ_TH, PS1, PS2 = V_{CC}			30	µA
		EN_RXD, $\overline{RST}$ = V_{CC}			1	
I_{IL}	Low Level Input Current	PS1, PS2 = GND	–1			µA
		OS, EQ, DE, SQ_TH, EN_RXD, $\overline{RST}$ = GND	–30			
RECEIVER AC/DC						
Vin_{diff_p-p}	RX1-RX4 Input voltage swing	AC coupled differential signal (5Gbps)	100		1200	mVp-p
T_{RX_TJ}	Max Rx total timing error	At device pin (5Gbps)			0.4	UI
T_{RX_DJ}	Max Rx deterministic timing error	At device pin (5Gbps)			0.3	UI
V_{CM_RX}	RX1-RX4 Common mode voltage		0		3.6	V
Vin_{COM_P}	RX1-RX4 AC peak common mode voltage				150	mVP
Z_{RX_DC}	DC single ended impedance		40	55	60	Ω
Z_{RX_Diff}	DC Differential input impedance		80	98	120	Ω
Z_{RX_High}	DC Input high impedance	Device in standby mode. Rx termination not powered measured with respect to GND over 200 mV max	50	75		kΩ
V_{EID_TH}	Electrical idle detect threshold	Measured at receiver pin: SQ_TH = NC		61		mVpp
		SQ_TH = 1	58	83	107	
		SQ_TH = 0		47		
$RL_{RX-DIFF}$	Differential return loss	50 MHz – 1.25 GHz	10	15		dB
		1.25 GHz – 2.5 GHz	8	11		
RL_{RX-CM}	Common mode return loss	50 MHz – 2.5 GHz	9	14		dB

ELECTRICAL CHARACTERISTICS (continued)

under recommended operating conditions

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER AC/DC						
V_{TXDIFF_P-P}	Differential peak-to-peak output voltage	RL = 100Ω ±1%, OS = NC, transition Bit	866	929	1031	mV
		RL = 100Ω ±1%, OS = GND transition Bit		800		
		RL = 100Ω ±1% OS = VCC transition Bit		1047		
		RL = 100Ω ±1%, DE=NC, OS = 0,1,NC on-transition bit		620		
		RL = 100Ω ±1%, DE=OS = 0,1,NC on-transition bit		456		
		RL = 100Ω ±1%, DE=OS = 0,1,NC on-transition bit		288		
	De-emphasis level	OS = NC (Figure 9) for OS = 1 and NC see Table 1)	–3.0	–3.4	–4.0	dB
			–5.5	–6.2	–6.5	
			–9.0	–10.3	–10.6	
T_{DE}	De-emphasis width	At 5 Gbps		0.9		UI
Z_{TX_diff}	DC Differential impedance	Defined during signaling	80	100	120	Ω
RL_{diff_TX}	Differential return loss	f = 50 MHz – 1.25 GHz	10	20		dB
		f = 1.25 GHz – 2.5 GHz	8	13		
RL_{CM_TX}	Common mode return loss	f = 50 MHz – 2.5 GHz	6	12		dB
I_{TX_SC}	TX short circuit current	TX± shorted to GND		44	90	mA
$V_{TX\_CM\_DC}$	Transmitter DC common-mode voltage	Allowed DC CM voltage at TX pins		1.8	2.2	V
$V_{TX\_CM\_AC2}$	TX AC common mode voltage at Gen II speed	$Max(V_{d+} + V_{d-}) /2 – Min(V_{d+} + V_{d-})/2$		30	100	mVpp
$V_{TX\_CM\_AC1}$	TX AC common mode voltage at Gen I speed	$RMS(V_{d+} + V_{d-})/2 – DC_{AVG}(V_{d+} + V_{d-})/2$		3	20	mV
$V_{TX\_CM\_DeltaL0-L0s}$	Absolute Delta DC CM voltage during active and idle states	$\|V_{TX\_CM\_DC\ [L0]}$ – VTX_CM_DC [L0$_s$] |	0		100	mV
$V_{TX\_CM-DC-Line-Delta}$	Absolute delta of DC CM voltage between D+ and D–	$\|V_{TX\_CM\_DC–D+\ [L0]} – V_{TX\_CM\_DC–D–\ [L0]}\|$	0		25	mV
$V_{TX\_idle\_diff-AC-p}$	Electrical idle differential peak output voltage	$\|V_{TX-Idle-D+} – V_{TX-Idle-D–}\|$, LP filtered to remove any DC component	0	1	20	mVpp
$V_{TX\_idle\_diff-DC}$	DC electrical idle differential output voltage	$\|V_{TX\_idle-D+} – V_{TX\_idle-D–}\|$, LP filtered to remove any AC component		1.9		mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver			600	mV
t_R,t_F	Output rise/fall time	De-Emphasis = 0 dB, OS = NC (CH 0 and CH 1) 20%-80% of differential voltage at the output	30	55	70	ps
t_{RF_MM}	Output rise/fall time mismatch	De-Emphasis = 0dB, OS = NC (CH 0 and CH 1) 20%-80% of differential voltage at the output			20	ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	De-Emphasis = 0dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		280	350	ps
T_{INTRA_SKEW}	Output skew (same lane)	5 Gbps			15	ps
T_{INTER_SKEW}	Lane to lane skew	5 Gbps	–25		25	ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times	See Figure 5			8	ns
$T_{tx\_EID\_min}$	Minimum time in EID		20			ns
Tx EQUALIZATION AT GEN II SPEED						
TX_{DJ} (1)	Residual deterministic jitter	At point A1 in Figure 8, EQ/DE=NC, OS=HIGH		25	60	ps p-p
		At point A2 in Figure 8, EQ/DE=NC, OS=LOW		26	60	
		At point B in Figure 8, EQ/DE=NC, OS=HIGH		27	60	
TX_{RJ}	Residual random jitter	D24.3 pattern at point A1/A2/B in Figure 8			0.1	psrms

(1) Refer to Figure 8 with ±K28.5 pattern, –3.5dB DE from source AWG

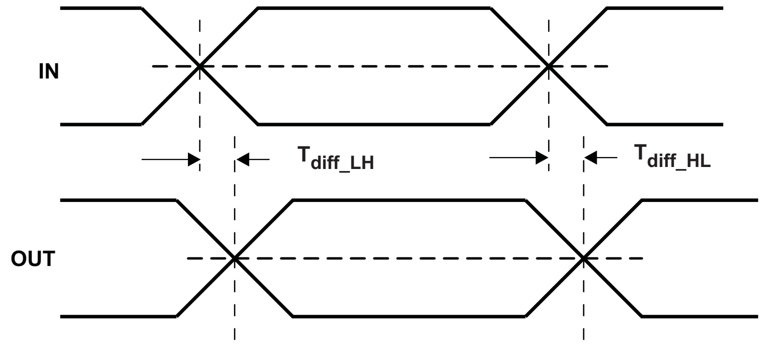


Figure 4. Propagation Delay

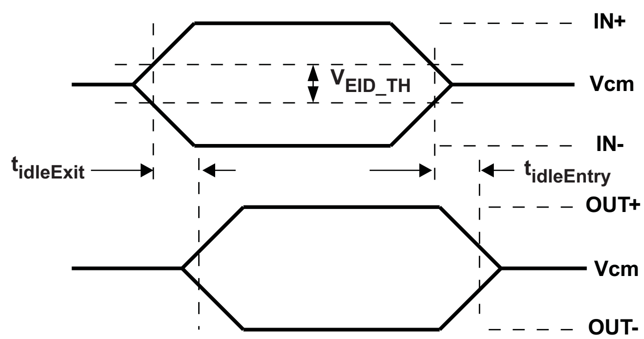


Figure 5. Idle Mode Exit and Entry Delay

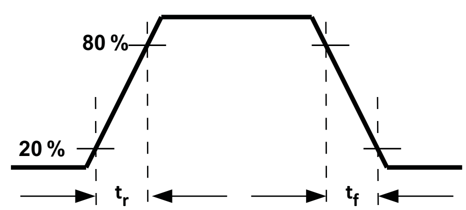


Figure 6. Output Rise and Fall Times

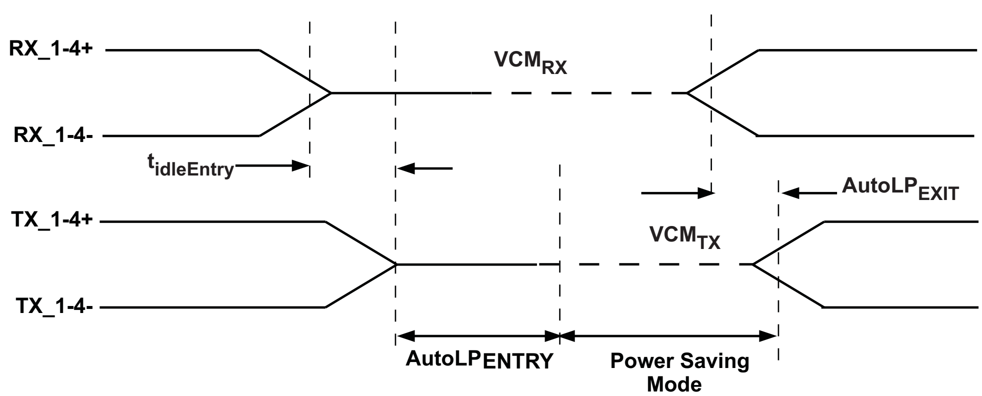


Figure 7. Auto Low Power Mode Timing (when enabled)

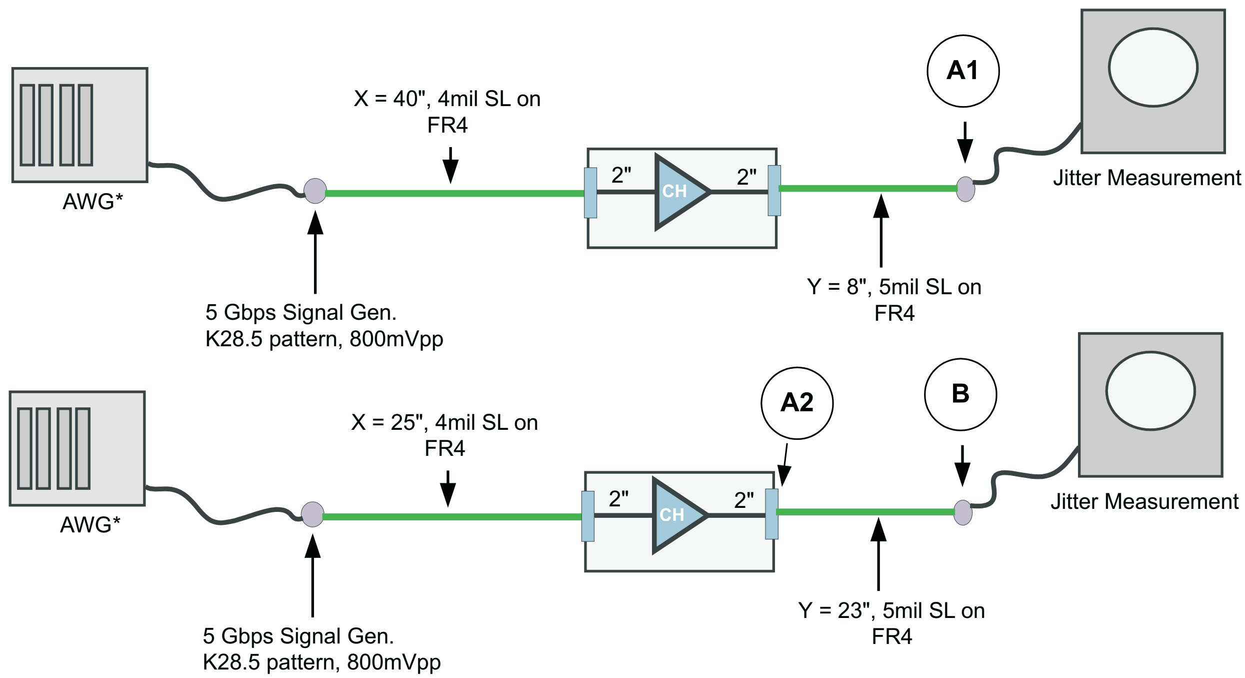


Figure 8. Jitter Measurement Setup

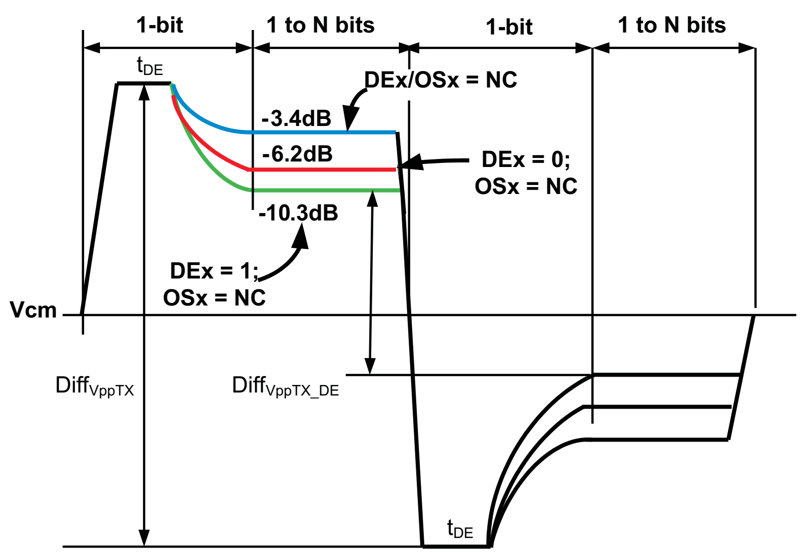


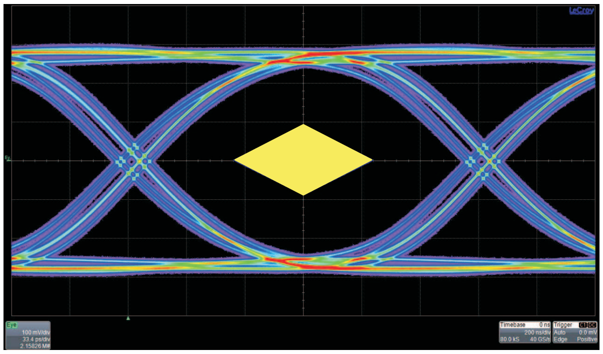
Figure 9. Output De-Emphasis Levels

TYPICAL CHARACTERISTICS

TYPICAL EYE DIAGRAM AND PERFORMANCE CURVES

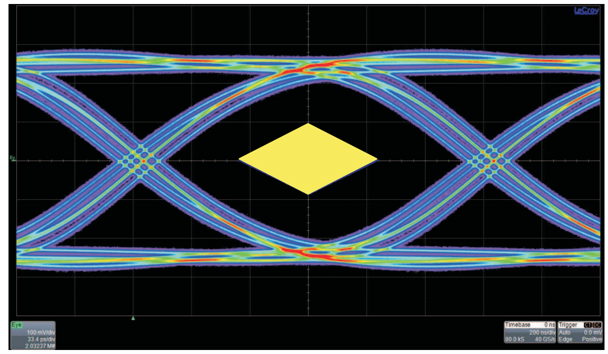
- Input Signal Characteristics – VID = 1000mVpp, DE = –3.5 dB, Pattern = K28.5
- Device Operating Conditions: VCC = 3.3 V, Temp = 25°C
- All trace are 4 mils
- PCIe Gen I and Gen II compliance mask shown

AT GEN II SPEED



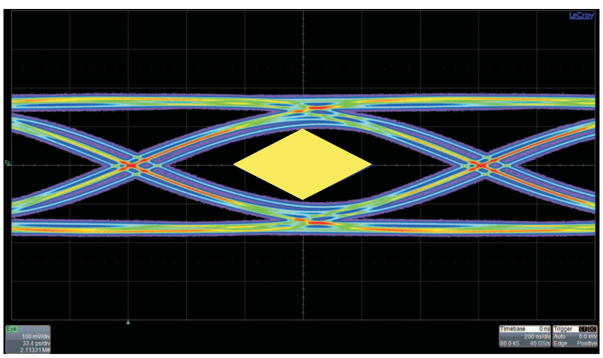
Input Trace = 4", Output Trace = 8"
EQ = 0 dB, OS = 833 mVpp, DE = –1.9 dB

Figure 10.



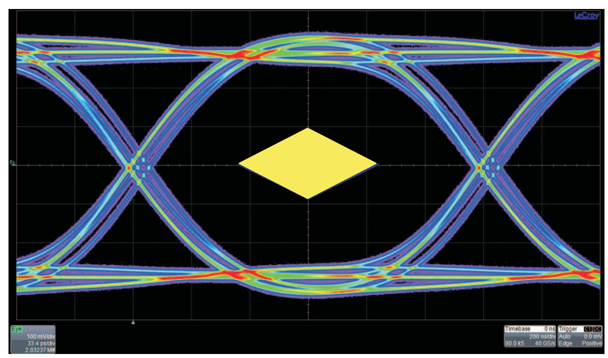
Input Trace = 4", Output Trace = 16"
EQ = 0 dB, OS = 1166 mVpp, DE = –4.9 dB

Figure 11.



Input Trace = 4", Output Trace = 28"
EQ = 0 dB, OS = 1166 mVpp, DE = –7.4 dB

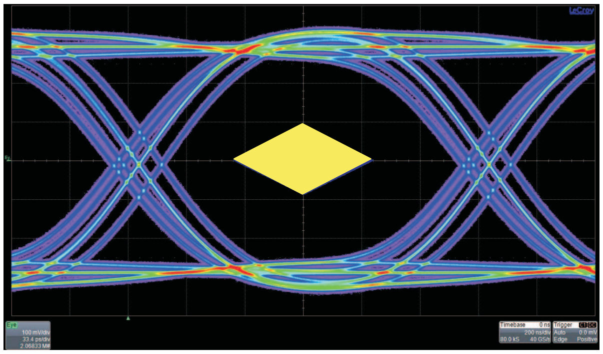
Figure 12.



Input Trace = 16", Output Trace = 4"
EQ = 0 dB, OS = 833 mVpp, DE = –1.9 dB

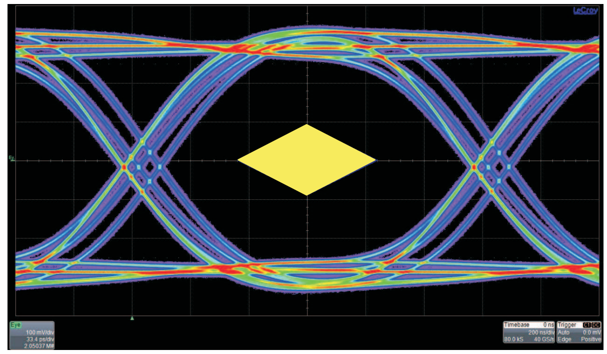
Figure 13.

TYPICAL CHARACTERISTICS (continued)



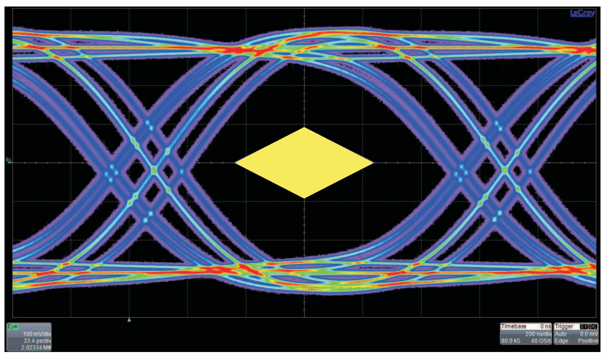
Input Trace = 28", Output Trace = 4"
EQ = 7 dB, OS = 833 mVpp, DE = –1.9 dB

Figure 14.



Input Trace = 36", Output Trace = 4"
EQ = 7 dB, OS = 833 mVpp, DE = –1.9 dB

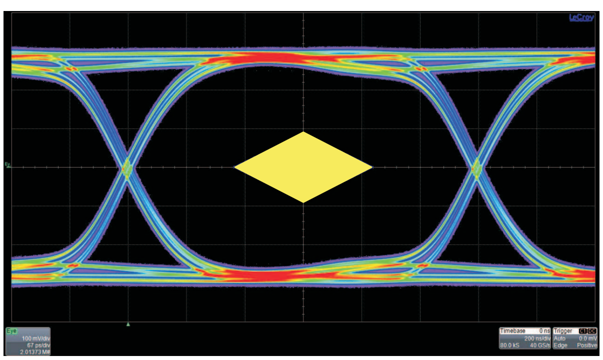
Figure 15.



Input Trace = 48", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = –1.9 dB

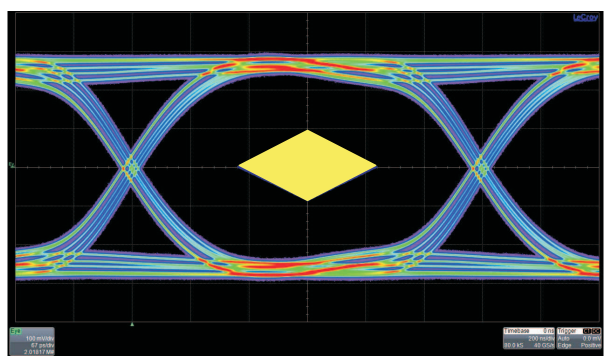
Figure 16.

AT GEN I SPEED



Input Trace = 4", Output Trace = 8"
EQ = 7 dB, OS = 833 mVpp, DE = –1.9 dB

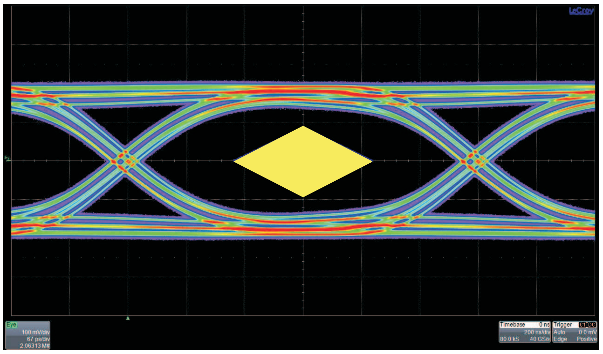
Figure 17.



Input Trace = 4", Output Trace = 16"
EQ = 7 dB, OS = 1166 mVpp, DE = –4.9 dB

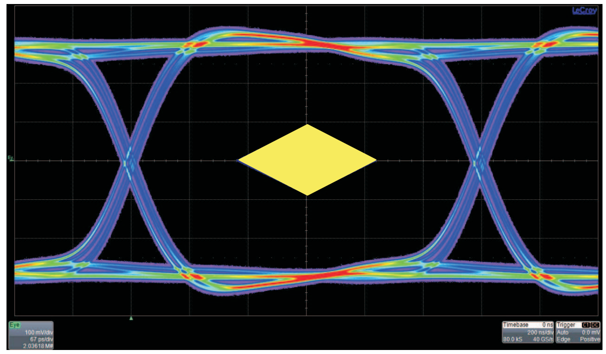
Figure 18.

TYPICAL CHARACTERISTICS (continued)



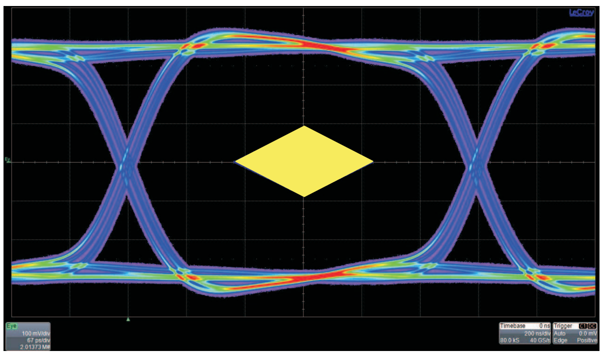
Input Trace = 4", Output Trace = 28"
EQ = 7 dB, OS = 1166 mVpp, DE = – 7.4 dB

Figure 19.



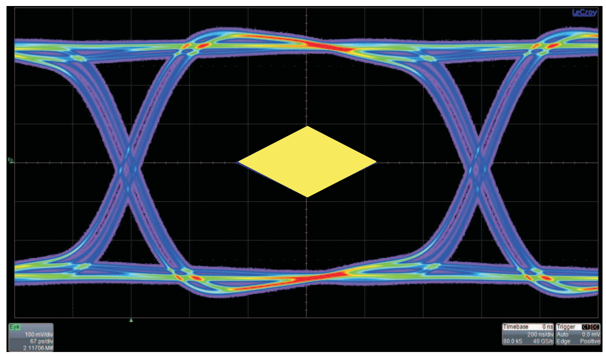
Input Trace = 16", Output Trace = 4"
EQ = 7 dB, OS = 833 mVpp, DE = – 1.9 dB

Figure 20.



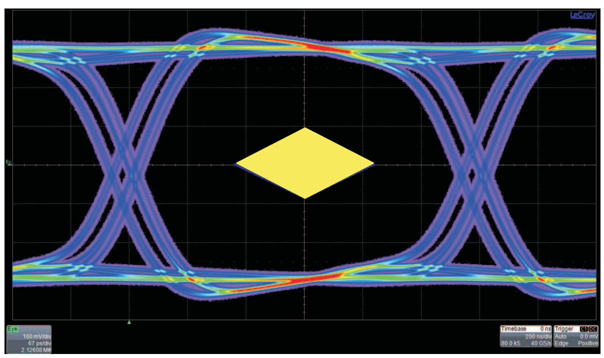
Input Trace = 28", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = – 1.9 dB

Figure 21.



Input Trace = 36", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = – 1.9 dB

Figure 22.



Input Trace = 48", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = – 1.9 dB

Figure 23.

查询"SN65LVPE504"供应商

PACKAG

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
SN65LVPE504RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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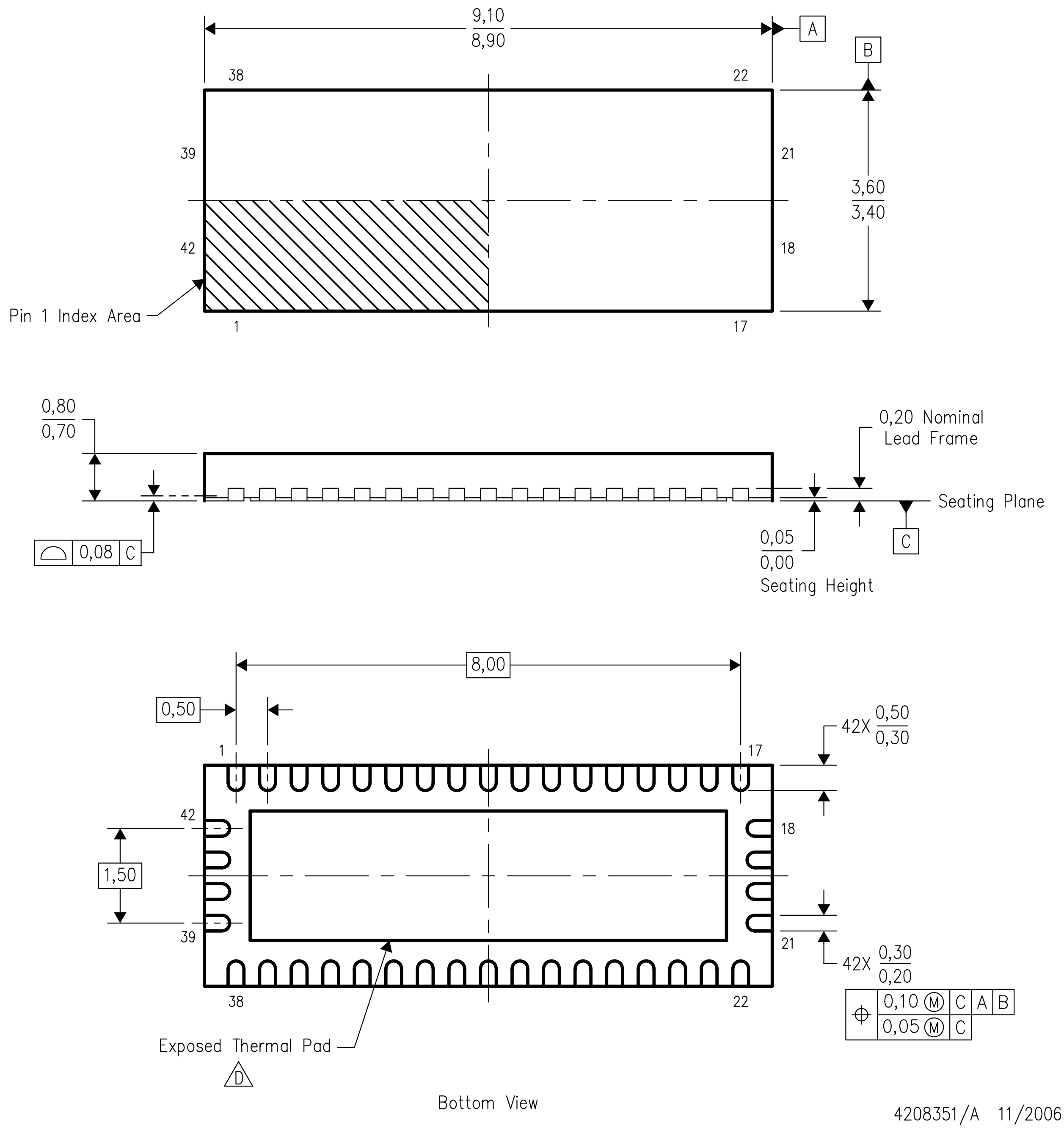
RUA (R-PQFP-N42) PLASTIC QUAD FLATPACK



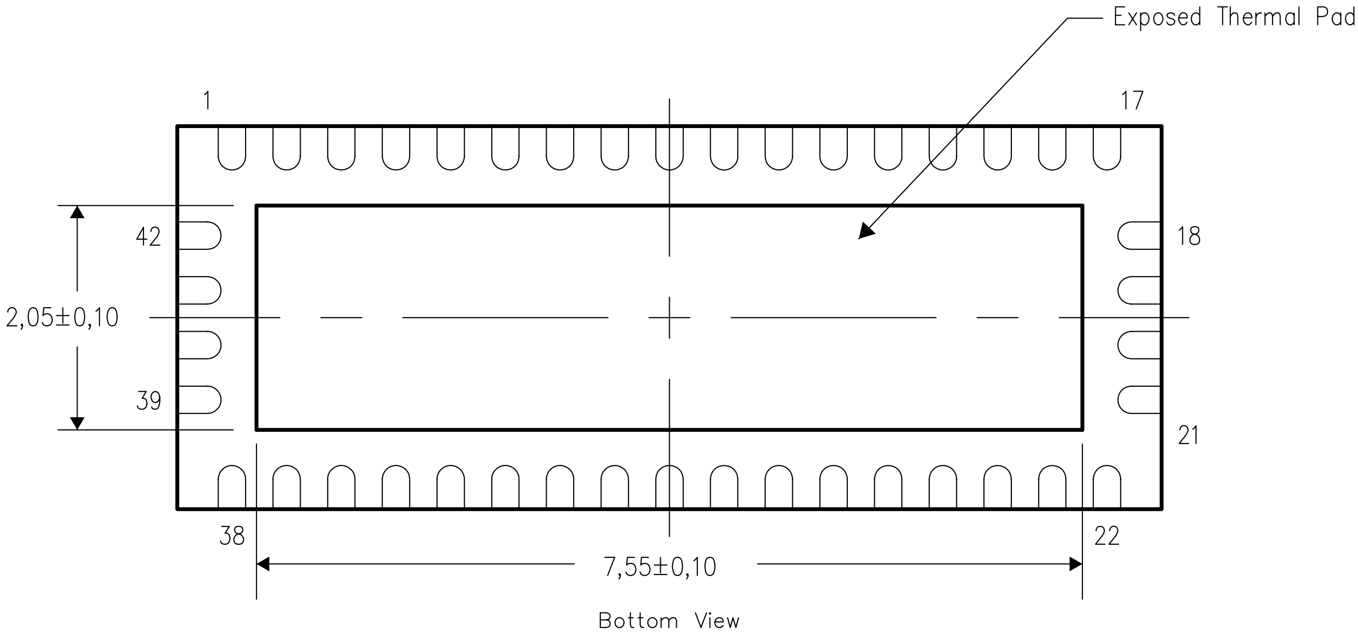
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

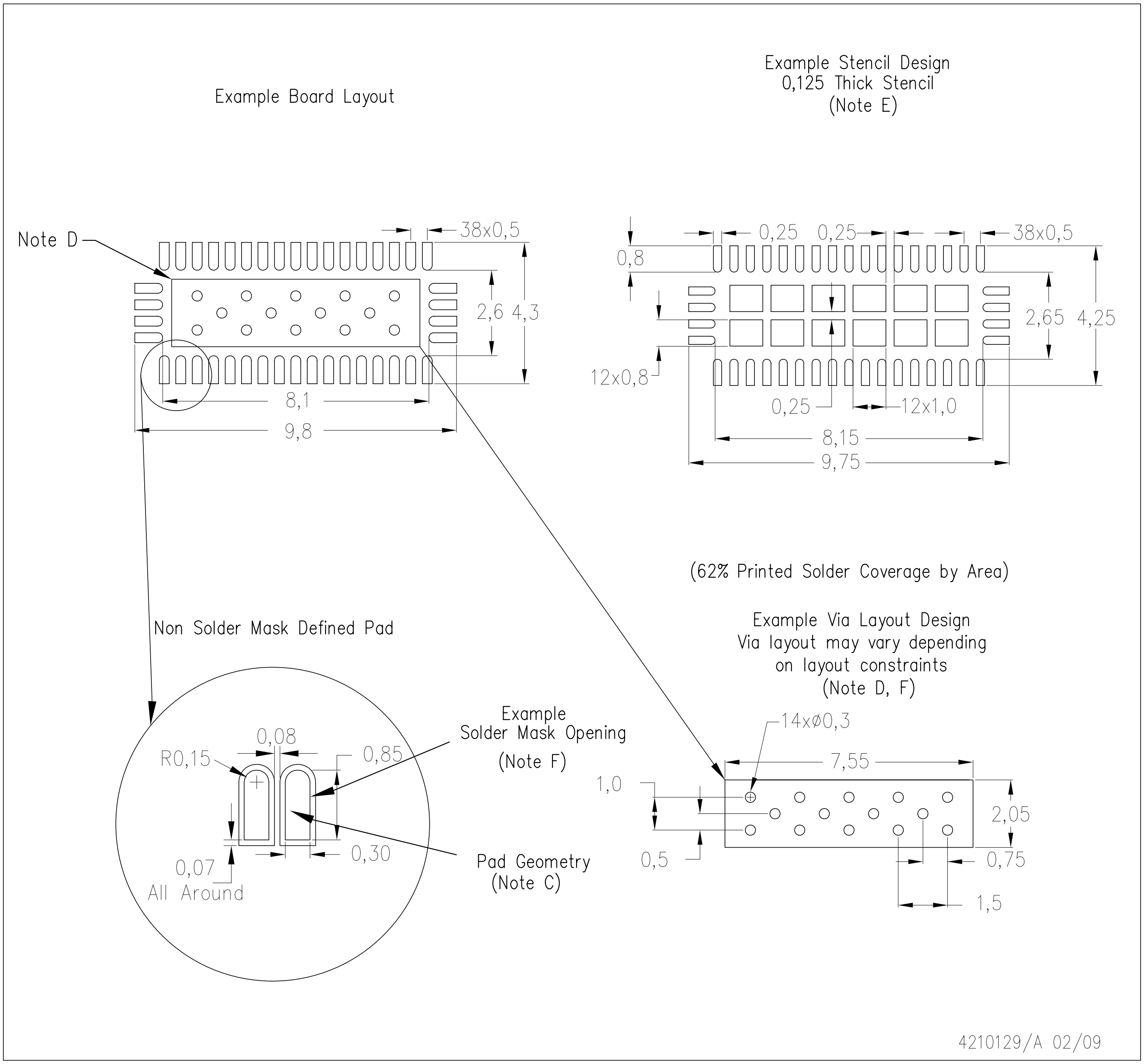


NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

查询"SN65LVPE504"供应商

RUA (R–PWQFN–N42)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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