

9-bit bus transceiver (3-State)

查询74ABT863D-T供应商

74ABT863

FEATURES

- Provides high performance bus interface buffering for wide data/address paths or buses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200 V per Machine Model

- Power-up 3-State
- Live insertion/extraction permitted
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT863 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity.

The 74ABT863 9-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

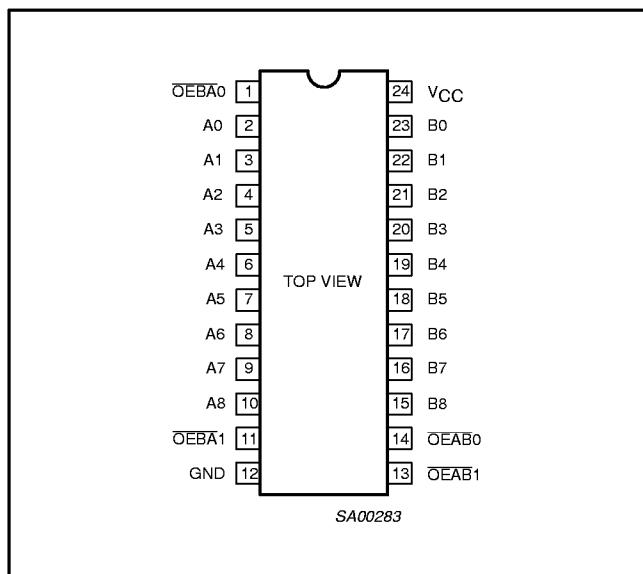
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	3.3	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	−40°C to +85°C	74ABT863 N	74ABT863 N	SOT222-1
24-Pin plastic SO	−40°C to +85°C	74ABT863 D	74ABT863 D	SOT137-1
24-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT863 DB	74ABT863 DB	SOT340-1
24-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT863 PW	74ABT863PW DH	SOT355-1

PIN CONFIGURATION



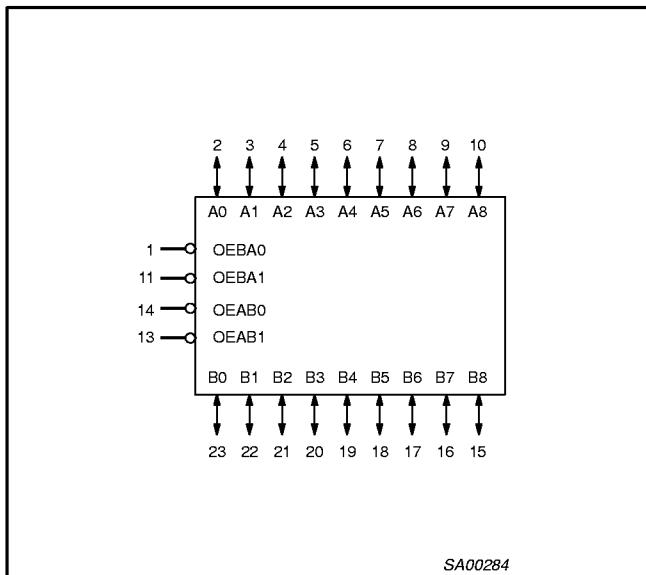
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 13	\overline{OEBA}_0 , \overline{OEAB}_1	Output enable inputs (active-Low)
2, 3, 4, 5, 6, 7, 8, 9, 10	A0-A8	Data inputs/outputs (A side)
23, 22, 21, 20, 19, 18, 17, 16, 15	B0-B8	Data inputs/outputs (B side)
1, 11	\overline{OEBA}_0 , \overline{OEBA}_1	Output enable inputs (active-Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

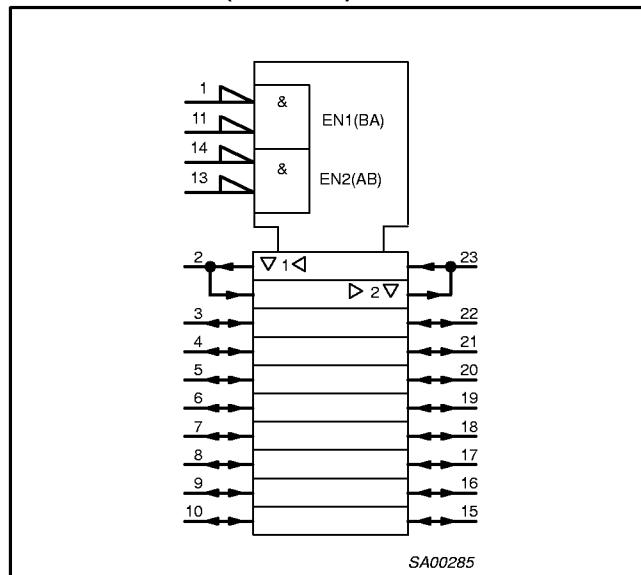
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OPERATING MODE
OEAB0	OEAB1	OEBA0	OEBA1	
L	L	H	X	A data to B bus
L	L	X	H	A data to B bus
H	X	L	L	B data to A bus
X	H	L	L	B data to A bus
H	H	H	H	Z

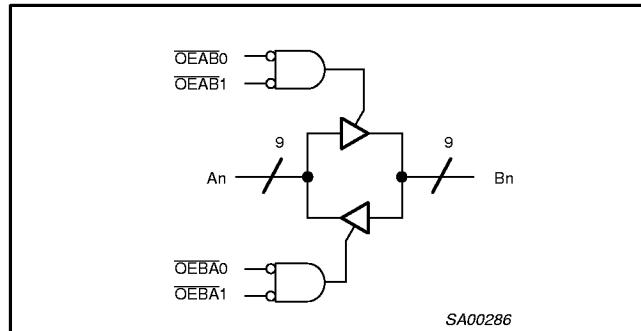
H = High voltage level

L = Low voltage level

X = Don't care

Z = High impedance "off" state

LOGIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS^{1,2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT	
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			
			Min	Typ	Max	Min	Max		
V_{IK}	Input clamp voltage	$V_{CC} = 4.5\text{V}$; $I_{IK} = -18\text{mA}$		-0.9	-1.2		-1.2	V	
V_{OH}	High-level output voltage	$V_{CC} = 4.5\text{V}$; $I_{OH} = -3\text{mA}$; $V_I = V_{IL}$ or V_{IH}	2.5	3.2		2.5		V	
		$V_{CC} = 5.0\text{V}$; $I_{OH} = -3\text{mA}$; $V_I = V_{IL}$ or V_{IH}	3.0	3.7		3.0		V	
		$V_{CC} = 4.5\text{V}$; $I_{OH} = -32\text{mA}$; $V_I = V_{IL}$ or V_{IH}	2.0	2.3		2.0		V	
V_{OL}	Low-level output voltage	$V_{CC} = 4.5\text{V}$; $I_{OL} = 64\text{mA}$; $V_I = V_{IL}$ or V_{IH}		0.42	0.55		0.55	V	
I_I	Input leakage current	$V_{CC} = 5.5\text{V}$; $V_I = \text{GND}$ or 5.5V		± 0.01	± 1.0		± 1.0	μA	
		$V_{CC} = 5.5\text{V}$; $V_I = \text{GND}$ or 5.5V		± 5	± 100		± 100	μA	
I_{OFF}	Power-off leakage current	$V_{CC} = 0.0\text{V}$; V_O or $V_I \leq 4.5\text{V}$		± 5.0	± 100		± 100	μA	
$I_{PU/PD}$	Power-up/down 3-State output current ³	$V_{CC} = 2.0\text{V}$; $V_O = 0.5\text{V}$; $V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{Don't care}$		± 5.0	± 50		± 50	μA	
$I_{IH} + I_{OZH}$	3-State output High current	$V_{CC} = 5.5\text{V}$; $V_O = 2.7\text{V}$; $V_I = V_{IL}$ or V_{IH}		5.0	50		50	μA	
$I_{IL} + I_{OZL}$	3-State output Low current	$V_{CC} = 5.5\text{V}$; $V_O = 0.5\text{V}$; $V_I = V_{IL}$ or V_{IH}		-5.0	-50		-50	μA	
I_{CEX}	Output high leakage current	$V_{CC} = 5.5\text{V}$; $V_O = 5.5\text{V}$; $V_I = \text{GND}$ or V_{CC}		5.0	50		50	μA	
I_O	Output current ¹	$V_{CC} = 5.5\text{V}$; $V_O = 2.5\text{V}$	-50	-63	-180	-50	-180	mA	
I_{CCH}	Quiescent supply current	$V_{CC} = 5.5\text{V}$; Outputs High, $V_I = \text{GND}$ or V_{CC}		110	250		250	μA	
I_{CCL}		$V_{CC} = 5.5\text{V}$; Outputs Low, $V_I = \text{GND}$ or V_{CC}		25	38		38	mA	
I_{CCZ}		$V_{CC} = 5.5\text{V}$; Outputs 3-State; $V_I = \text{GND}$ or V_{CC}		110	250		250	μA	
ΔI_{CC}	Additional supply current per input pin ²	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA	
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; $V_{CC} = 5.5\text{V}$		110	250		250	μA	
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$, a transition time of up to 100 μsec is permitted.

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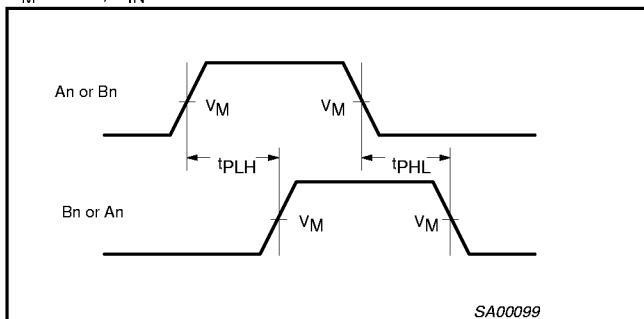
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AC CHARACTERISTICS

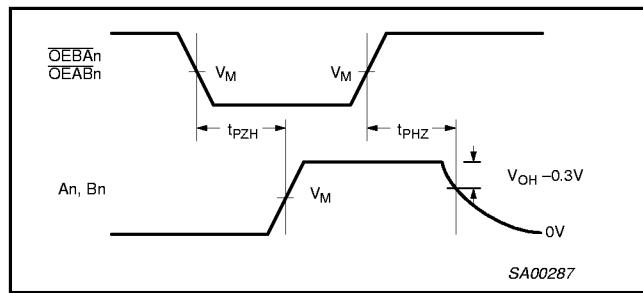
 $V_{IN} = 0V$, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT	
			$T_{amb} = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$			$T_{amb} = -40 \text{ to } +85^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$			
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation delay A0-7 to B0-7 or Bn to An A8 to B8 An to Bn or Bn to An	1	1.3 1.3 1.2	3.3 4.5 2.8	4.8 5.9 4.6	1.3 2.5 1.2	5.3 6.3 5.2	ns	
t_{PHL}									
t_{PZH}	Output enable time $\overline{OE}Bn$ to An or $\overline{OE}An$ to B0-7 $\overline{OE}Bn$ to B8 $\overline{OE}An$ to An or $\overline{OE}Bn$ to Bn	2	1.3 1.3 2.2	4.3 4.9 5.2	5.5 6.4 6.3	1.3 2.4 2.2	6.5 7.5 7.3	ns	
t_{PZL}		3							
t_{PHZ}	Output disable time from High and Low level	2	3.0 2.5	5.0 4.8	6.3 6.3	3.0 2.5	7.1 6.8	ns	
t_{PLZ}		3							

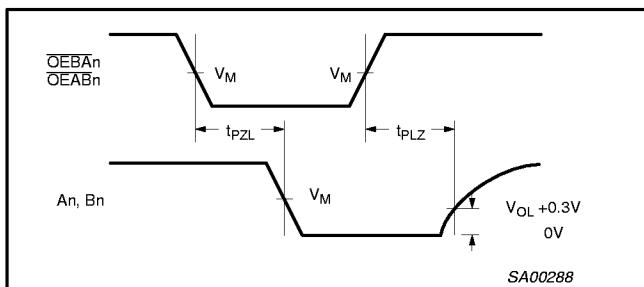
AC WAVEFORMS

 $V_M = 1.5\text{V}$, $V_{IN} = \text{GND to } 3.0\text{V}$ 

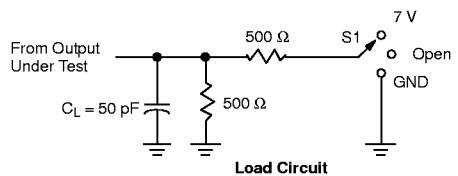
Waveform 1. Propagation Delay for Data to Outputs



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance;
see AC CHARACTERISTICS for value.

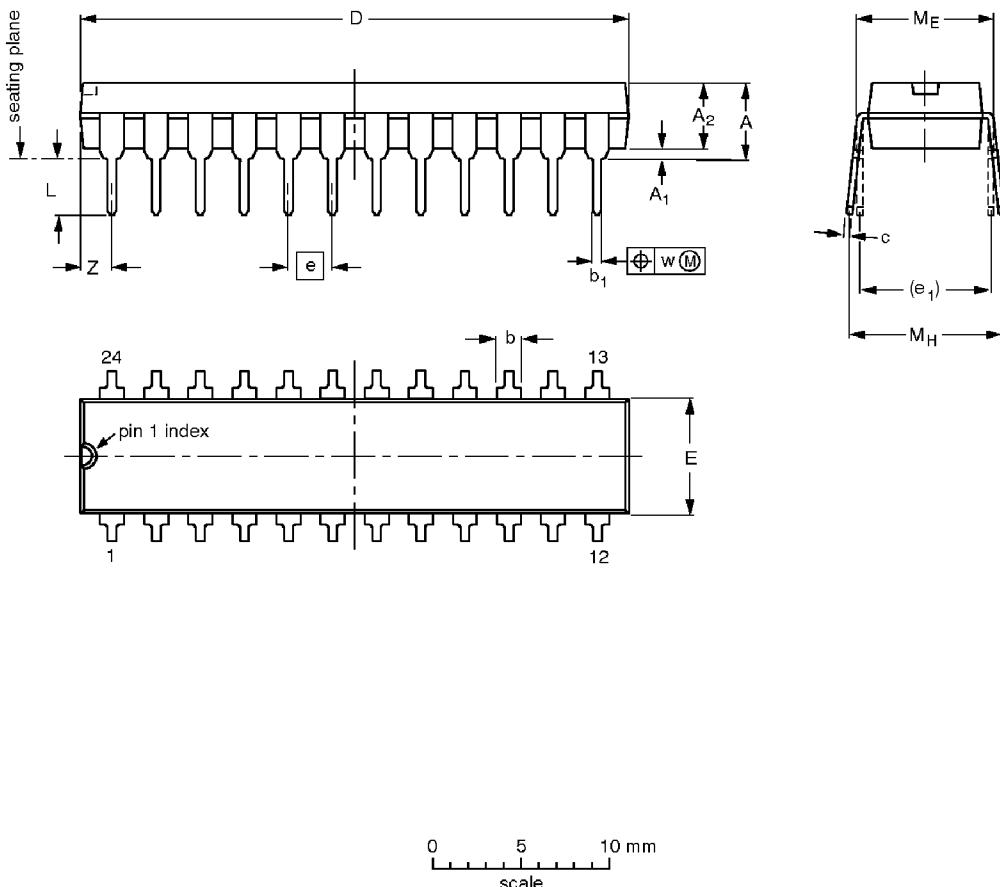
SA00012

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

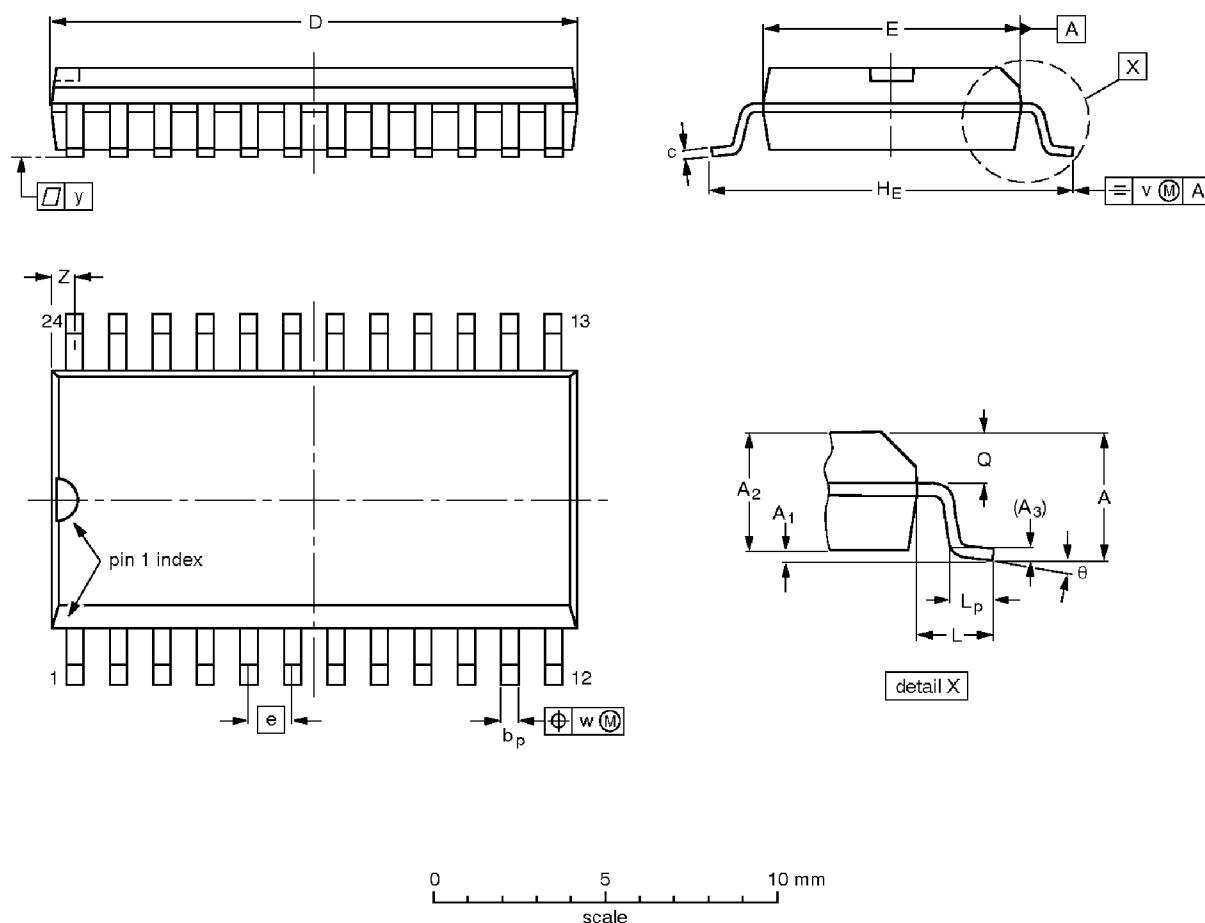
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

9-bit bus transceiver (3-State)
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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65 0.10	0.30 2.25	2.45	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10 0.004	0.012 0.089	0.096 0.014	0.01	0.019 0.009	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

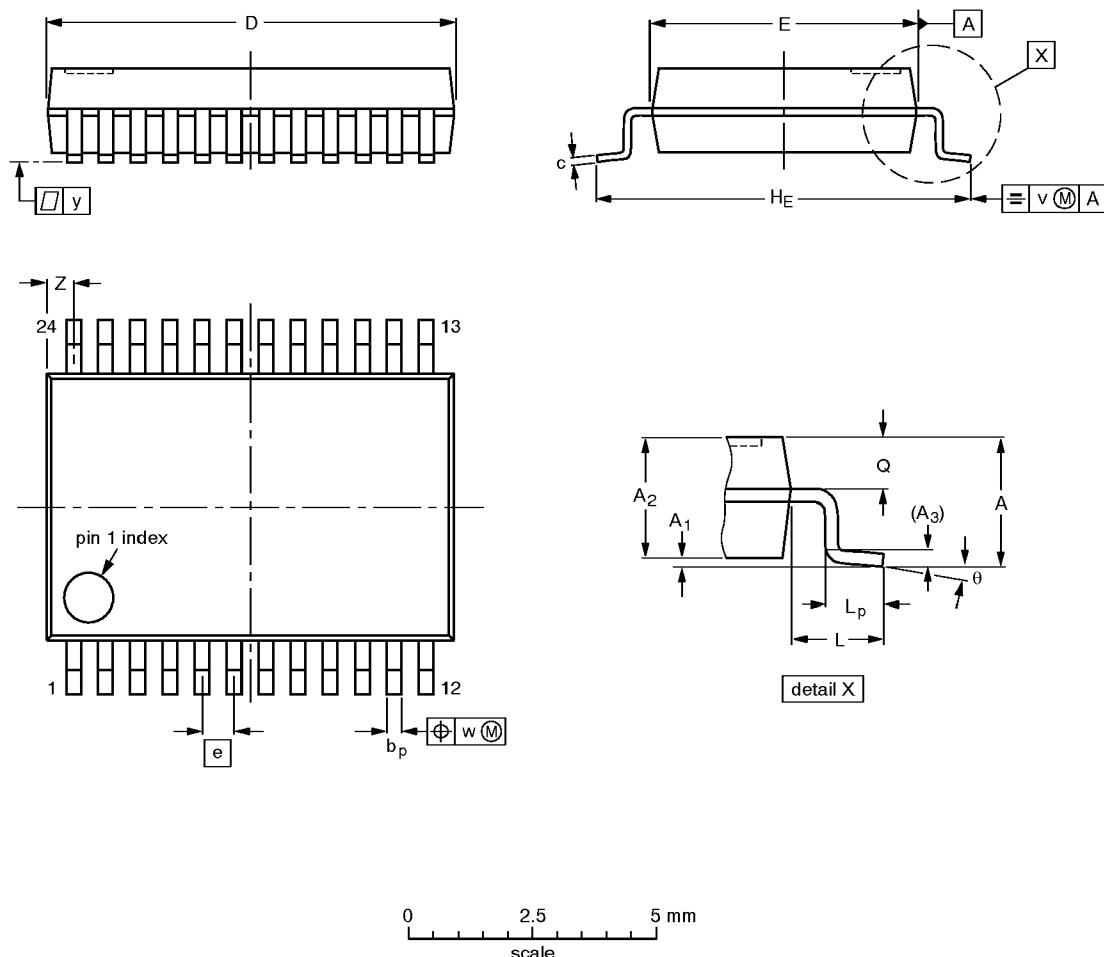
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

DIMENSIONS (mm are the original dimensions)																		
UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

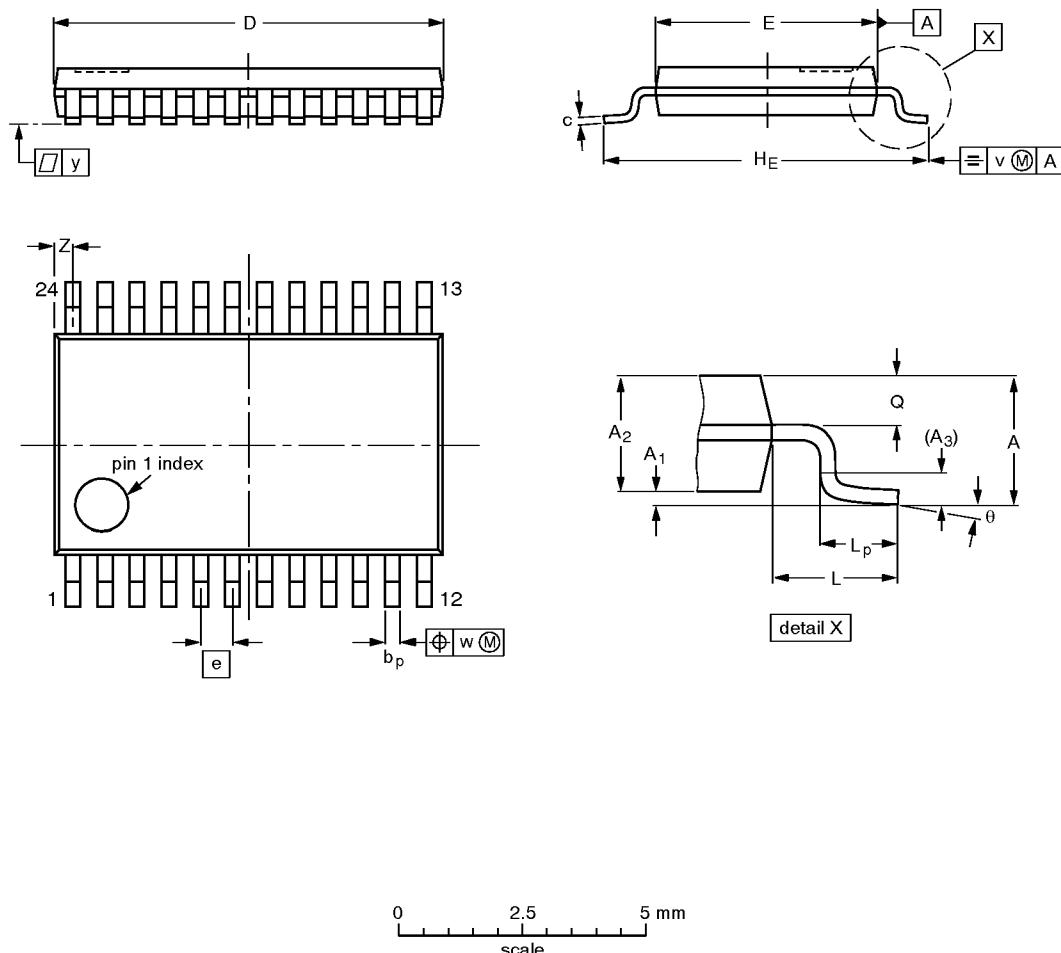
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

9-bit bus transceiver (3-State)
74ABT863D-T 供应商

74ABT863

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.10 0.05	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04