16-Bit transceiver with dual enable; 3-state | 74ALVCH16623

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Multibyte™ pin-out architecture**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVCH16623 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVCH16623 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

This 16-bit bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (nOE_{AB}, $n\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of nOE_{AB} and $n\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when all control inputs are enabled and all other data sources to the four sets of the bus lines are at high impedance OFF-state, all sets of bus lines will remain at their last states. The 8-bit codes appearing on the two double sets of buses will be complementary. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.7	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVCH16623DL	48	SSOP48	plastic	SOT370-1
74ALVCH16623DGG	48	TSSOP48	plastic	SOT362-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1OE_{AB}$	'1' output enable input (active HIGH)
2, 3, 5, 6, 8, 9, 11, 12	$1B_0$ to $1B_7$	'1B' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2B_0$ to $2B_7$	'2B' data inputs/outputs
24	$2OE_{AB}$	'2' output enable input (active HIGH)
25	$2\overline{OE}_{BA}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs/outputs
48	$1\overline{OE}_{BA}$	'1' output enable input (active LOW)

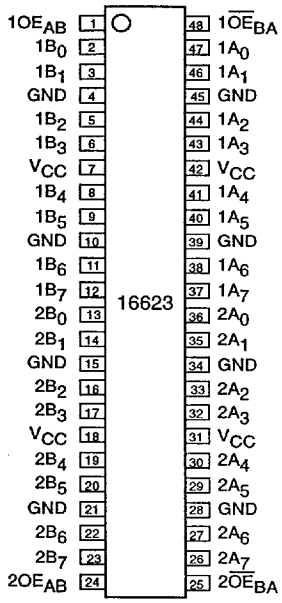


Fig.1 Pin configuration.

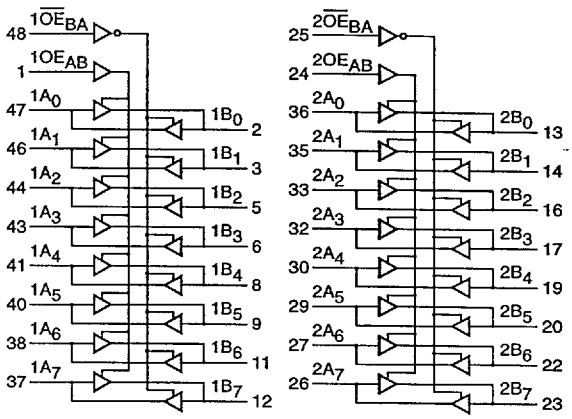


Fig.2 Logic symbol.

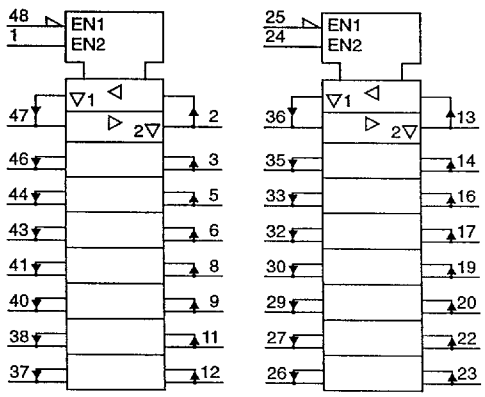


Fig.3 IEC logic symbol.

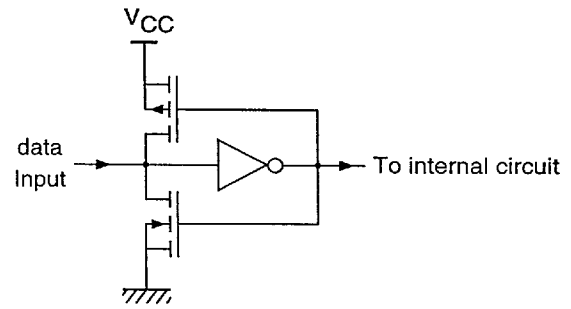


Fig. 4 Bushold circuit

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE_{AB}	$n\overline{OE}_{BA}$	nA_n	nB_n
L	L	A = B	inputs
H	H	inputs	B = A
L	H	Z	Z
H	L	A = B	B = A

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74ALVCH16623

For the DC characteristics see chapter "ALVCH family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVCH16623

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n; nB_n to nA_n	– 1.5 1.5	15 3.1 2.7*	– 4.0 3.6	ns	1.2 2.7 3.0 to 3.6	Figs 4, 7
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	– 1.5 1.5	– 3.5 3.1*	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Figs 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	– 1.5 1.5	– 3.3 3.1*	– 5.2 5.0	ns	1.2 2.7 3.0 to 3.6	Figs 6, 7
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	– 1.5 1.5	– 3.9 3.4*	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Figs 5, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	– 1.5 1.5	– 3.0 2.8*	– 5.2 5.0	ns	1.2 2.7 3.0 to 3.6	Figs 5, 7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

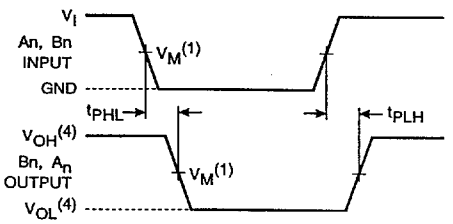


Fig. 4 Waveforms showing the input (nA_n, nB_n) to output (nB_n, nA_n) propagation delay times.

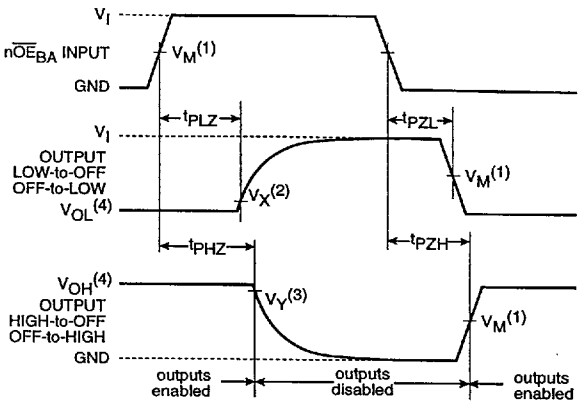


Fig.5 Waveforms showing the 3-state enable and disable times for $n\overline{OE}_{BA}$ input.

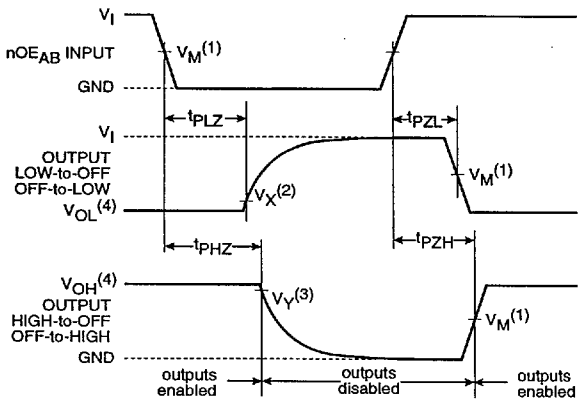
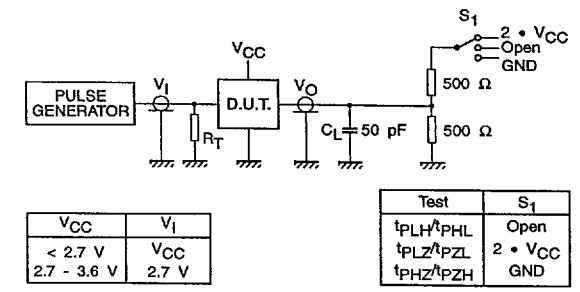


Fig.6 Waveforms showing the 3-state enable and disable times for nOE_{AB} input.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.