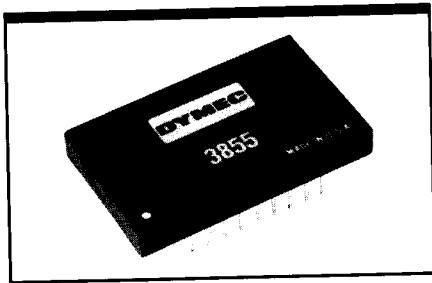


Signal Conditioning 5MHz V/F Converter



Description

The 3855 is a high performance, precision 5MHz full scale voltage-to-frequency converter with integral low noise, user-configurable high input impedance buffer and gain stage amplifiers. Each functional block may be used independently or in combination to obtain a signal conditioning and V/F converter subsystem. By integrating a high performance amplifier and V/F in the same package, users can quickly

implement a front-end/converter design with guaranteed end-to-end specifications, tailored to their application requirements, and save design time and pc board space, reduce potential ground loops and improve overall performance.

The input buffer stage provides an input impedance of 10^{12} ohms. The separate inverting gain stage offers user programmable gains by adding a pair of precision resistors. When used in combination, the input buffer/gain stage offer an extremely stable amplifier chain.

The V/F converter itself accepts a $-100\mu\text{V}$ to -10V full scale analog signal which is converted to an output frequency proportional to the input signal and 5MHz, within $\pm 0.02\%$ linearity. Buffered complementary TTL-compatible frequency outputs are provided that will drive

FEATURES

- Integral High Input Impedance Buffer**
 10^{12} ohms
- Integral User-Programmable Inverting Gain Stage**
 Two-resistor Programming
- Wide Dynamic Range**
 $5,000,000:1$
 $>134\text{dB}$
- Precision V/F Converter**
 $\pm 0.02\%$ Linearity
- Excellent Stability**
 $10\mu\text{V}/^\circ\text{C}$ offset
 $60\text{ppm}/^\circ\text{C}$ gain
- Complementary Frequency Outputs**
 TTL/CMOS Compatible
- Small Size**
 24-pin Double-width DIL Package
- Low Power**
 $<1.15\text{W}$

APPLICATIONS

- Precision Integration
- Analytical Instrumentation
- Medical Instrumentation
- Weighing Systems
- Data Recording
- Data Transmission

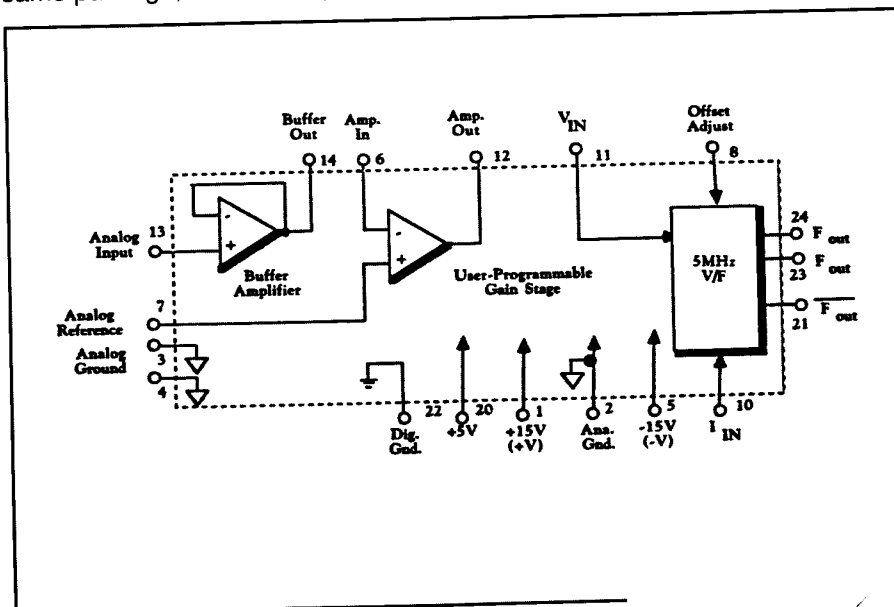


Figure 1. 3855 Block Diagram

Specifications

All Specifications Guaranteed at 25°C Unless Otherwise Noted

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V/F CONVERTER

ANALOG INPUT

Input Range

-100 μ V to -10V

Overrange

5% minimum

Configuration

Single-ended

Impedance

6K Ω nominal

Offset Voltage

± 7 mV typical, ± 10 mV maximum;
adjustable to zero

Overvoltage Protection

$\pm V_S$ without damage

TRANSFER CHARACTERISTICS

Full Scale Frequency Output (Fout)

5.000MHz; $\pm 5\%$ overrange minimum

V/F Transfer Characteristic

5MHz(Vin/10V)

Gain Error

$\pm 1\%$, trimmable to zero

Non-Linearity

$\pm 0.02\%$ FS, $\pm 0.02\%$ of input, maximum

Full Scale Step Response

2 cycles of new frequency, plus 10 μ s;
to $\pm 0.01\%$

Overload Recovery

10 cycles of new frequency

STABILITY

(Exclusive of external components)

Gain - Tempco

± 60 ppm/ $^{\circ}$ C typical, ± 100 ppm/ $^{\circ}$ C maximum

Gain - Power Supply Sensitivity

200ppm per 1% change in power supply voltage

Offset - Tempco

$\pm 10\mu$ V/ $^{\circ}$ C typical, $\pm 30\mu$ V/ $^{\circ}$ C maximum

Offset - Power Supply Sensitivity

$\pm 10\mu$ V per 1% change in power supply voltage

Warmup Time

< 2 minutes to specified accuracy

OUTPUT

Pulse Polarity

Positive and Negative

Pulse Width

100ns \pm 20ns

Logic Levels (V_{CC}=+5V)

Logic "1" (High) = +4.0V \pm 0.5V

Logic "0" (Low) = <0.4V @ 3mA sink

Load

≤ 50 pF for rated performance;

10 LSTTL loads

INPUT BUFFER

Input Offset Voltage

5mV typical, 10mV maximum

Input Offset Current

25pF typical, 100pA maximum;
doubles every 10 $^{\circ}$ C

Input Impedance

10¹² Ω

Common Mode Voltage Range

11V minimum

Gain

+1

Bandwidth

4MHz typical

Equivalent Input Voltage Noise

25nV/ \sqrt Hz typical; R_S=100 Ω , f=1kHz

Equivalent Input Current Noise

0.01pA/ \sqrt Hz typical; f=1kHz

GAIN STAGE

Input Offset Voltage

5mV typical, 10mV maximum

Input Offset Current

25pA typical, 100pA maximum;
doubles every 10 $^{\circ}$ C

Input Impedance

10¹² Ω

Common Mode Voltage Range

11V minimum

Large Signal Voltage Gain

25V/mV minimum, 100V/mV typical;
V_O=10V, R_L=2.0k Ω

Supply Voltage Rejection

70dB minimum, 100dB typical

Slew Rate

13V/ μ s typical; gain=-1

Gain-Bandwidth Product

4MHz typical

Equivalent Input Voltage Noise

25nV/ \sqrt Hz typical; R_S=100 Ω , f=1kHz

Equivalent Input Current Noise

0.01pA/ \sqrt Hz typical; f=1kHz

TOTAL POWER REQUIREMENTS

(+V_S) +15V, $\pm 3\%$

40mA maximum

(-V_S) -15V, $\pm 3\%$

20mA maximum

(+V_{CC}) +5V, $\pm 5\%$

40mA maximum

Power Dissipation

1.10W maximum

Specifications (continued)

<p>ENVIRONMENTAL AND MECHANICAL</p> <p>Operating Temperature 0°C to +70°C</p> <p>Storage Temperature -55°C to +125°C</p>	<p>Dimensions 1.6"x0.69"x0.22" (40.6x17.5x5.5mm)</p>
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Description (continued)

up to 50pF capacitive loads. Stability of the V/F over temperature is excellent, with offset and gain temperature coefficients of 10µV/°C and

60ppm/°C typical respectively.

The 3855 is packaged in a 1.6"x0.69"x0.22" 24-pin DIL plastic package. Pin spacing is 0.1"x0.6".

Power dissipation is less than 1.10W. Operation to specified performance is over the 0°C to +70°C temperature range.

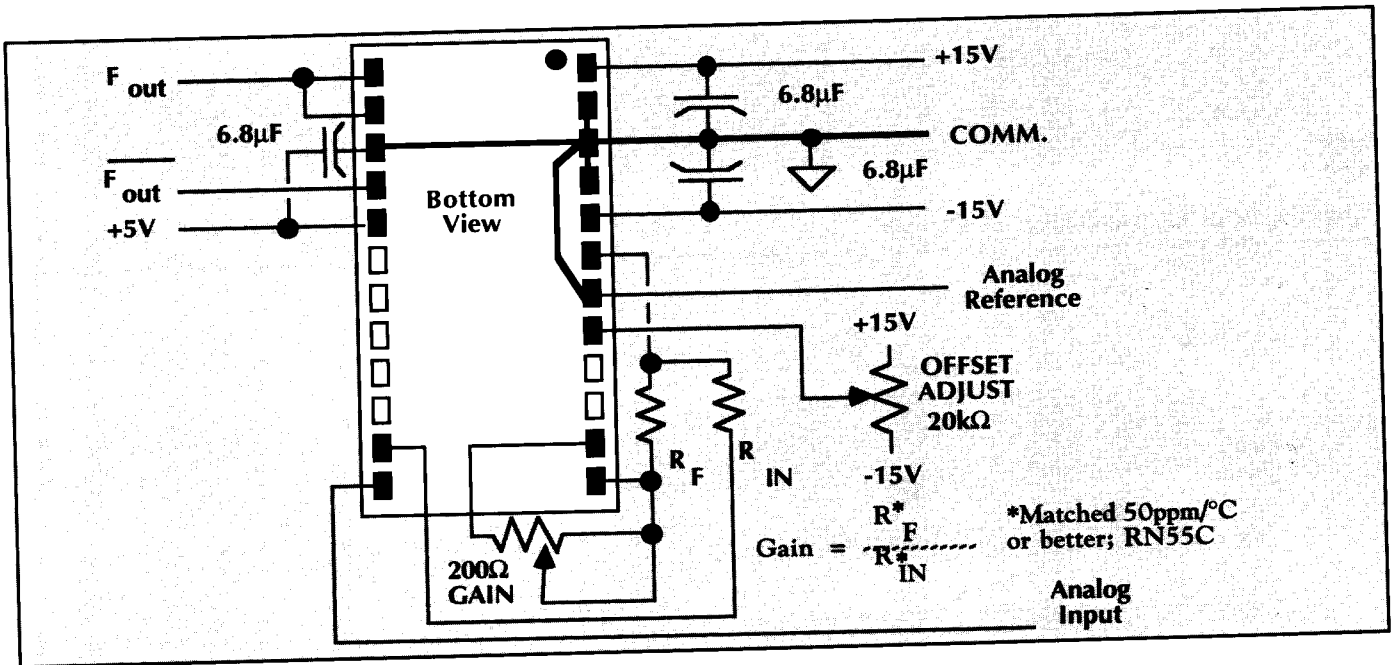


Figure 2. Recommended Interconnection and Signal Routing

Using the 3855

General Considerations

As with any high precision, signal conditioning and data acquisition and conversion circuitry, the use of a ground plane is strongly recommended. The layout should be clean, with output pulses routed as far away as possible from the input analog signals. As shown in Figure 2, bypass capacitors should be mounted as close as possible to the power supply pins of the 3855.

Gain Stage

As shown in Figure 2, the gain stage is configured such that the gain can be set using a matched set of user-supplied, 50ppm or better, RN55C metal film resistors.

Improving the Offset TC Performance

Due to the offset voltage

tracking and compensation scheme employed in the 3855 design, an approximate 2:1 improvement in the offset TC is possible for the combination buffer/gain stage, over the gain stage alone. In circuit configurations that do not require the high impedance buffer, consideration should be given to using the buffer stage to improve the overall offset TC performance of the complete front-end.

Using the 3855 (continued)

Offset and Gain Calibration

The V/F OFFSET adjustment potentiometer should be a 20K Ω , 10-turn unit. With this pot in the circuit, initial offsets from the V/F, buffer and gain stage combination of up to ± 50 mV may be trimmed to zero.

The V/F GAIN adjustment potentiometer should be a 200 Ω , 10-turn unit with a recommended temperature coefficient of 100ppm/ $^{\circ}$ C or better. With this potentiometer in the circuit, initial gain errors of up to $\pm 2\%$ may be trimmed to zero.

To calibrate the 3855, the offset is adjusted prior to adjusting the gain. With a voltage at the analog input of the buffer/gain stage/V-to-F configuration that will yield a -10mV signal at pin 11 (V_{IN}) of the V/F, adjust the OFFSET pot until an output frequency of 5.000kHz is

obtained at pins 23, 24 or 21. With a full scale voltage at the input of the circuit such that -10.000V is present at pin 11 (V_{IN}) of the V/F, adjust the gain pot for an output frequency of 5.000MHz. Calibration is now completed.

Grounding

The Analog and Digital grounds are internally separated within the 3855 circuitry. The use of a ground plane is recommended with the 3855 to avoid ground loops and common mode problems. If a ground plane is not feasible, then a single-point ground ("star" ground) must be used. Significant performance degradation will result if these grounding schemes are not utilized.

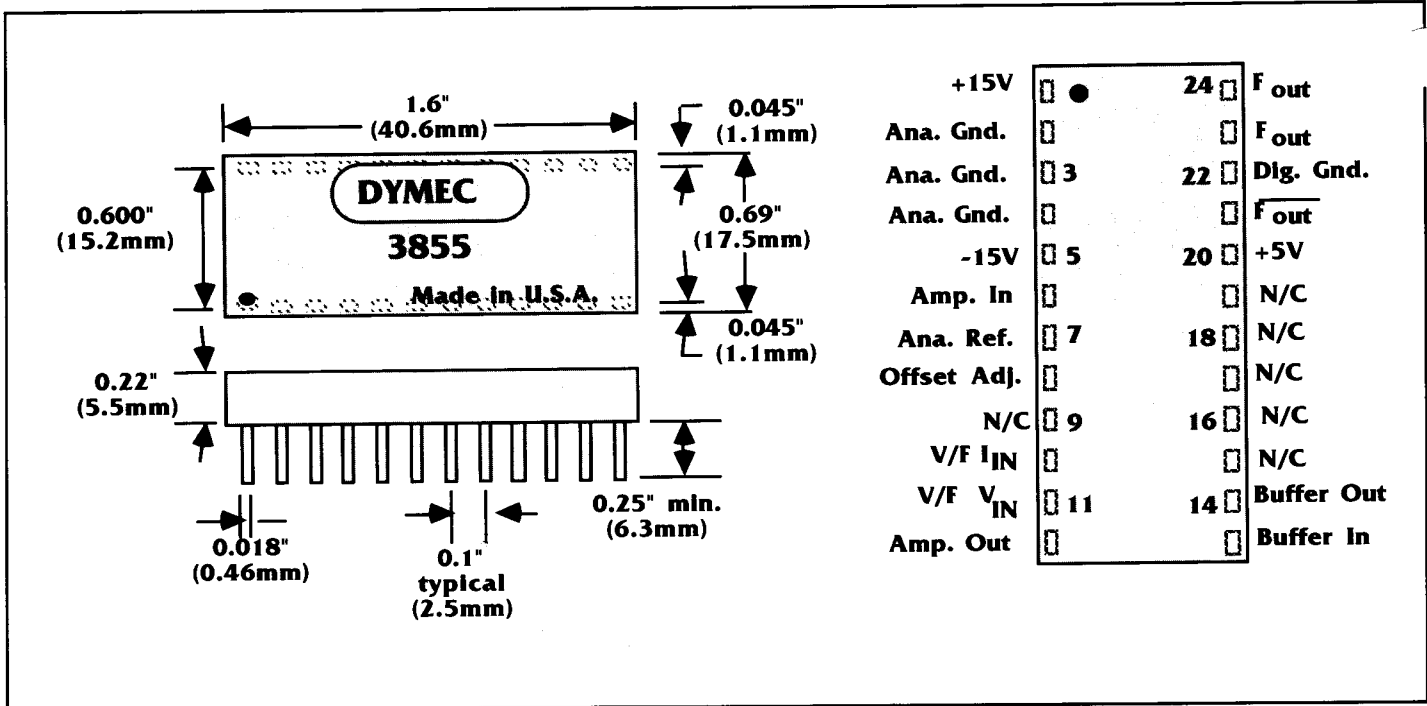
N/C Pins

Pins marked as N/C (no connection) have no electrical connection to the internal circuitry of the 3855.

Frequency Outputs

Pins 23 and 24 are tied together internally to the 3855. Either or both may be used as the source of the frequency output of the 3855 as long as the 10 LSTTL and 50pF load limits are not exceeded. Pin 21 provides an inverted signal relative to pins 23 and 24 with the same load limits.

Mechanical Dimensions & Pinout



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