300-mA 40-V LOW-DROPOUT REGULATOR WITH 25-µA QUIESCENT CURRENT

Check for Samples: TPS7A6033-Q1, TPS7A6050-Q1

FEATURES

- Low Dropout Voltage
  - 300mV at I_{OUT} = 150mA
- 4-V to 40-V Wide Input Voltage Range With up to 45-V Transients
- 300-mA Maximum Output Current
- Ultra Low Quiescent Current
  - $I_{QUIESCENT}$ = 25 µA (Typ) at Light Loads
  - I_{SLEEP} < 2µA when EN = Low
- 3.3-V and 5-V Fixed Output Voltage
- Low-ESR Ceramic Output Stability Capacitor
- Integrated Power-On Reset
  - Programmable Delay
  - Open-Drain Reset Output
- Integrated Fault Protection
  - Short-Circuit/Over-Current Protection
  - Thermal Shutdown
- Low Input Voltage Tracking
- Thermally Enhanced Power Package
  - 5-pin TO-263 (KTT /D2PAK)
  - 5-pin TO-252 (KVU /DPAK)

APPLICATIONS

- Qualified for Automotive Applications
- Infotainment Systems with Sleep Mode
- Body Control Modules
- Always ON Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

DESCRIPTION

The TPS7A60xx/TPS7A61xx is a series of low dropout linear voltage regulators designed for low power consumption and quiescent current less than 25 µA in light load applications. These devices feature an integrated over current protection and are designed to achieve stable operation even with low-ESR ceramic capacitors. Power-On Reset delay is implemented during device start up to indicate that the output voltage is stable and in regulation. The Power-On Reset delay is fixed (250 µs typical), and can also be programmed by an external capacitor. Low voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, these devices are well suited in power supplies for various automotive applications.

TYPICAL REGULATOR STABILITY

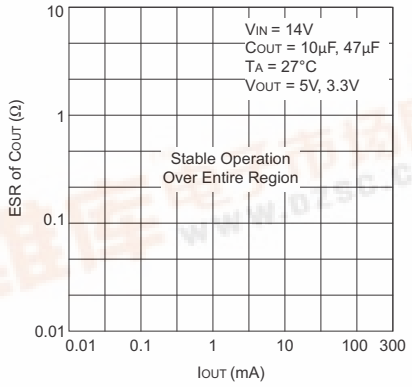


Figure 1. ESR vs Load Current for TPS7A60/1xx

TYPICAL APPLICATION SCHEMATIC

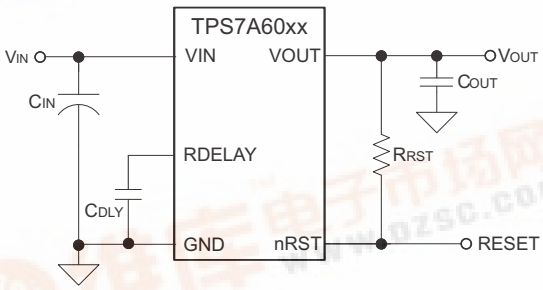


Figure 2. Programmable Reset Delay Option

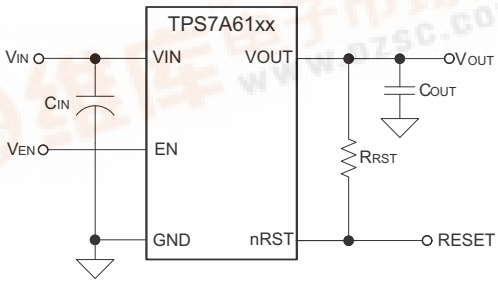


Figure 3. Enable Option

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION(1)

KEY FEATURE	OUTPUT VOLTAGE	PACKAGE		ORDERABLE PART NUMBER(2)	TOP-SIDE MARKING
Programable Reset Delay	5V	5 pin KTT	Reel of 500	TPS7A6050QKTTRQ1	7A6050Q1
		5 pin KVU	Tube of 70	TPS7A6050QKVUQ1	7A6050Q1
			Reel of 2500	TPS7A6050QKVURQ1	Product Preview
	3.3V	5 pin KTT	Reel of 500	TPS7A6033QKTTRQ1	7A6033Q1
		5 pin KVU	Reel of 2500	TPS7A6033QKVURQ1	Product Preview
Enable	5V	5 pin KTT	Reel of 500	TPS7A6150QKTTRQ1	Product Preview
		5 pin KVU	Reel of 2500	TPS7A6150QKVURQ1	Product Preview
	3.3V	5 pin KTT	Reel of 500	TPS7A6133QKTTRQ1	Product Preview
		5 pin KVU	Reel of 2500	TPS7A6133QKVURQ1	Product Preview

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

NO.	DESCRIPTION		VALUE	UNIT
1.1	V_{IN}, V_{EN}	Unregulated inputs(2)(3)	45	V
1.2	V_{OUT}	Regulated output	7	V
1.3	nRST	Open drain reset output(2)	7	V
1.4	RDELAY	Output to charge an external cpacitor(2)	7	V
1.5	θ_{JP}	Thermal impedance junction to exposed pad KTT (D2PAK) package	10.4	°C/W
		Thermal impedance junction to exposed pad KVU (DPAK) package	12.7	°C/W
1.6	θ_{JA}	Thermal impedance junction to ambient KTT (D2PAK) package(4)	30.2	°C/W
		Thermal impedance junction to ambient KVU (DPAK) package(4)	29.3	°C/W
1.7	θ_{JA}	Thermal impedance junction to ambient KTT (D2PAK) package (5)	34.4	°C/W
		Thermal impedance junction to ambient KVU (DPAK) package(5)	38.6	°C/W
1.8	ESD	Electrostatic discharge(6)	2	kV
1.9	T_{OP}	Operating ambient temperature	125	°C
1.10	T_S	Storage temperature range	-65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute negative voltage on these pins not to go below –0.3V.
(3) Absolute maximum voltage for duration less than 480ms.
(4) The thermal data is based on JEDEC standard high K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(5) The thermal data is based on JEDEC standard low K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(6) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

DISSIPATION RATINGS

NO.	JEDEC STANDARD	PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (°C/W)	T_A = 85°C POWER RATING (W)
2.1	JEDEC Standard PCB - low K, JESD 51-3	5 pin KTT	3.63	34.4	1.89
2.2		5 pin KVU	3.24	38.6	1.68
2.3	JEDEC Standard PCB - high K, JESD 51-5	5 pin KTT	4.14	30.2	2.15
2.4		5 pin KVU	4.27	29.3	2.22

RECOMMENDED OPERATING CONDITIONS

NO.	DESCRIPTION		MIN	MAX	UNIT
3.1	V_{IN}, V_{EN} (1)	Unregulated input voltage	4	40	V
3.2	nRST, RDELAY (2)	Low voltage input/output	0	5.25	V
3.3	T_J	Operating junction temperature range	-40	150	°C

(1) Applicable for TPS7A61xx only.
(2) Applicable for TPS7A60xx only.

ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4. Input Voltage (VIN pin)							
4.1	V_{IN}	Input voltage	Fixed 5V output, I_{OUT} = 1mA	5.3		40	V
			Fixed 3.3V output, I_{OUT} = 1mA	4		40	
4.2	$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2V to 18V, V_{EN} (1) = 5V, I_{OUT} = 0.01mA to 0.75mA		25	40	µA
4.3	I_{SLEEP} (1)	Sleep/shutdown current	V_{IN} = 8.2V to 18V, V_{EN} (1) < 0.8V, I_{OUT} = 0mA (no load), T_A = 125°C			3	µA
4.4	$V_{IN-UVLO}$	Under voltage lock out voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
4.5	$V_{IN(POWERUP)}$	Power up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
5. Enable Input (EN pin)							
5.1	V_{IL} (1)	Logic input low level		0		0.8	V
5.2	V_{IH} (1)	Logic input high level		2.5		40	V
6. Regulated Output Voltage (VOUT pin)							
6.1	V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3V or 5V as applicable), I_{OUT} = 10mA	-2		2	%
6.2	$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 5V			15	mV
			V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 3.3V			20	mV
6.3	$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10mA to 300mA, V_{IN}= 14V, V_{OUT} = 5V			25	mV
			I_{OUT} = 10mA to 300mA,V_{IN} = 14V, V_{OUT} = 3.3V			35	mV
6.4	$V_{DROPOUT}$ (2)	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 250mA			500	mV
			I_{OUT} = 150mA			300	mV
6.5	R_{SW} (3)	Switch resistance	VIN to VOUT resistance			2	Ω
6.6	I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
6.7	I_{CL}	Output current limit	V_{OUT} = 0V (VOUT pin is shorted to ground)	350		1000	mA
6.8	PSRR (3)	Power supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300mA, frequency = 100 Hz, V_{OUT} = 5V and V_{OUT} = 3.3V		60		dB
			$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300mA, frequency = 150 kHz, V_{OUT} = 5V and V_{OUT} = 3.3V		30		

(1) Applicable for TPS7A61xx only.
(2) This test is done with V_{OUT} in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} (3.3V or 5.0V) drops by 100mV at specified loads.
(3) Specified by design – not tested

ELECTRICAL CHARACTERISTICS (continued)

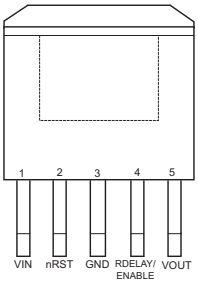
V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7. Reset (nRST pin)							
7.1	V_{OL}	Reset pulled low	I_{OL} = 5mA			0.4	V
7.2	I_{OH}	Leakage current	Reset pulled to VOUT through 5kΩ resistor			1	µA
7.3	$V_{TH(POR)}$	Power-On Reset threshold	V_{OUT} power up above internally set tolerance, V_{OUT} = 5V	4.5	4.65	4.77	V
			V_{OUT} power up above internally set tolerance, V_{OUT} = 3.3V		3.07		
7.4	UV_{THRES}	Reset threshold	V_{OUT} falling below internally set tolerance, V_{OUT} = 5V	4.5	4.65	4.77	V
			V_{OUT} falling below internally set tolerance, V_{OUT} = 3.3V		3.07		
7.5	t_{POR} (4)	Power-On Reset delay	C_{DLY} = 100pF		300		µs
			C_{DLY} = 100nF		300		ms
7.6	$t_{POR-PRESET}$	Internally preset Power-On Reset delay	C_{DLY} not connected in TPS7A60xx/ not available in TPS7A61xx, V_{OUT} = 5V and V_{OUT} = 3.3V		250		µs
7.7	$t_{DEGLITCH}$	Reset deglitch time			5.5		µs
8. Reset Delay (RDELAY pin)							
8.1	$V_{TH(RDELAY)}$ (5)	Threshold to release nRST high	Voltage at RDELAY pin is ramped up		3	3.3	V
8.2	I_{DLY} (5)	Delay capacitor charging current		0.75	1	1.25	µA
8.3	I_{OL} (5)	Delay capacitor discharging current	Voltage at RDELAY pin = 1V	5			mA
9. Operating Temperature Range							
9.1	T_J	Operating junction temperature		-40		150	ºC
9.2	$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
9.3	T_{HYST}	Thermal shutdown hysteresis			10		ºC

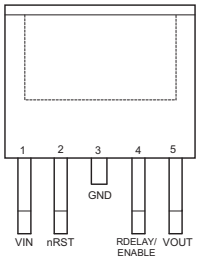
(4) Design Information – not tested; specified by characterization
(5) Applicable for TPS7A60xx only.

DEVICE INFORMATION

KTT PACKAGE
(TOP VIEW)



KVU PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NO.	NAME	TYPE	DESCRIPTION
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	nRST	O	Reset pin: This is an output pin with an external pull up resistor connected to VOUT pin.
3	GND	I/O	Ground pin: This is signal ground pin of the IC.
4	RDELAY	O	Reset delay timer pin (for TPS7A60xx only): This pin is used to program the reset delay timer using an external capacitor (C_{DLY}) to ground.
	EN	I	Enable pin (for TPS7A61xx only): This is a high voltage tolerant input pin with an internal pull down. A high input to this pin activates the device and turns the regulator ON. This input can be connected to VIN terminal for self bias applications. If this pin is not connected, the device will stay disabled.
5	VOUT	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3V or 5V, as applicable) pin with a limitation on maximum output current. In order to achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and GND pin.

FUNCTIONAL BLOCK DIAGRAM

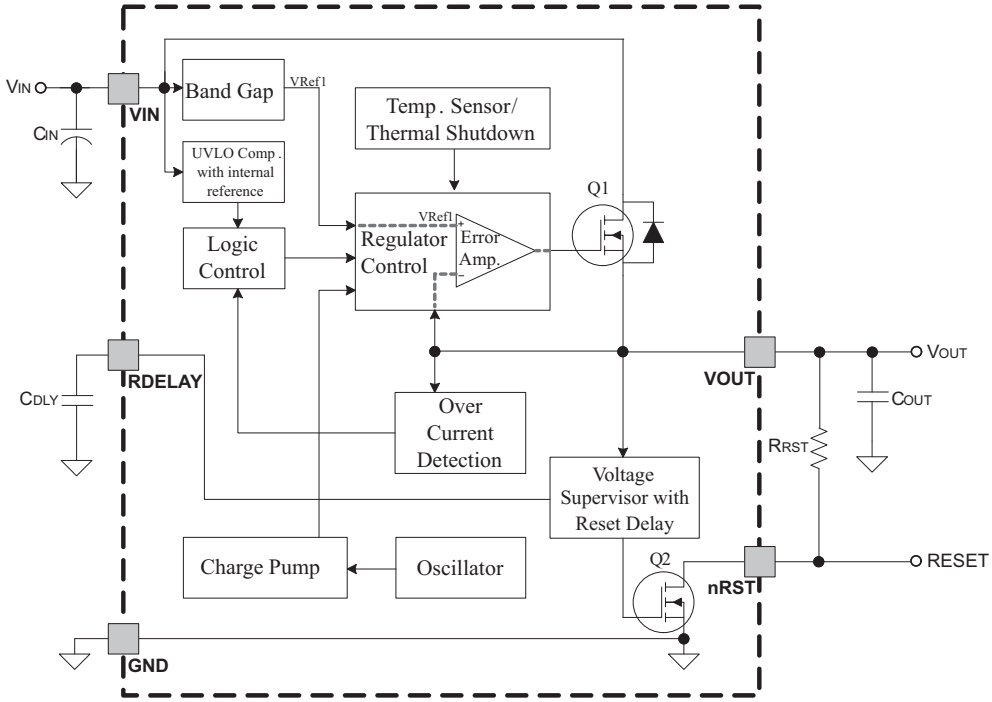


Figure 4. TPS7A60xx Functional Block Diagram

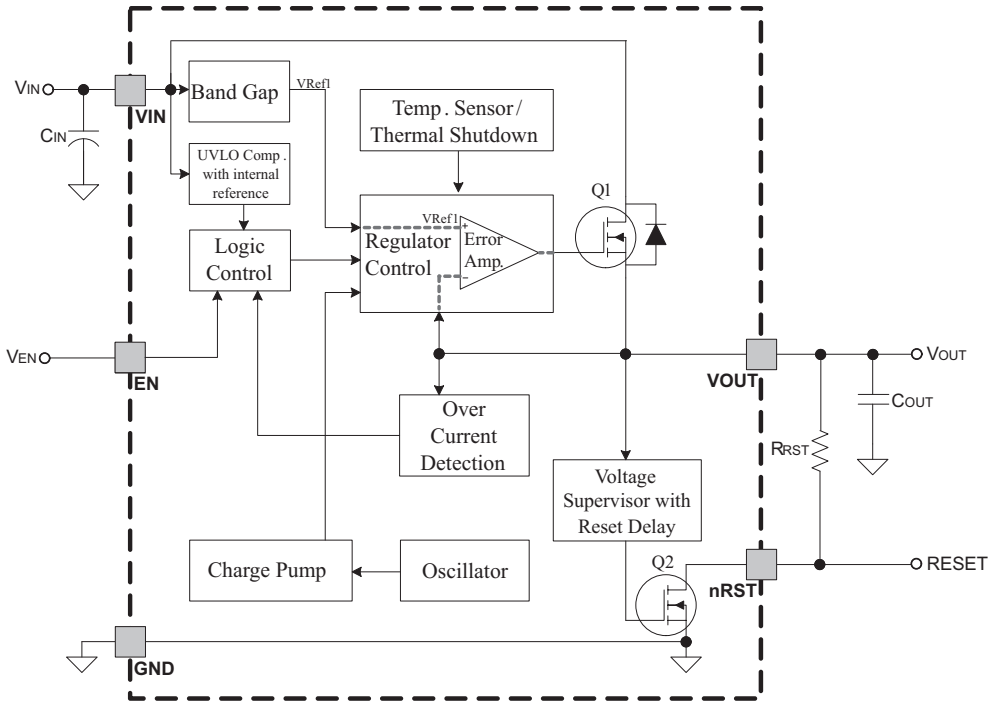
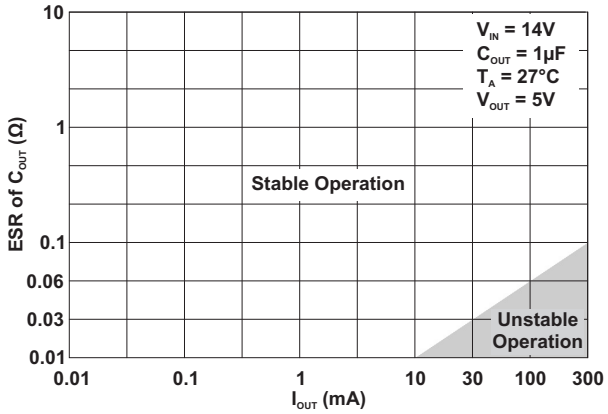


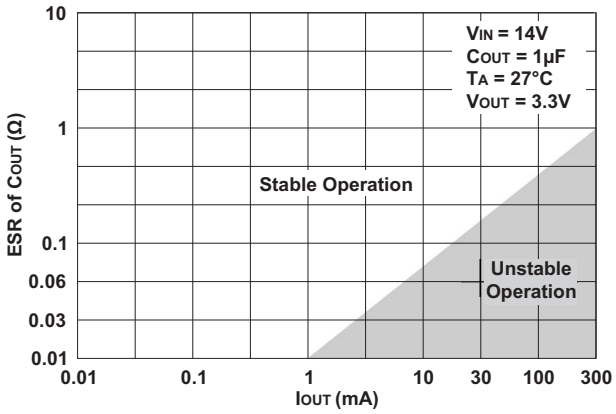
Figure 5. TPS7A61xx Functional Block Diagram

TYPICAL CHARACTERISTICS

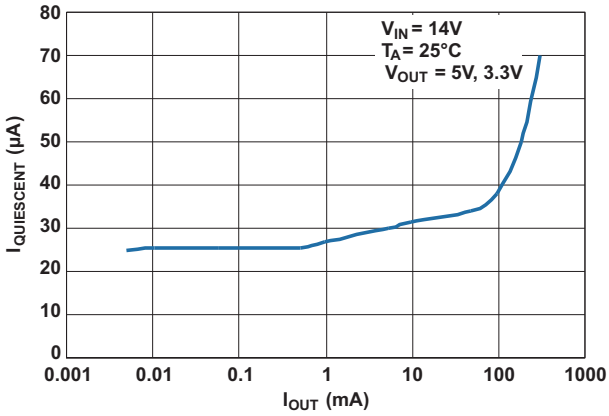
ESR vs LOAD CURRENT



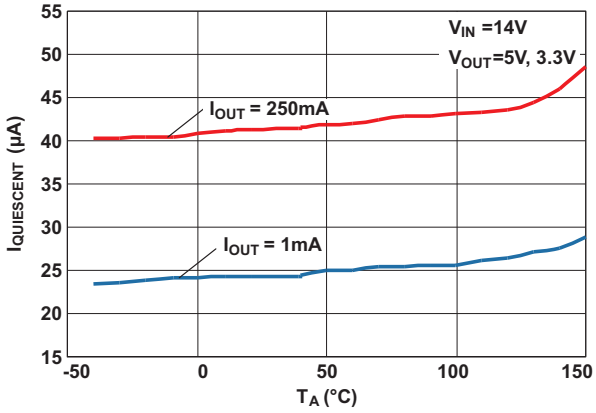
ESR vs LOAD CURRENT



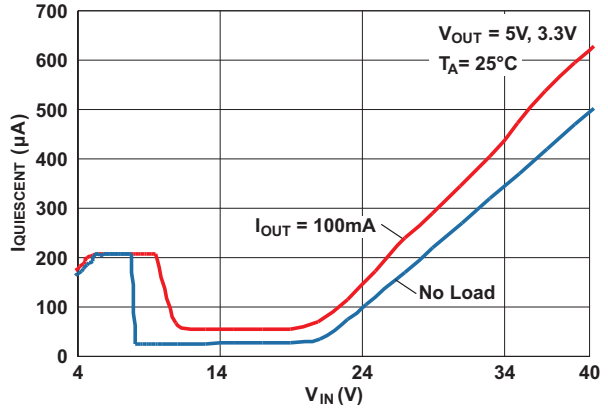
QUIESCENT CURRENT vs LOAD CURRENT



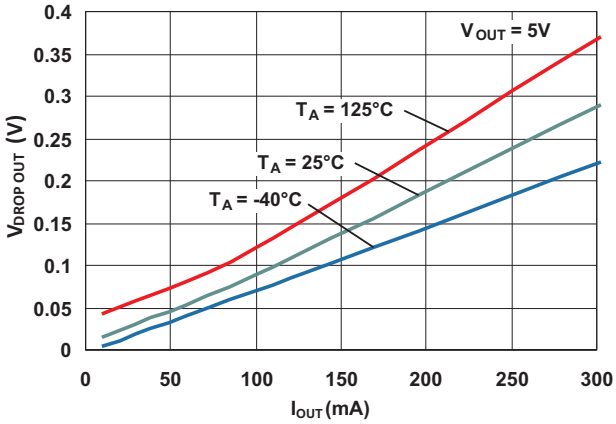
QUIESCENT CURRENT vs AMBIENT AIR TEMPERATURE



QUIESCENT CURRENT vs INPUT VOLTAGE



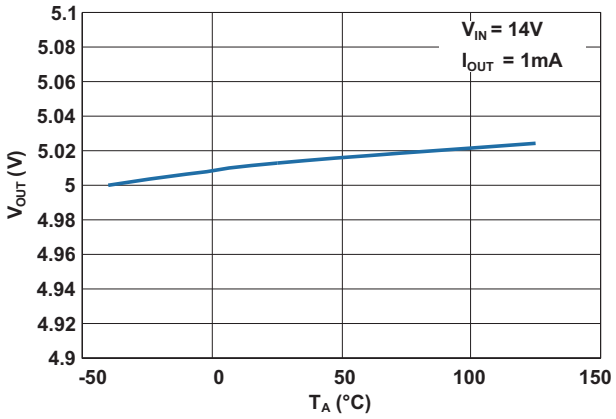
DROP OUT VOLTAGE(1) vs LOAD CURRENT



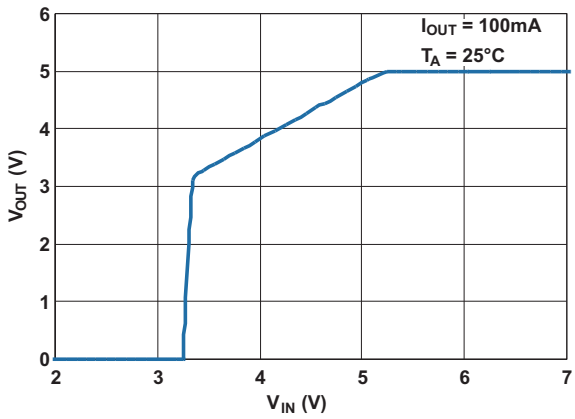
(1) Drop out voltage is measured when the output voltage drops by 100mV from the regulated output voltage level. (For example, drop out voltage for TPS7A6050 is measured when the output voltage drops down to 4.9V from 5V.)

TYPICAL CHARACTERISTICS (continued)

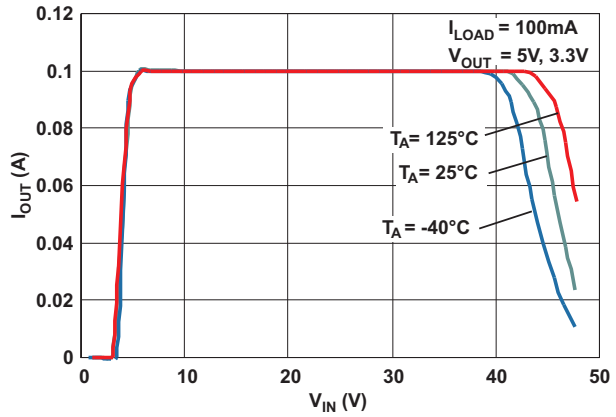
OUTPUT VOLTAGE vs AMBIENT AIR TEMPERATURE



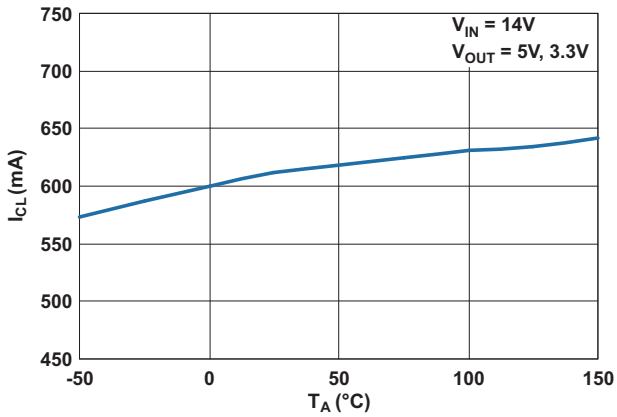
OUTPUT VOLTAGE vs INPUT VOLTAGE



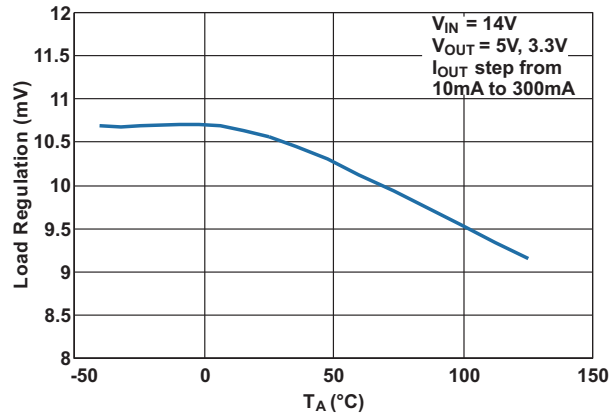
OUTPUT CURRENT vs INPUT VOLTAGE



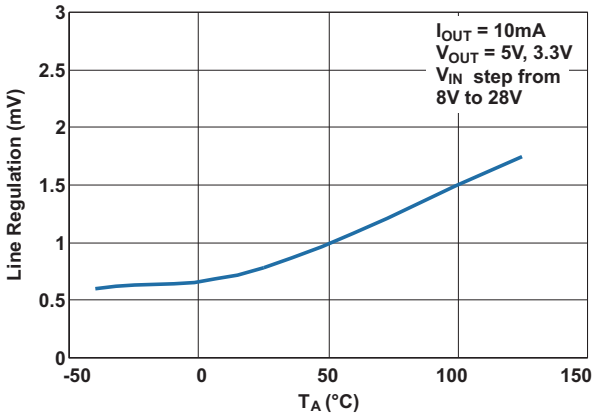
OUTPUT CURRENT LIMIT vs AMBIENT AIR TEMPERATURE



LOAD REGULATION vs AMBIENT AIR TEMPERATURE

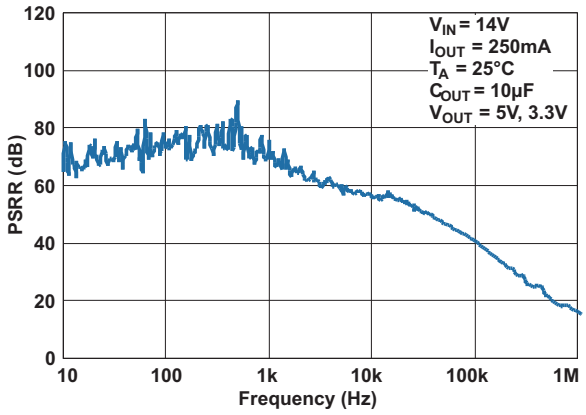


LINE REGULATION vs AMBIENT AIR TEMPERATURE

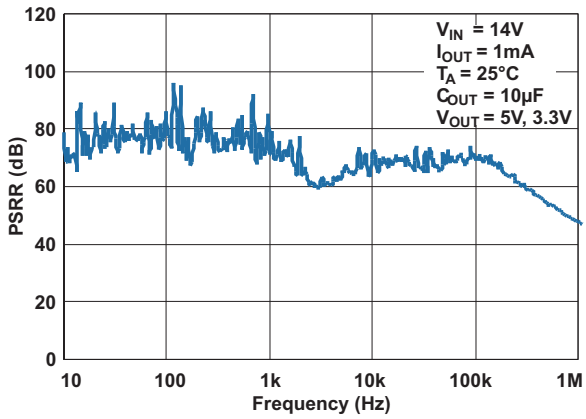


TYPICAL CHARACTERISTICS (continued)

PSRR AT HEAVY LOAD CURRENT



PSRR AT LIGHT LOAD CURRENT



Note: Graphs shown in 'Typical Characteristics' section for unreleased devices are for preview only.

DETAILED DESCRIPTION

TPS7A60/1xx is a series of monolithic low dropout linear voltage regulators with integrated reset functionality. These voltage regulators are designed for low power consumption and quiescent current less than 25µA in light load applications. Because of an integrated reset delay (also called Power-On Reset delay), these devices are well suited in power supplies for microprocessors/ microcontrollers.

These devices are available in two fixed output voltage (3.3V and 5V) versions as follows:

- Programmable reset delay version (TPS7A60xx)
- Enable version (TPS7A61xx)

The following section describes the features of TPS7A60/1xx voltage regulators in detail.

Reset Delay and Reset Output

Reset delay is implemented when the device starts up to indicate that output voltage is stable and in regulation, and also when the output recovers from a negative voltage spike due to a load step or a dip in the input voltage for a specified duration. Reset delay timer is initialized when the voltage at output (V_{OUT}) exceeds 93% of the regulated output voltage (3.3V or 5V, as applicable). The reset output (nRST) is asserted high after Power-On Reset delay (t_{POR}) has elapsed. If the regulated output voltage falls below 93% of the set level, nRST is asserted low after a short de-glitch time of approximately 5.5µs (typical).

For TPS7A60xx devices, reset delay time can be programmed by connecting an external capacitor (C_{DLY}) to RDELAY pin. The delay time is given by Equation 1:

$$t_{POR} = \frac{CDLY \times 3}{1 \times 10^{-6}} \quad (1)$$

Where,

t_{POR} = reset delay time in seconds

C_{DLY} = reset delay capacitor value in farads, 100 pF to 100 nF

In TPS7A61xx devices, there is no RDELAY pin and reset delay time is preset internally (250µs typical).

During power up, the regulator incorporates a protection scheme to limit the current through pass element and output capacitor. When the input voltage exceeds a certain threshold ($V_{IN(POWERUP)}$) level, the output voltage begins to ramp as shown in Figure 6 and Figure 7. When the output voltage reaches power on reset threshold ($V_{TH(POR)}$) level, a constant output current charges an external capacitor (C_{DLY}) to an internal threshold ($V_{TH(RDELAY)}$) voltage level. Then, nRST is asserted high and C_{DLY} is discharged through an internal load. This allows C_{DLY} to charge from approximately 0V during the next power cycle. If no external capacitor is connected, the delay time is preset internally. This is shown in Figure 6.

In TPS7A60xx devices, if C_{DLY} capacitor is not connected to RDELAY pin, reset delay time is set internally. This is shown in Figure 7.

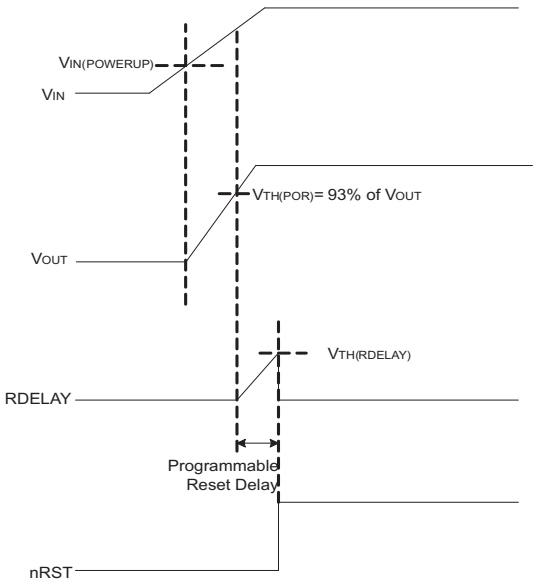


Figure 6. Power Up and Reset Delay Function with C_{DLY} Capacitor connected to RDELAY Pin for TPS7A60xx

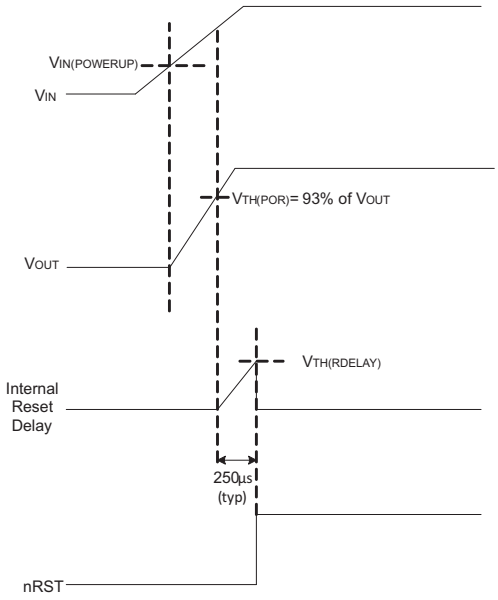


Figure 7. Power Up and Reset Delay Function with C_{DLY} Capacitor not connected/available in TPS7A60xx/TPS7A61xx respectively

In case of negative transients in the input voltage (V_{IN}), the reset signal will be asserted low only if the output (V_{OUT}) drops and stays below the reset threshold level ($V_{TH(POR)}$) for more than deglitch time ($t_{DEGLITCH}$). This is shown in Figure 8.

While nRST is low, if the input voltage resumes to the nominal operating voltage, normal power up sequence will be followed. nRST will be asserted high, only if the output voltage exceeds the reset threshold voltage ($V_{TH(POR)}$) and the reset delay time (t_{POR}) has elapsed. This is shown in the shaded region of Figure 8.

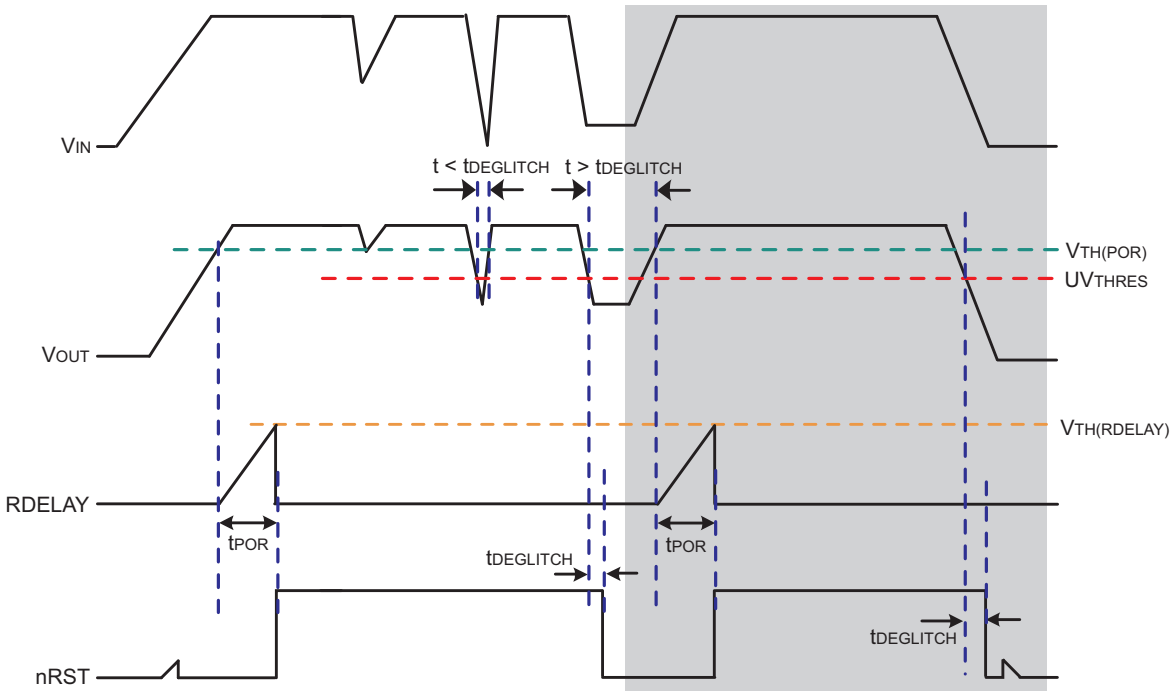


Figure 8. Conditions for Activation of Reset

Charge Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry shall not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. Figure 9 and Figure 10 shows typical switching thresholds for the charge pump at light (I_{OUT} < ~2mA) and heavy (I_{OUT} > ~2mA) loads respectively.

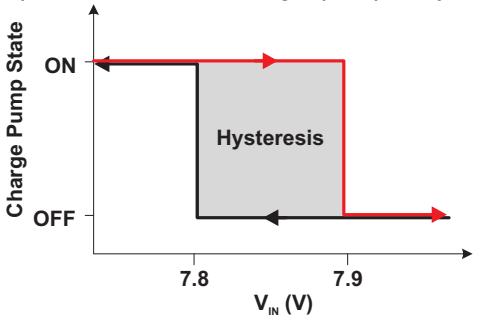


Figure 9. Charge Pump Operation at Light Loads

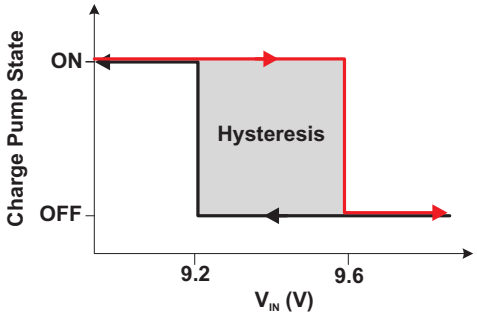


Figure 10. Charge Pump Operation at Heavy Loads

Low Power Mode

At light loads and high input voltages (V_{IN}>~8V such that charge pump is off) the device operates in Low Power Mode and the quiescent current consumption is reduced to 25µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < ~2mA (Light load)	250 µA	25 µA (Low Power Mode)
I_{OUT} > ~2mA (Heavy load)	280 µA	70 µA

Under Voltage Shutdown

These devices have an integrated under voltage lock out (UVLO) circuit to shutdown the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$). This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds $V_{IN(POWERUP)}$ level.

Low Voltage Tracking

At low input voltages the regulator drops out of regulation, the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions.

Integrated Fault Protection

These devices feature an integrated fault protection to make them ideal for use in automotive applications. In order to keep them in safe area of operation during certain fault conditions, internal current limit protection and current limit fold back are used to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short circuit condition on the output; current through the pass element is limited to I_{CL} to protect the device from excessive power dissipation.

Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed TSD trip point. If the junction temperature exceeds TSD trip point, the output is turned off. When the junction temperature falls below TSD trip point, the output is turned on again. This is shown in Figure 11.

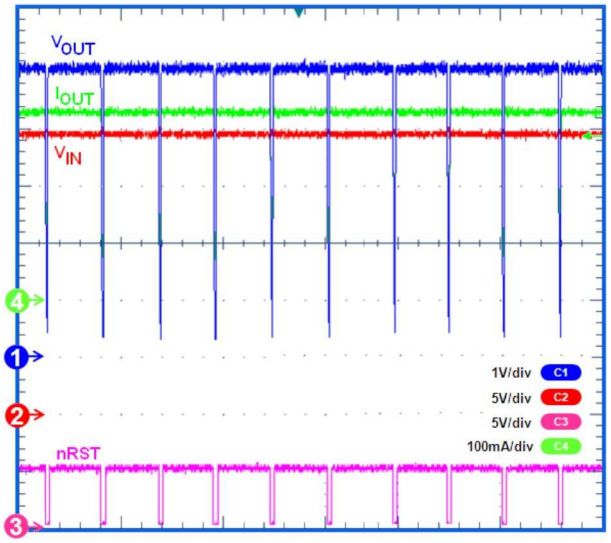


Figure 11. Thermal Cycling Waveform for TPS7A6050 (V_{IN} = 24 V, I_{OUT} = 300 mA, V_{OUT} = 5 V)

APPLICATION INFORMATION

Typical application circuits for TPS7A60xx and TPS7A61xx are shown in Figure 12 and Figure 13 respectively. Depending upon an end application, different values of external components may be used. A larger output capacitor may be required during fast load steps in order to prevent reset from occurring. A low ESR ceramic capacitor with dielectric of type X5R or X7R is recommended. Additionally, a bypass capacitor can be connected at the output to decouple high frequency noise as per the end application.

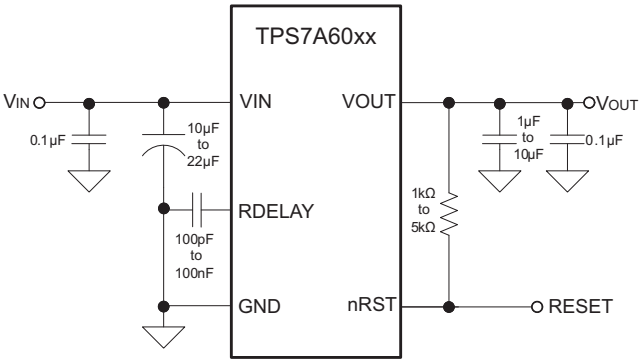


Figure 12. Typical Application Schematic for TPS7A60xx

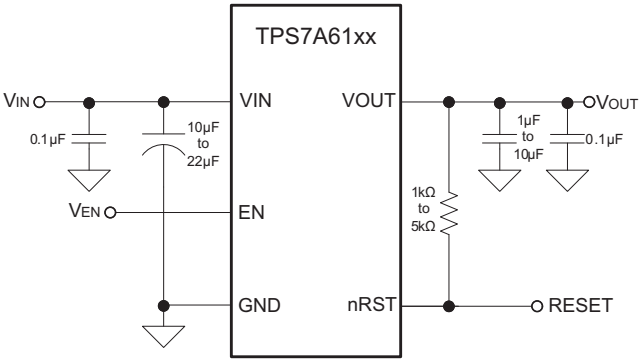


Figure 13. Typical Application Schematic for TPS7A61xx

Power Dissipation and Thermal Considerations

Power dissipated in the device can be calculated using Equation 2.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN} \quad (2)$$

Where,

P_D = continuous power dissipation
I_{OUT} = output current
V_{IN} = input voltage
V_{OUT} = output voltage
$I_{QUIESCENT}$ = quiescent current

As $I_{QUIESCENT}$ << I_{OUT}, therefore, the term $I_{QUIESCENT} \times V_{IN}$ in Equation 2 can be ignored.

For device under operation at a given ambient air temperature (T_A), the junction temperature (T_J) can be calculated using Equation 3.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (3)$$

Where,

θ_{JA} = junction to ambient air thermal impedance

The rise in junction temperature due to power dissipation can be calculated using Equation 4.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (4)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate can be calculated using Equation 5.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (\theta_{JA} \times P_D) \quad (5)$$

Example

If I_{OUT} = 100mA, V_{OUT} = 5V, V_{IN} = 14V, $I_{QUIESCENT}$ = 250µA and θ_{JA}= 30˚C/W, the continuous power dissipated in the device is 0.9W. The rise in junction temperature due to power dissipation is 27˚C. For a maximum junction temperature of 150˚C, maximum ambient air temperature at which the device can operate is 123˚C.

For adequate heat dissipation, it is recommended to solder the power pad (exposed heat sink) to thermal land pad on the PCB. Doing this provides a heat conduction path from die to the PCB and reduces overall package thermal resistance. Power derating curves for TPS7A60/1xx series of devices in KTT(D2PAK) and KVU(DPAK) packages are shown in Figure 14.

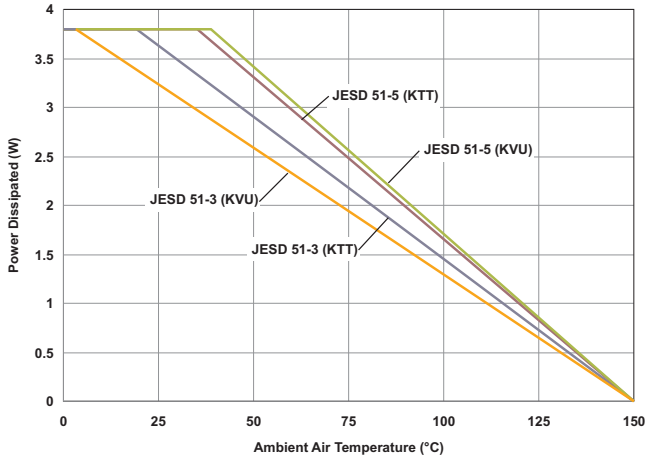


Figure 14. Power Derating Curves

For optimum thermal performance, it is recommended

to use a high K PCB with thermal vias between ground plane and solder pad/ thermal land pad. This is shown in Figure 15 (a) and (b). Further, heat spreading capabilities of a PCB can be considerably improved by using a thicker ground plane and a thermal land pad with a larger surface area.

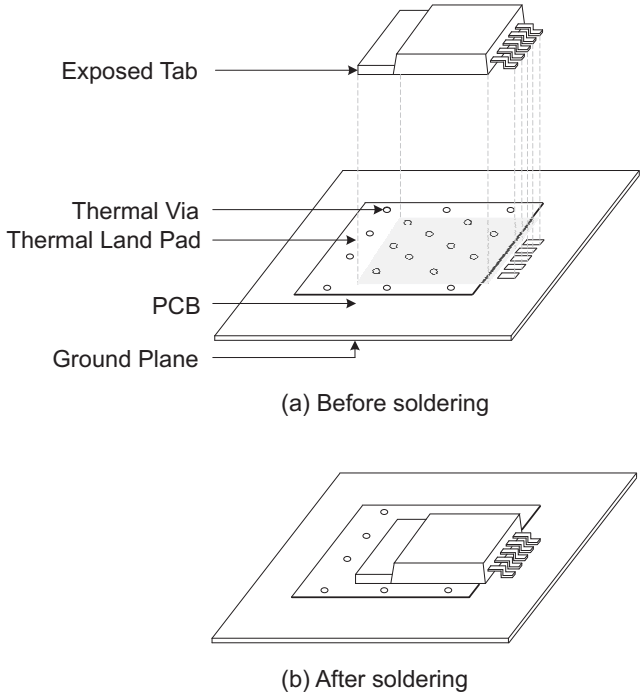


Figure 15. Using Multilayer PCB and Thermal Vias For Adequate Heat Dissipation

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 16 shows variation of θ_{JA} with surface area of the thermal land pad (soldered to the exposed pad) for KTT and KVU packages.

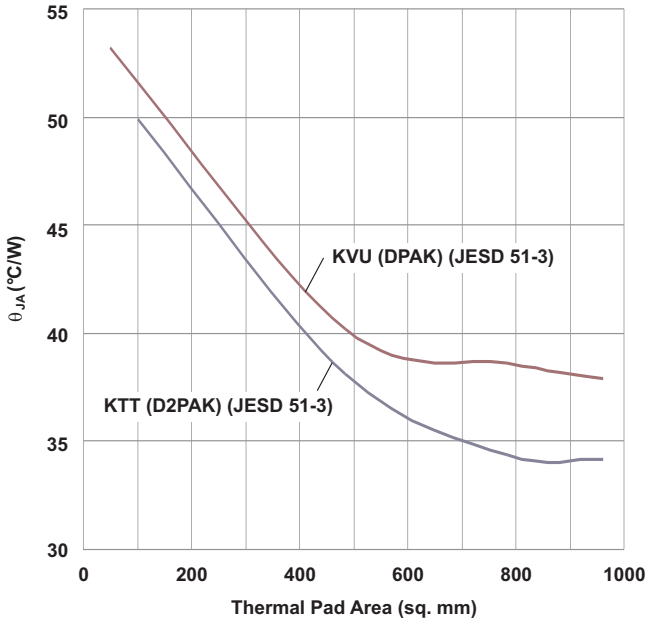


Figure 16. θ_{JA} vs Thermal Pad Area

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TPS7A6033QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245
TPS7A6033QKVURQ1	ACTIVE	PFM	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260
TPS7A6050QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245
TPS7A6050QKVUQ1	ACTIVE	PFM	KVU	5	70	Green (RoHS & no Sb/Br)	CU SN	Level-3-260
TPS7A6050QKVURQ1	ACTIVE	PFM	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260
TPS7A6133QKTTRQ1	PREVIEW	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI
TPS7A6133QKVURQ1	PREVIEW	PFM	KVU	5	2500	TBD	Call TI	Call TI
TPS7A6150QKVURQ1	PREVIEW	PFM	KVU	5	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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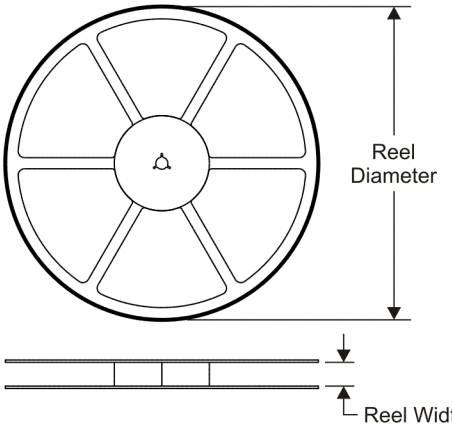
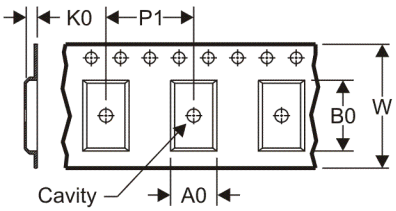
TAPE AND REEL INFORMATION

REEL DIMENSIONS

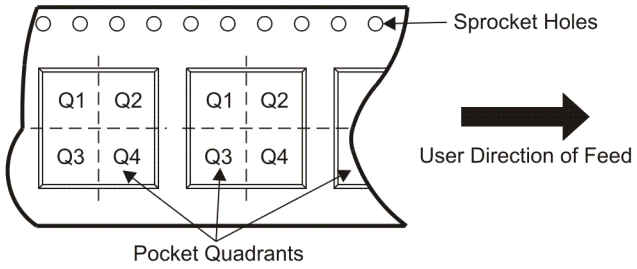


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

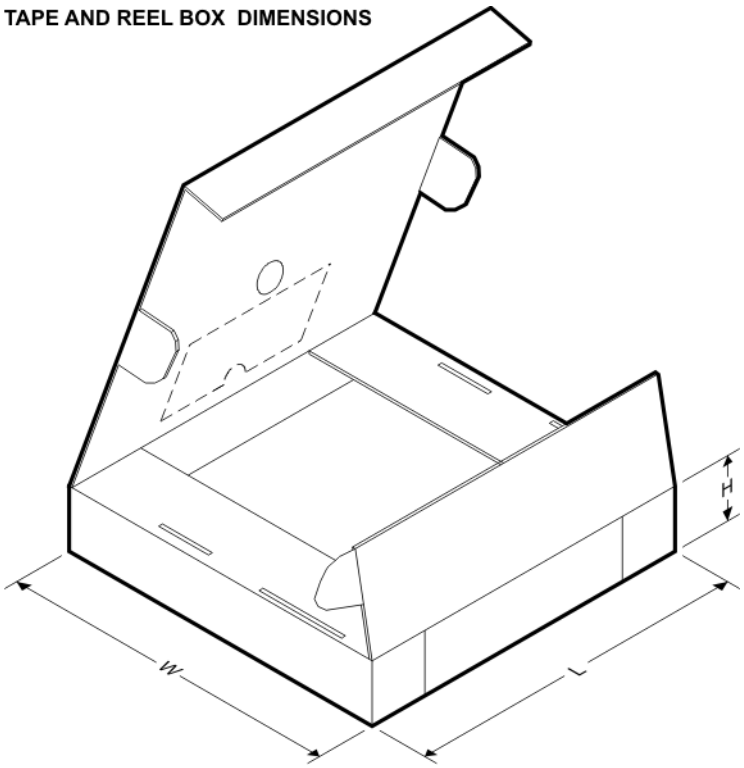
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6033QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS7A6033QKVURQ1	PFM	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6050QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS7A6050QKVURQ1	PFM	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

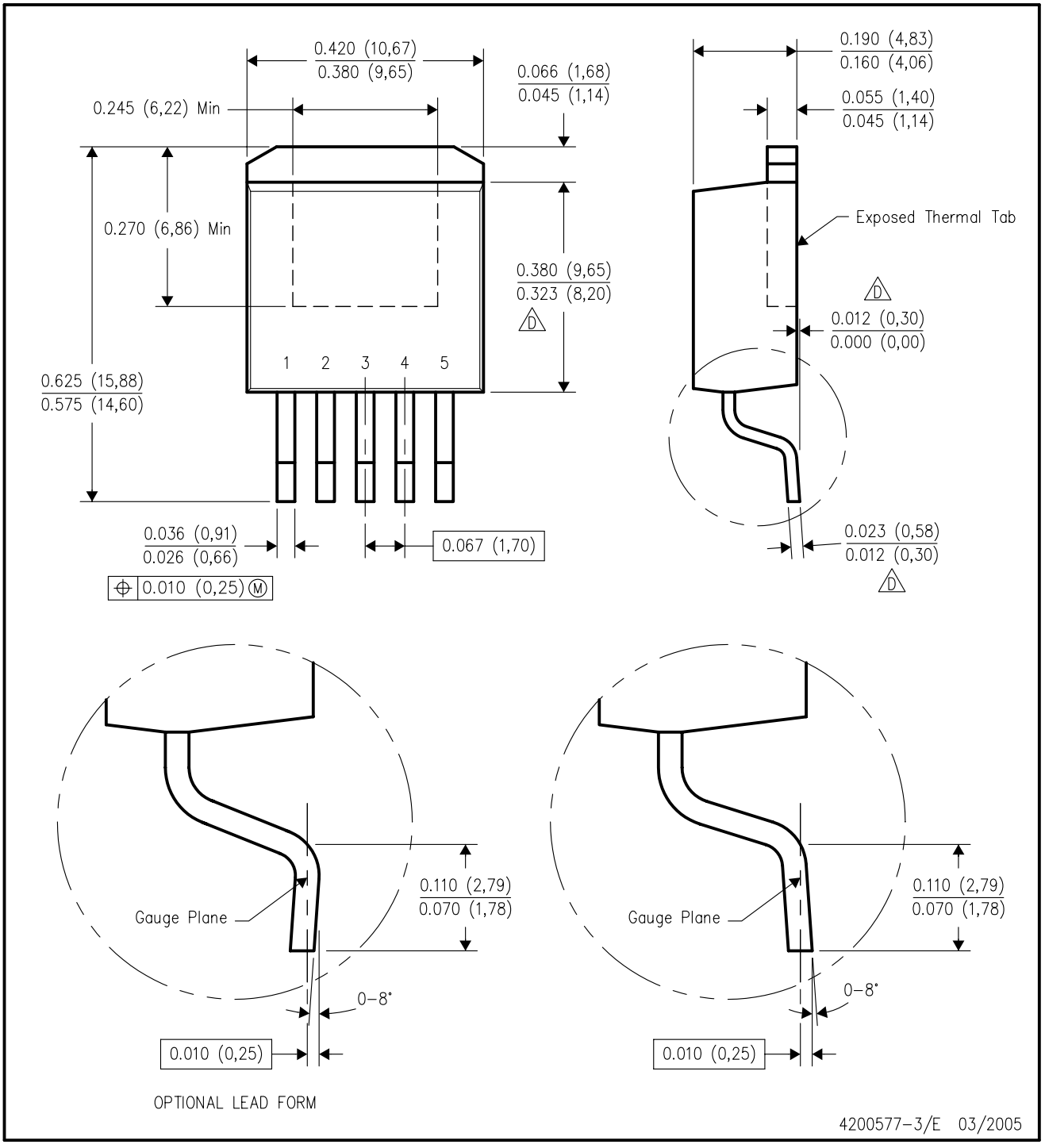
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

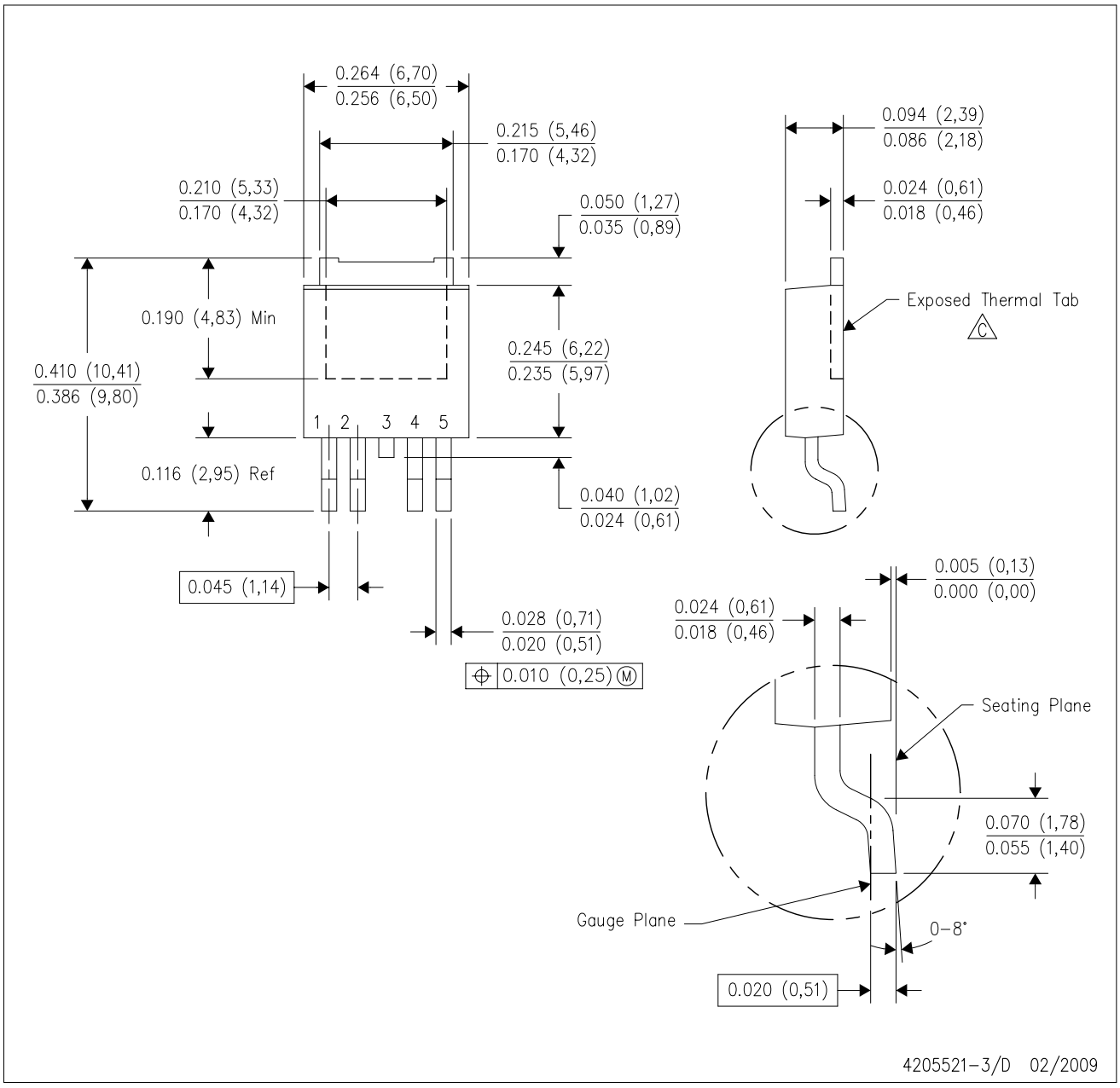
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6033QKTTRQ1	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS7A6033QKVURQ1	PFM	KVU	5	2500	530.0	340.0	70.0
TPS7A6050QKTTRQ1	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS7A6050QKVURQ1	PFM	KVU	5	2500	340.0	340.0	38.0

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

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