

## 3.3V 18-bit universal bus transceiver (3-State)

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## 74LVT16501A

### FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

### DESCRIPTION

The 74LVT16501A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and  $\overline{OEBA}$ ), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{OEBA}$ , LEBA and CPBA. The output enables are complimentary (OEAB is active High, and  $\overline{OEBA}$  is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}$ ; $V_{CC} = 3.3\text{V}$	1.9	ns
$C_{IN}$	Input capacitance (Control pins)	$V_I = 0\text{V}$ or $3.0\text{V}$	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or $3.0\text{V}$	9	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	70	$\mu\text{A}$

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT16501A DL	VT16501A DL	SOT371-1
56-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT16501A DGG	VT16501A DGG	SOT364-1

### PIN DESCRIPTION

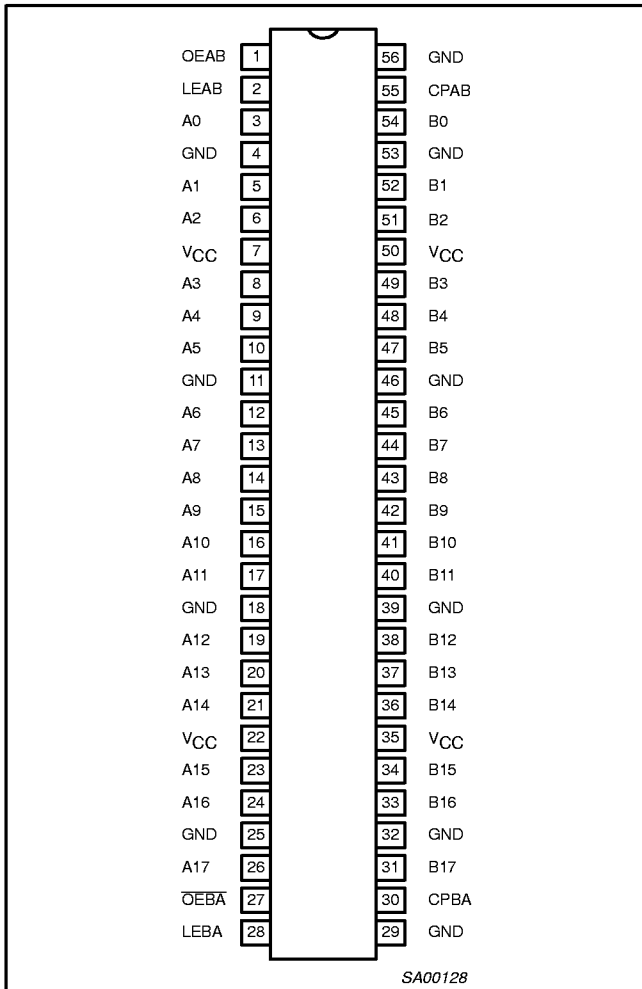
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55, 30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	$V_{CC}$	Positive supply voltage

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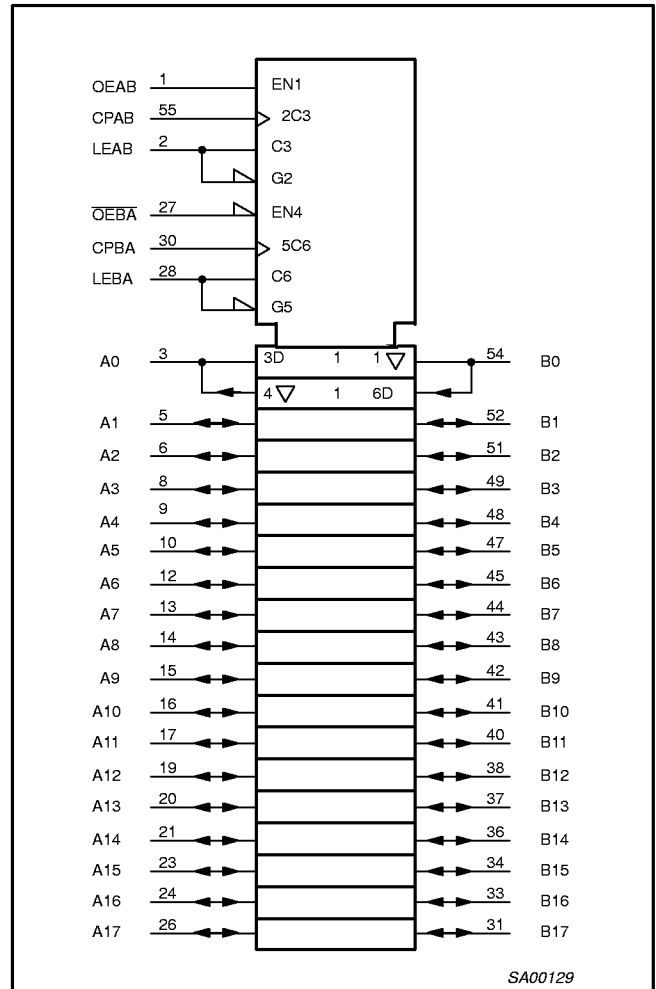
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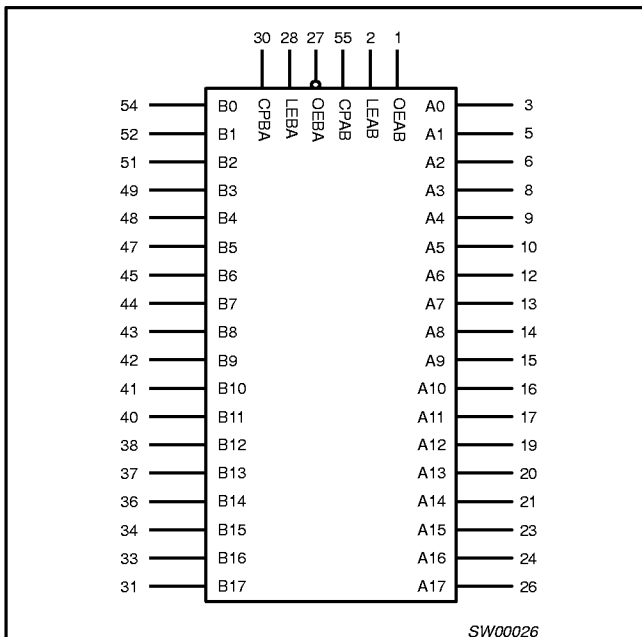
### PIN CONFIGURATION



### LOGIC SYMBOL (IEEE/IEC)



### LOGIC SYMBOL



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**FUNCTION TABLE**

INPUTS				INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

**NOTE:** A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CPBA.

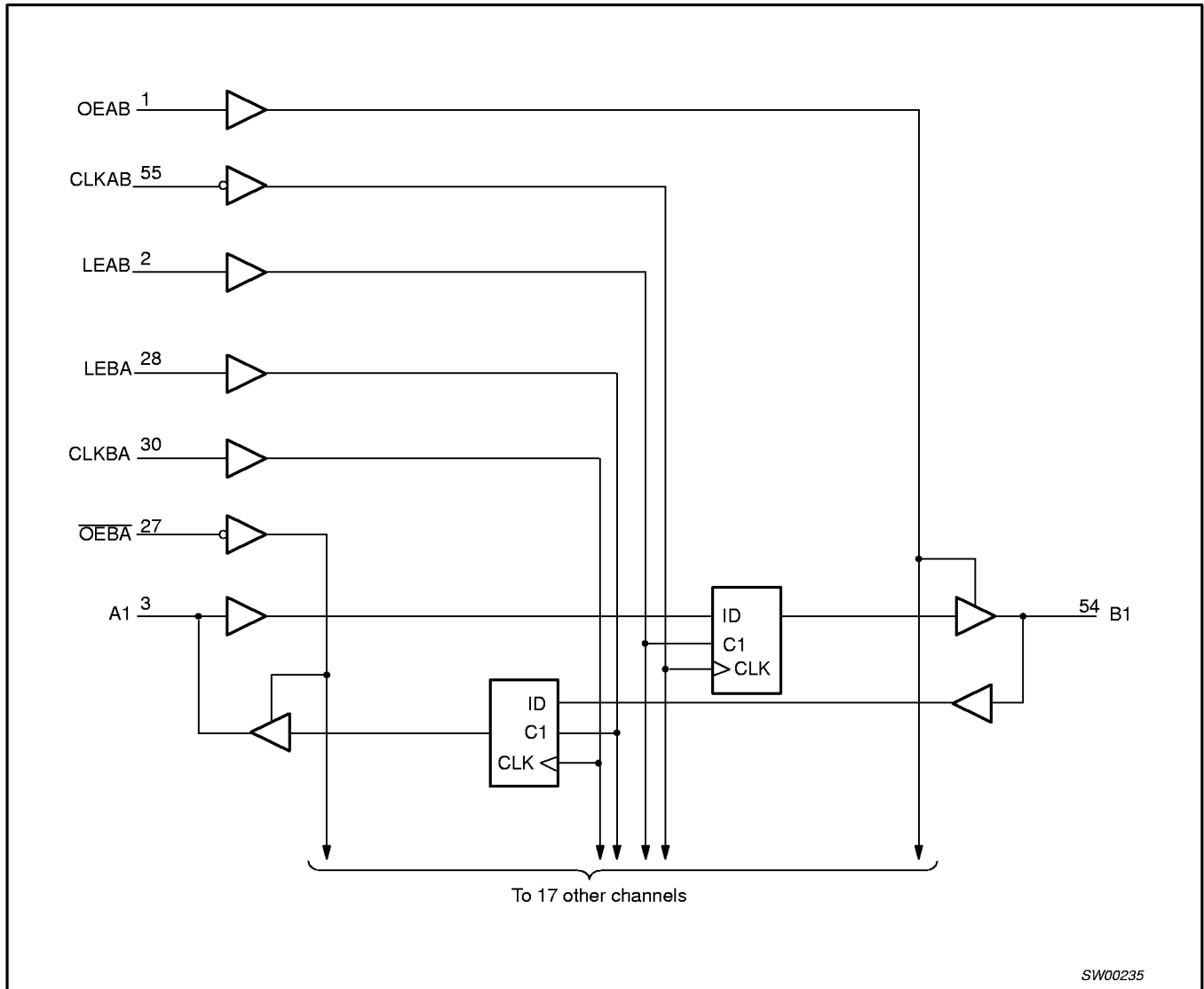
- H = High voltage level
- h = High voltage level one set-up time prior to the Enable or Clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Enable or Clock transition
- NC= No Change
- X = Don't care
- Z = High Impedence "off" state
- ↓ = High-to-Low Enable or Clock transition

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#### LOGIC DIAGRAM



## 3.3V 18-bit universal bus transceiver (3-State)

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SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

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**DC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7V; I <sub>IK</sub> = -18mA		-0.85	-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = -100µA	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -8mA	2.4	2.55		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -32mA	2.0	2.3		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100µA		0.07	0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.25	0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA		0.36	0.55	
V <sub>RST</sub>	Power-up output low voltage <sup>5</sup>	V <sub>CC</sub> = 3.6V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.1	0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	0.1	±1	µA
		V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V		0.1	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V	I/O Data pins <sup>4</sup>	1.0	20	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>		0.1	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0		0.1	-5	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		1.0	±100	µA
I <sub>HOLD</sub>	Bus Hold current A or B outputs <sup>7</sup>	V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V	75	130		µA
		V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V	-75	-130		
		V <sub>CC</sub> = 0V to 3.6V; V <sub>CC</sub> = 3.6V	±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		50	125	µA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care		40	±100	µA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.07	0.12	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		4	5	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>6</sup>		0.07	0.12	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> -0.6V, Other inputs at V <sub>CC</sub> or GND		0.1	0.2	mA

**NOTES:**

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
3. This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
4. Unused pins at V<sub>CC</sub> or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I<sub>CCZ</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

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**AC CHARACTERISTICS**

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$f_{\text{MAX}}$	Maximum clock frequency	1	150				MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Bn or Bn to An	2	0.5 0.5	1.9 1.9	4.2 4.2	5.4 5.4	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	3.2 3.2	5.4 5.4	6.4 6.4	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay LEAB to Bn or LEBA to An	3	1.0 1.0	2.4 2.9	5.4 5.4	6.4 6.4	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to High and Low level	5 6	1.0 1.0	2.4 2.2	3.9 3.9	4.6 5.2	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from High and Low Level	5 6	1.0 1.0	2.8 3.2	5.2 5.2	5.6 5.6	ns

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

**AC SETUP REQUIREMENTS**

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	UNIT
			MIN	TYP	MIN	
			$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time, High or Low An to CPAB or Bn to CPBA	4	
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time, High or Low An to CPAB or Bn to CPBA	4	0 0	0 0	0 0	ns
$t_{\text{s(H)}}$ $t_{\text{s(L)}}$	Setup time, High or Low An to LEAB or Bn to CPBA	4	1.8 1.8	1.1 1.8	1.5 1.5	ns
$t_{\text{h(H)}}$ $t_{\text{h(L)}}$	Hold time, High or Low An to LEAB or Bn to LEBA	4	0 0	0 0	0 0	ns
$t_{\text{w(H)}}$ $t_{\text{w(L)}}$	Pulse width, High or Low CPAB or CPBA	1	1.2 1.2	0.8 0.8	1.5 1.5	ns
$t_{\text{w(H)}}$	LEAB or LEBA pulse width, High	3	1.2	0.8	1.5	ns

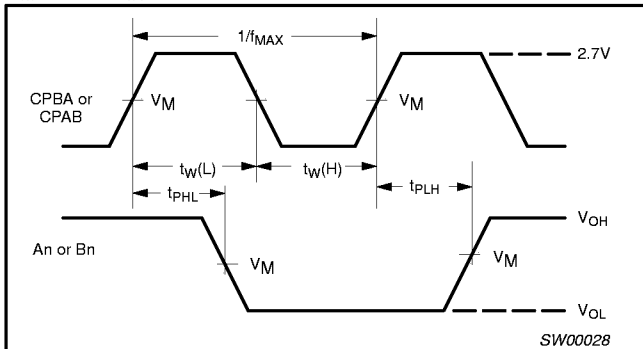
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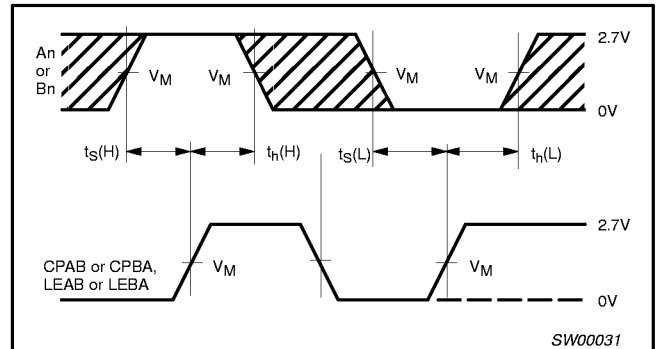
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AC WAVEFORMS

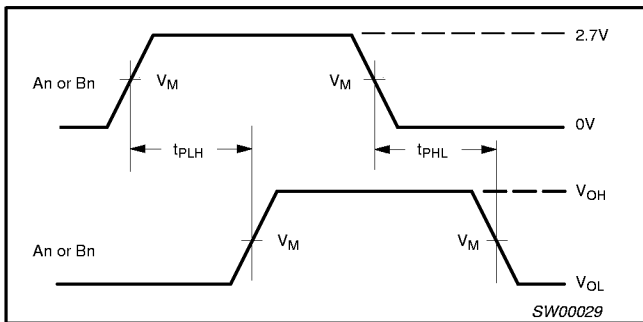
$V_M = 1.5V, V_{IN} = GND \text{ to } 2.7V$



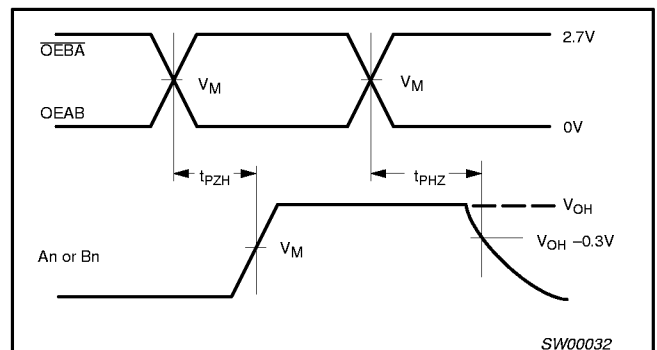
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



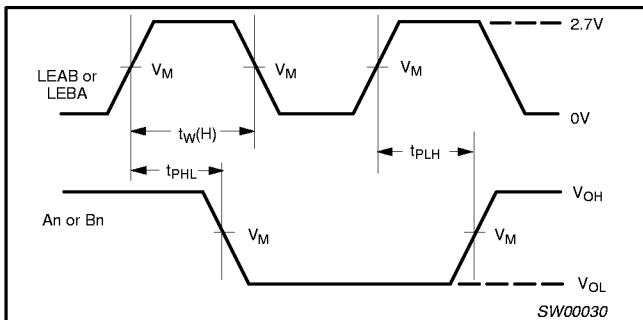
Waveform 4. Data Setup and Hold Times



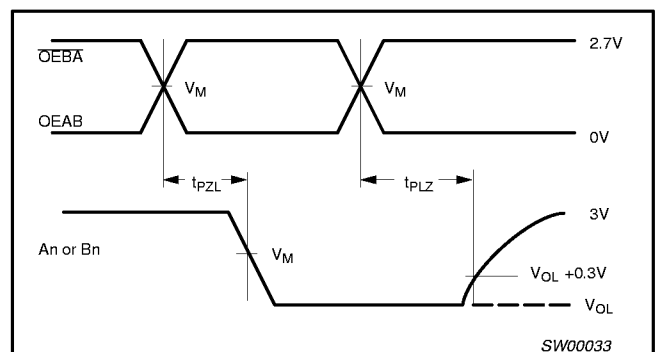
Waveform 2. Propagation Delay, Transparent Mode



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



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TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**Input Pulse Definition**  
 $V_M = 1.5V$

**SWITCH POSITION**

TEST	SWITCH
$t_{PHZ}/t_{PZH}$	GND
$t_{PLZ}/t_{PZL}$	6V
$t_{PLH}/t_{PHL}$	open

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74LVT16	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

SW00003

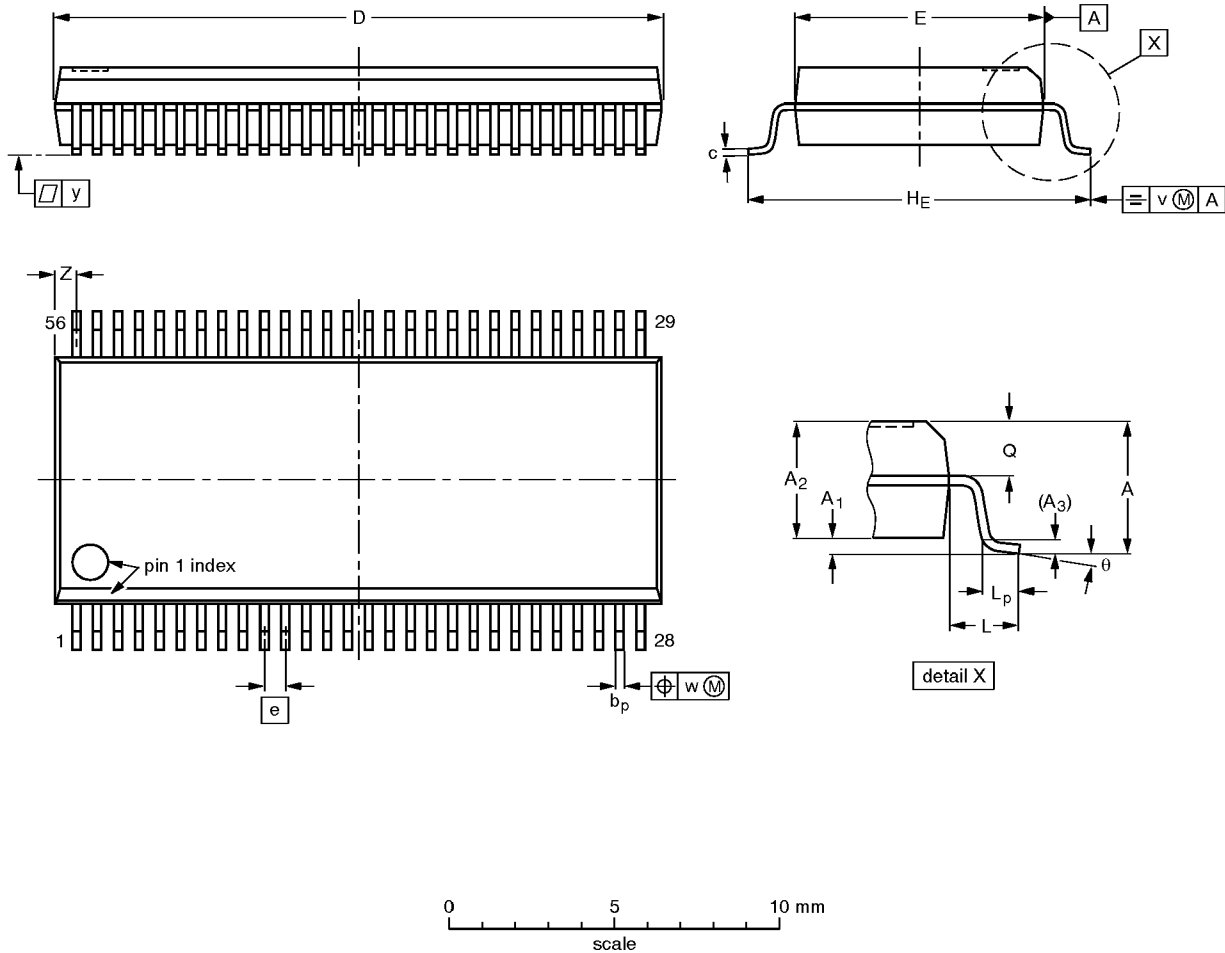
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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1

