National Semiconductor

## 54LS283／DM54LS283／DM74LS283 4－Bit Binary Adders with Fast Carry

## General Description

These full adders perform the addition of two 4－bit binary numbers．The sum（ $\Sigma$ ）outputs are provided for each bit and the resultant carry（C4）is obtained from the fourth bit． These adders feature full internal look ahead across all four bits．This provides the system designer with partial look－ ahead performance at the economy and reduced package count of a ripple－carry implementation．
The adder logic，including the carry，is implemented in its true form meaning that the end－around carry can be accom－ plished without the need for logic or level inversion．

## Features

－Full－carry look－ahead across the four bits
■ Systems achieve partial look－ahead performance with the economy of ripple carry
－Typical add times
Two 8－bit words 25 ns
Two 16－bit words 45 ns
－Typical power dissipation per 4－bit adder 95 mW
－Alternate Military／Aerospace device（54LS283）is avail－ able．Contact a National Semiconductor Sales Office／ Distributor for specifications．

Order Number 54LS283DMQB，54LS283FMQB，54LS283LMQB DM54LS283J，DM54LS283W，DM74LS283M or DM74LS283N See NS Package Number E20A，J16A，M16A，N16E or W16A

查询＂DM 74LS283M＂供应商


## Recommended Operating Conditions

| Symbol | Parameter | DM54LS283 |  |  | DM74LS283 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  | －0．4 |  |  | －0．4 | mA |
| lOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | －55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range（unless otherwise noted）

| Symbol | Parameter | Conditions |  | Min | Typ （Note 1） | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | －1．5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\text { Min } \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current＠Max Input Voltage | $\begin{aligned} & V_{C C}=M a x \\ & V_{I}=7 V \end{aligned}$ | A，B |  |  | 0.2 | mA |
|  |  |  | C0 |  |  | 0.1 |  |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\begin{aligned} & V_{C C}=M a x \\ & V_{I}=2.7 V \end{aligned}$ | A，B |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  | C0 |  |  | 20 |  |
| ILL | Low Level Input Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{I}}=0.4 \mathrm{~V} \end{aligned}$ | A，B |  |  | －0．8 | mA |
|  |  |  | C0 |  |  | －0．4 |  |
| los | Short Circuit Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & (\text { Note 2) } \end{aligned}$ | DM54 | －20 |  | －100 | mA |
|  |  |  | DM74 | －20 |  | －100 |  |
| $\mathrm{I}_{\mathrm{C} 1}$ | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$（Note 3） |  |  | 19 | 34 | mA |
| ICC2 | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$（Note 4） |  |  | 22 | 39 | mA |

Note 1：All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ．
Note 2：Not more than one output should be shorted at a time，and the duration should not exceed one second．
Note 3： $\mathrm{I}_{\mathrm{CC} 1}$ is measured with all outputs open，all B inputs low and all other inputs at 4.5 V ，or all inputs at 4.5 V ．
Note 4： $\mathrm{I}_{\mathrm{CC} 2}$ is measured with all outputs open and all inputs grounded．

查询＂DM 74LS283M＂供应商
Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$（See Section 1 for Test Waveforms and Output Load）

| Symbol | Parameter | From（Input） To（Output） |  |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $C_{L}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 1, \Sigma 2 \end{gathered}$ |  | 24 |  | 28 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 1, \Sigma 2 \\ \hline \end{gathered}$ |  | 24 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 3 \end{gathered}$ |  | 24 |  | 28 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 3 \end{gathered}$ |  | 24 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 4 \\ \hline \end{gathered}$ |  | 24 |  | 28 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \Sigma 4 \\ \hline \end{gathered}$ |  | 24 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{A}_{\mathrm{i}} \text { or } \mathrm{B}_{\mathrm{i}} \\ \text { to } \Sigma_{\mathrm{i}} \\ \hline \end{gathered}$ |  | 24 |  | 28 | ns |
| ${ }^{\text {P }}$ HL | Propagation Delay Time High to Low Level Output | $\begin{aligned} & \mathrm{A}_{\mathrm{i}} \text { or } \mathrm{B}_{\mathrm{i}} \\ & \text { to } \Sigma_{\mathrm{i}} \end{aligned}$ |  | 24 |  | 30 | ns |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \mathrm{C} 4 \\ \hline \end{gathered}$ |  | 17 |  | 24 | ns |
| ${ }_{\text {tPHL }}$ | Propagation Delay Time High to Low Level Output | $\begin{gathered} \mathrm{C} 0 \text { to } \\ \mathrm{C} 4 \\ \hline \end{gathered}$ |  | 17 |  | 25 | ns |
| ${ }_{\text {tpLH }}$ | Propagation Delay Time Low to High Level Output | $\mathrm{A}_{\mathrm{i}}$ or $\mathrm{B}_{\mathrm{i}}$ to C4 |  | 17 |  | 24 | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\mathrm{A}_{\mathrm{i}}$ or $\mathrm{B}_{\mathrm{i}}$ to C 4 |  | 17 |  | 26 | ns |

Function Table

|  |  |  |  |  |  | Out | puts |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Inp | put |  | When $\mathbf{C O}=$ |  | － | When Co＝ |  |  |
|  | $\mathrm{B3}_{\mathrm{B}}^{\mathrm{B1}}$ |  |  | $\begin{array}{\|lll} \hline & \Sigma 1 & \\ & & 53 \\ \hline \end{array}$ |  | C2 |  |  |  |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H＝High Level，L＝Low Level
Note：Input conditions at A1，B1，A2，B2，and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2．The values at $\mathrm{C} 2, \mathrm{~A} 3, \mathrm{~B} 3, \mathrm{~A} 4$ ，and B4 are then used to determine outputs $\Sigma 3, \Sigma 4$ ，and C 4

查询＂DM 74LS283M＂供应商

## Logic Diagram



TL／F／6421－2

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Physical Dimensions inches（millimeters）（Continued）


## Physical Dimensions inches（millimeters）（Continued）


detail A

16－Lead Ceramic Flat Package（W） Order Number 54LS283FMQB or DM54LS283W NS Package Number W16A

## LIFE SUPPORT POLICY

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2．A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system，or to affect its safety or effectiveness．

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