

## N-Channel 60 V (D-S) MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
60	0.021 at $V_{GS} = 10$ V	9.5
	0.031 at $V_{GS} = 4.5$ V	7.9

## FEATURES

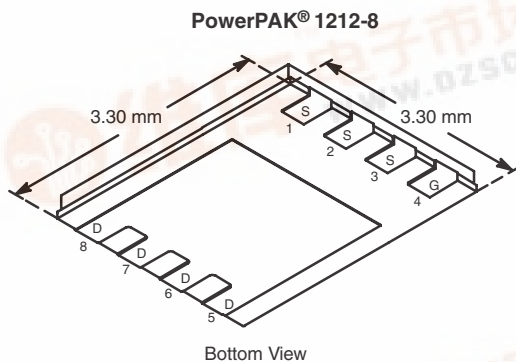
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 %  $R_G$  Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE

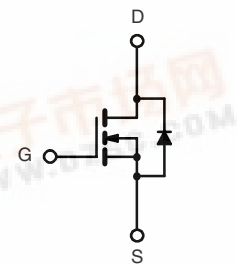
## APPLICATIONS

- Primary Side Switch
- Synchronous Rectification



Bottom View

Ordering Information: Si7120ADN-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS  $T_A = 25$  °C, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	60		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_A = 25$ °C	9.5	6.0	A
		$T_A = 70$ °C	7.6	4.8	
Pulsed Drain Current	$I_{DM}$	40		A	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	3.2	1.3		
Single Avalanche Current	$I_{AS}$	L = 0.1 mH	22		mJ
Single Avalanche Energy			$E_{AS}$	24	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25$ °C	3.8	1.5	W
		$T_A = 70$ °C	2.4	1.0	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>		260			

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ s	26	33	°C/W
		Steady State	65	81	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.9	2.4		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

## Si7120ADN


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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.5	2.5	3.0	V
Gate Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 9.5\text{ A}$		0.0175	0.021	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 7.9\text{ A}$		0.025	0.031	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 9.5\text{ A}$		35		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 3.2\text{ A}$ , $V_{GS} = 0\text{ V}$		0.78	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 9.5\text{ A}$		30	45	nC
Gate-Source Charge	$Q_{gs}$			6.9		
Gate-Drain Charge	$Q_{gd}$			5.8		
Gate Resistance	$R_g$		0.65	1.3	1.95	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$ , $R_L = 30\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 6\text{ }\Omega$		14	25	ns
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			50	80	
Fall Time	$t_f$			12	20	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 3.2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		60	100	

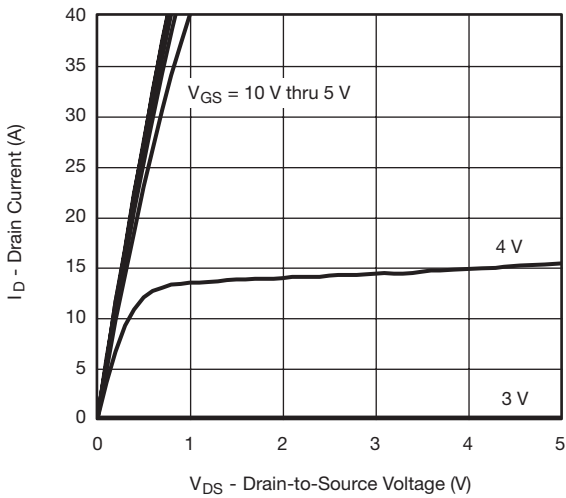
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

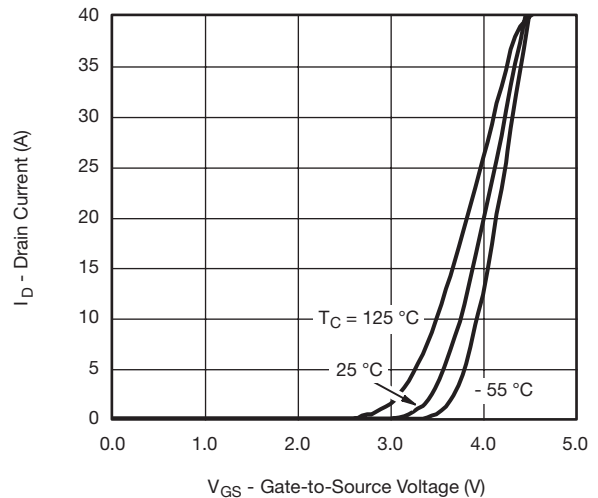
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

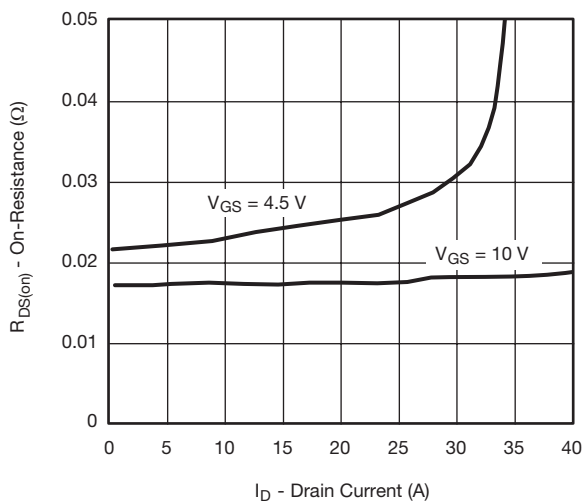
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



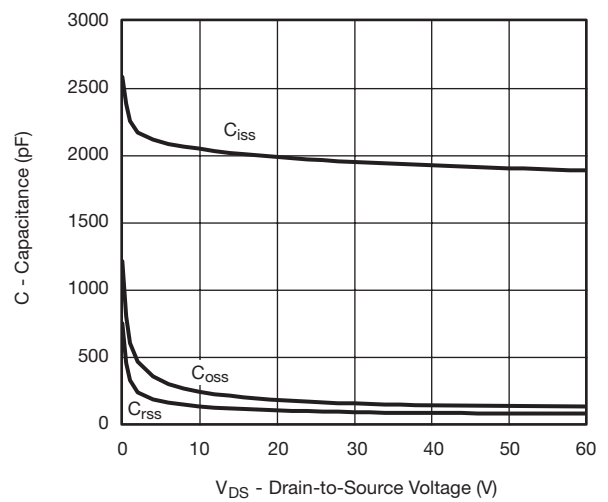
**Output Characteristics**



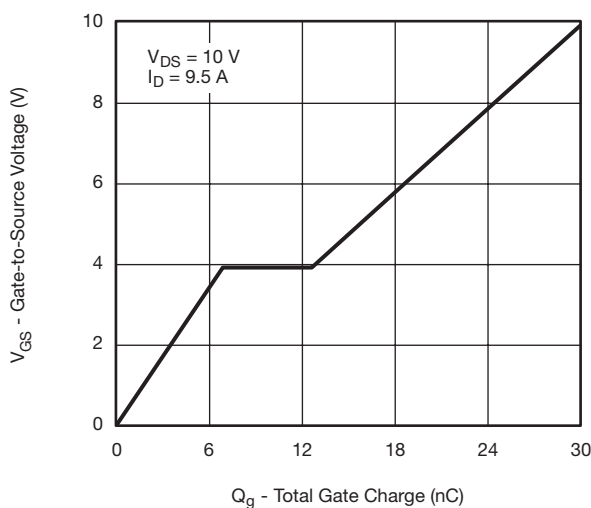
**Transfer Characteristics**



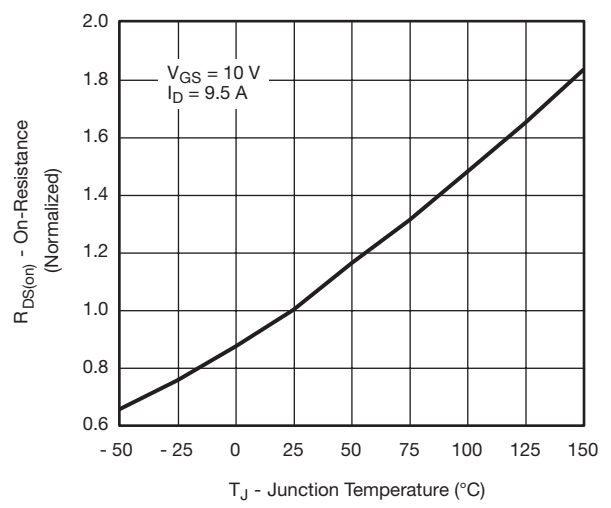
**On-Resistance vs. Drain Current**



**Capacitance**



**Gate Charge**



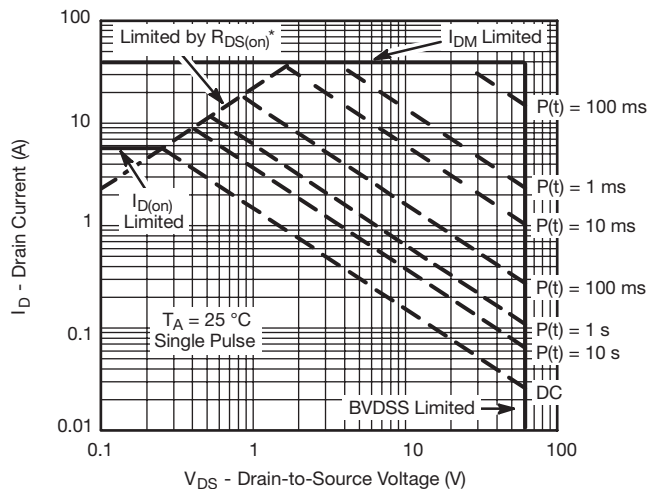
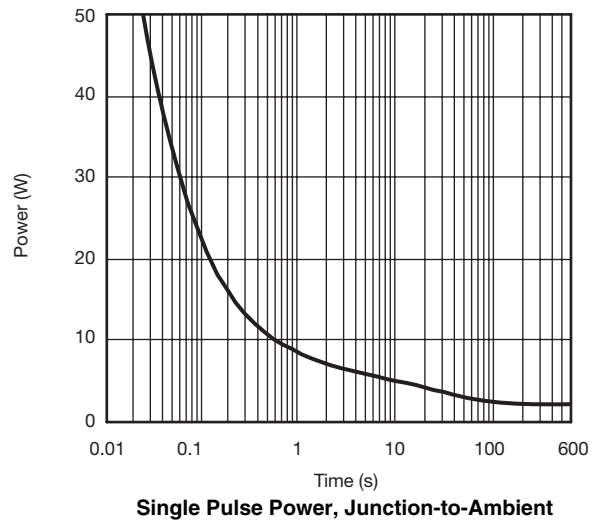
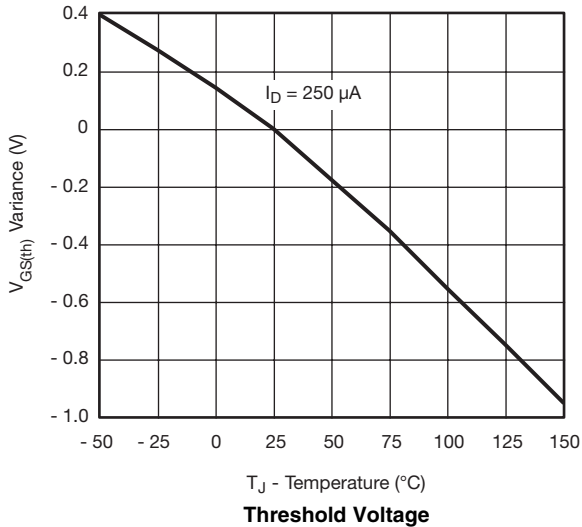
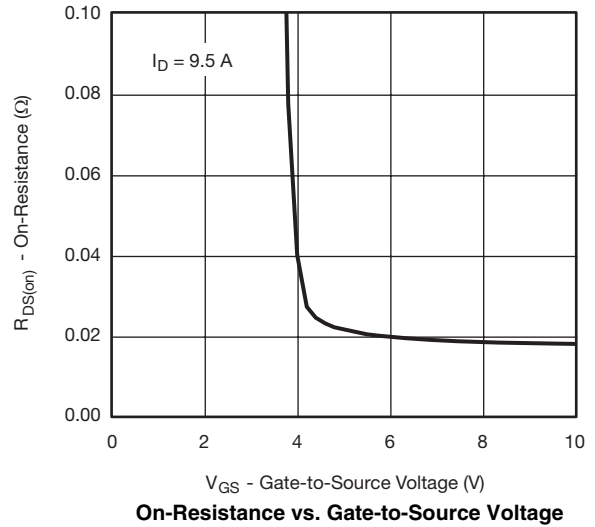
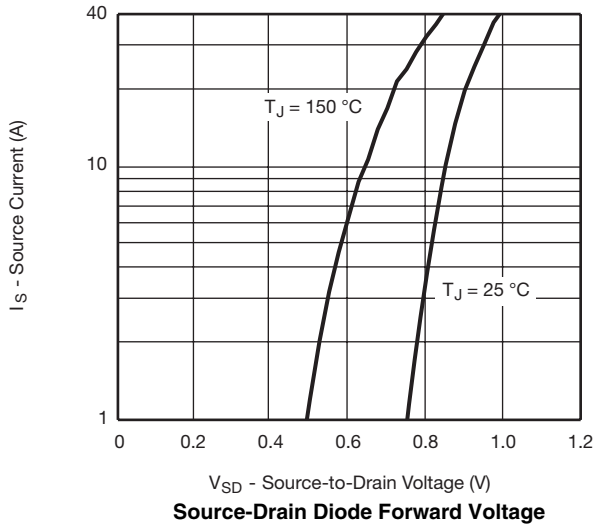
**On-Resistance vs. Junction Temperature**

# Si7120ADN



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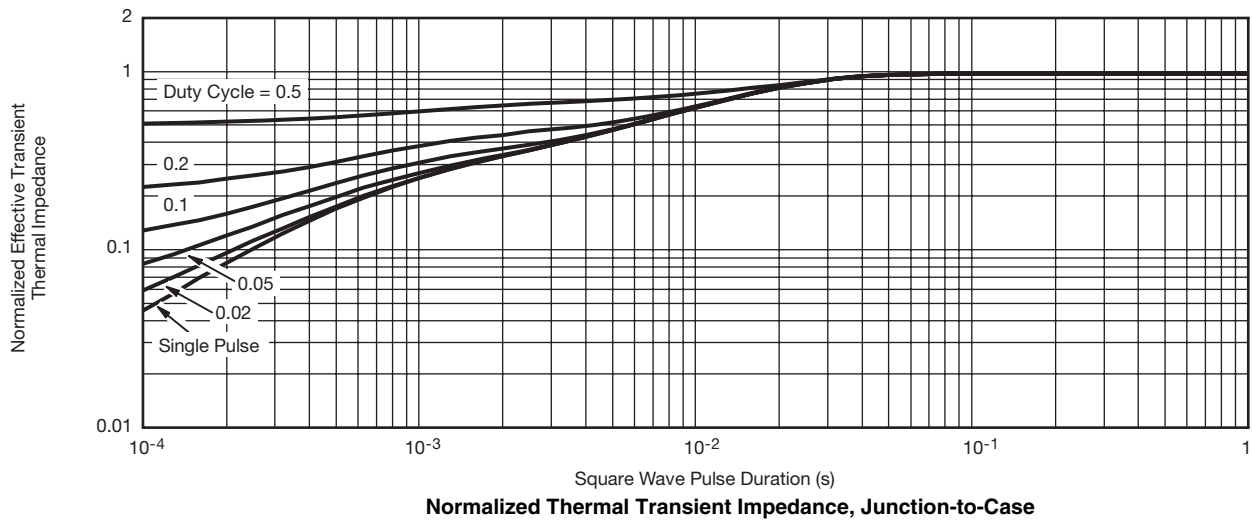
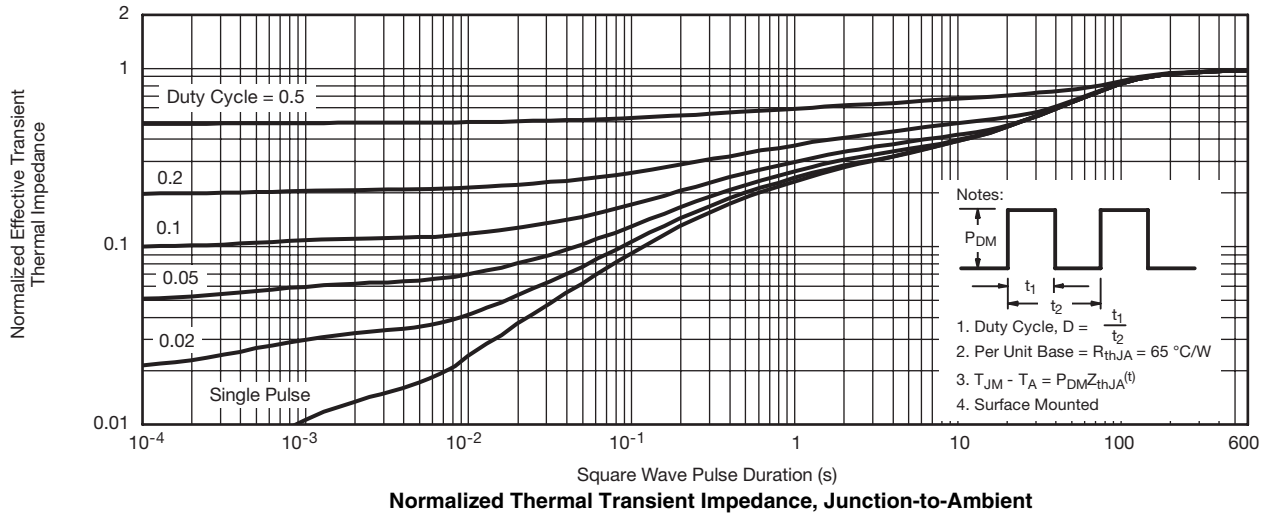
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

### Safe Operating Area

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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