

N-Channel 150-V (D-S) WFET

| PRODUCT SUMMARY | | | |
|---------------------|---------------------------------|---------------------------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) ^a | Q _g (Typ.) |
| 150 | 0.045 at V _{GS} = 10 V | 7.7 | 23 nC |
| | 0.047 at V _{GS} = 8 V | 7.5 | |

FEATURES

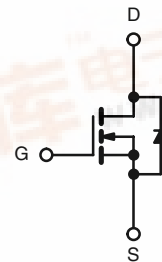
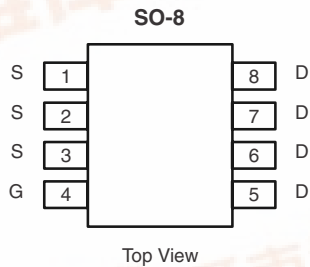
- Halogen-free According to IEC 61249-2-21 Available
- Extremely Low Qgd WFET[®] Technology for Switching Losses
- 100 % R_g Tested
- 100 % Avalanche Tested



RoHS
 COMPLIANT
 HALOGEN
FREE
 Available

APPLICATIONS

- Primary Side Switch



N-Channel MOSFET

Ordering Information: Si4472DY-T1-E3 (Lead (Pb)-free)
 Si4472DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | |
|---|-----------------------------------|------------------------|---------------------|---|
| Parameter | Symbol | Limit | Unit | |
| Drain-Source Voltage | V _{DS} | 150 | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | |
| Continuous Drain Current (T _J = 150 °C) | I _D | T _C = 25 °C | 7.7 | A |
| | | T _C = 70 °C | 6.1 | |
| | | T _A = 25 °C | 5.5 ^{b, c} | |
| | | T _A = 70 °C | 4.5 ^{b, c} | |
| Pulsed Drain Current | I _{DM} | 50 | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | 4.5 | |
| | | T _A = 25 °C | 2.6 ^{b, c} | |
| Single Pulse Avalanche Current | I _{AS} | 20 | | |
| Single Pulse Avalanche Energy | E _{AS} | 20 | mJ | |
| Maximum Power Dissipation | P _D | T _C = 25 °C | 5.9 | W |
| | | T _C = 70 °C | 3.8 | |
| | | T _A = 25 °C | 3.1 ^{b, c} | |
| | | T _A = 70 °C | 2 ^{b, c} | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | °C | |

| THERMAL RESISTANCE RATINGS | | | | |
|---|-------------------|---------|---------|------|
| Parameter | Symbol | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient ^{b, f} | R _{thJA} | 33 | 40 | °C/W |
| Maximum Junction-to-Foot (Drain) | R _{thJF} | 17 | 21 | |

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 80 °C/W.



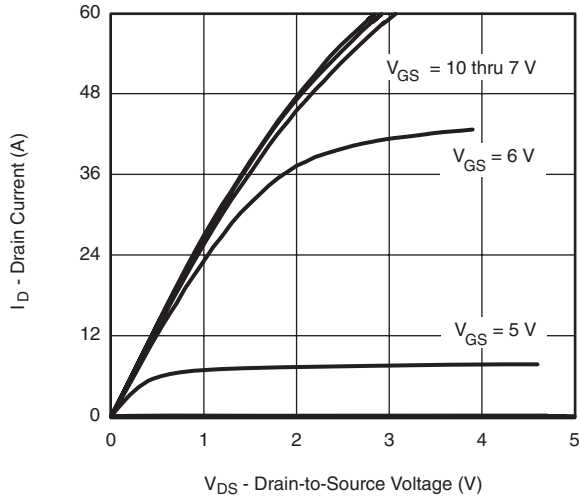
| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|--|-------------------------|--|------|--------|-----------|---------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 150 | | | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D = 250\text{ }\mu\text{A}$ | | 172 | | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | - 10 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2.5 | | 4.5 | V |
| Gate-Source Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$ | | | 10 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$ | 30 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 5\text{ A}$ | | 0.036 | 0.045 | Ω |
| | | $V_{GS} = 8\text{ V}, I_D = 5\text{ A}$ | | 0.0375 | 0.047 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 5\text{ A}$ | | 23 | | S |
| Dynamic^b | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 1735 | | μF |
| Output Capacitance | C_{oss} | | | 160 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 37 | | |
| Total Gate Charge | Q_g | $V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$ | | 28.5 | 43 | nC |
| | | $V_{DS} = 75\text{ V}, V_{GS} = 8\text{ V}, I_D = 5\text{ A}$ | | 23 | 35 | |
| Gate-Source Charge | Q_{gs} | | | 8 | | |
| Gate-Drain Charge | Q_{gd} | | 6.5 | | | |
| Gate Resistance | R_g | $f = 1\text{ MHz}$ | | 0.85 | 1.3 | Ω |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD} = 50\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ | | 14 | 21 | ns |
| Rise Time | t_r | | | 12 | 18 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 22 | 33 | |
| Fall Time | t_f | | | 6 | 10 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 50\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 8\text{ V}, R_g = 1\text{ }\Omega$ | | 16 | 24 | |
| Rise Time | t_r | | | 12 | 18 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 20 | 30 | |
| Fall Time | t_f | | | 7 | 12 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25\text{ }^\circ\text{C}$ | | | 7.7 | A |
| Pulse Diode Forward Current ^a | I_{SM} | | | | 50 | |
| Body Diode Voltage | V_{SD} | $I_S = 2.6\text{ A}$ | | 0.77 | 1.2 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ | | 63 | 95 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 110 | 165 | nC |
| Reverse Recovery Fall Time | t_a | | | 49 | | ns |
| Reverse Recovery Rise Time | t_b | | | 14 | | |

Notes:

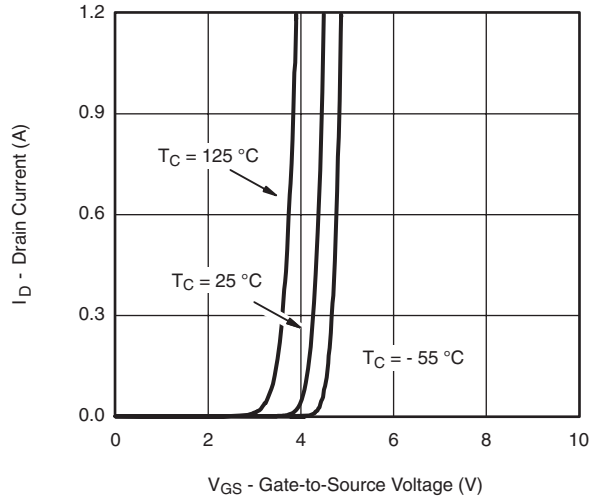
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
a. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

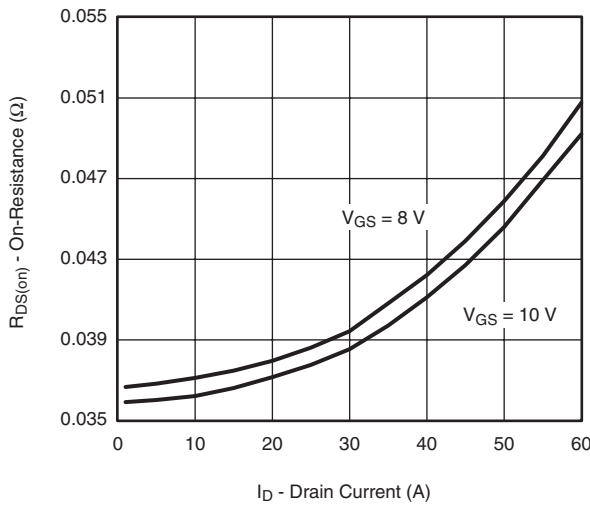
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



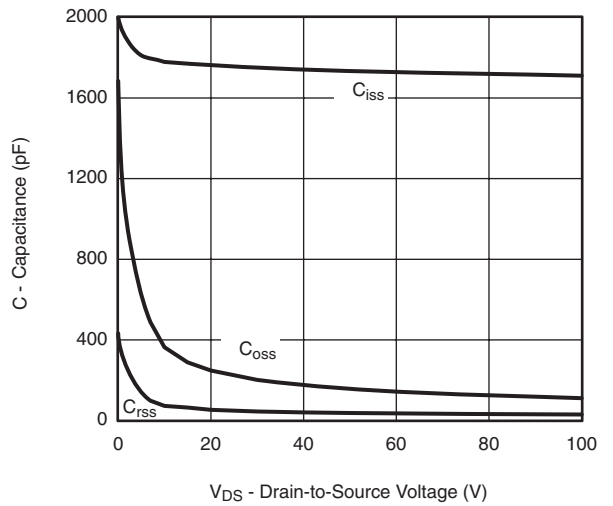
Output Characteristics



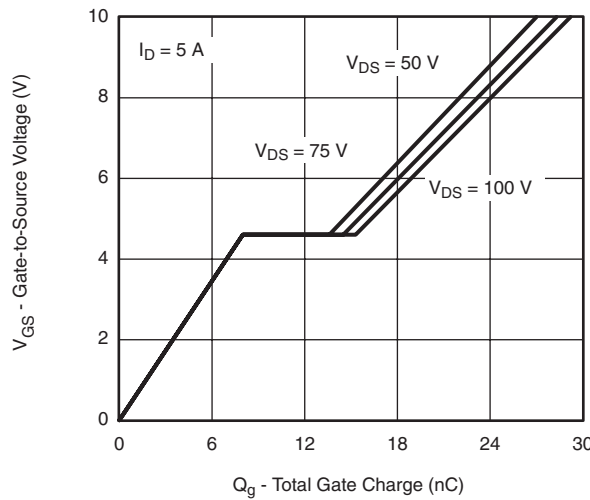
Transfer Characteristics



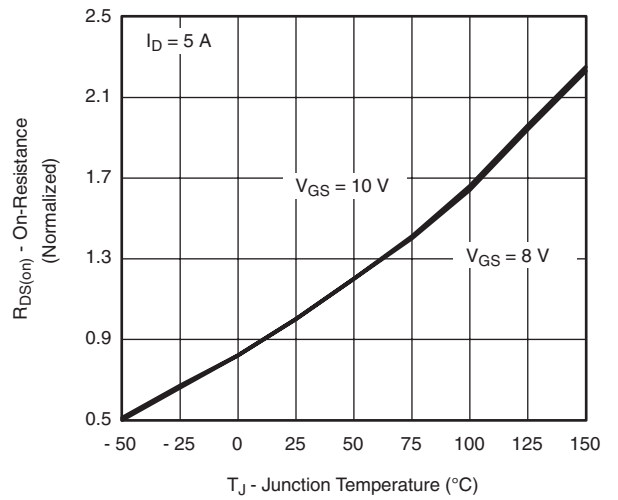
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

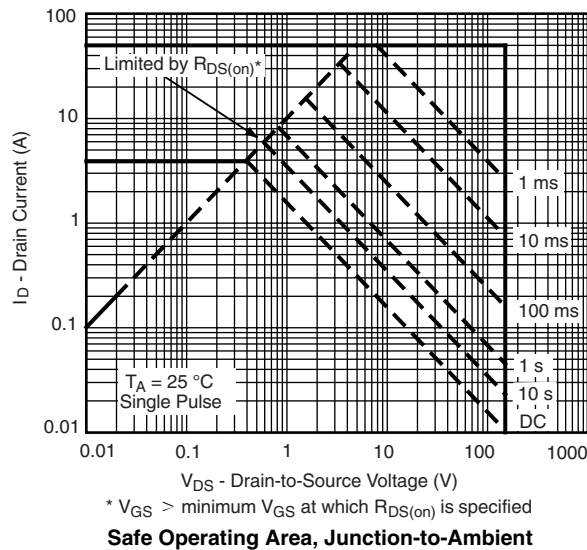
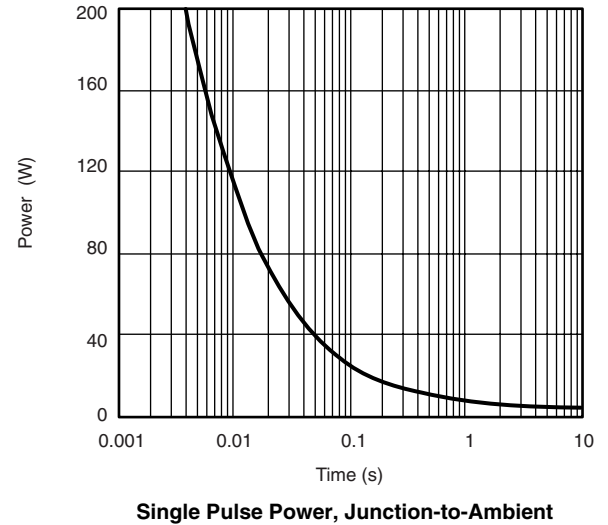
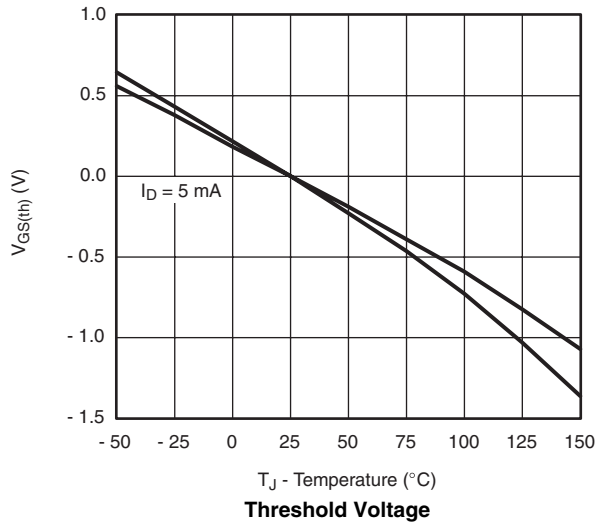
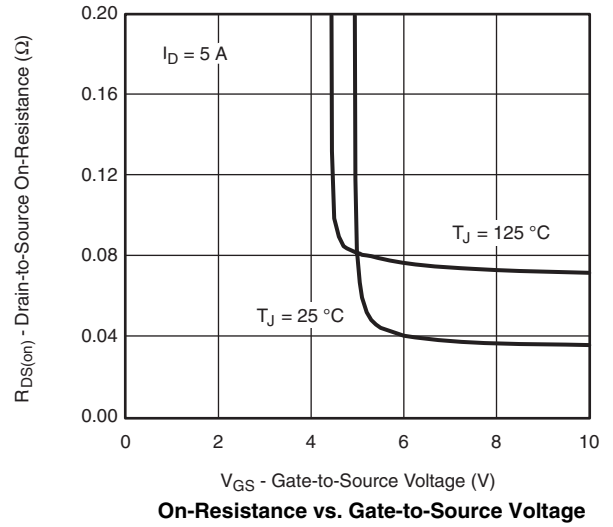
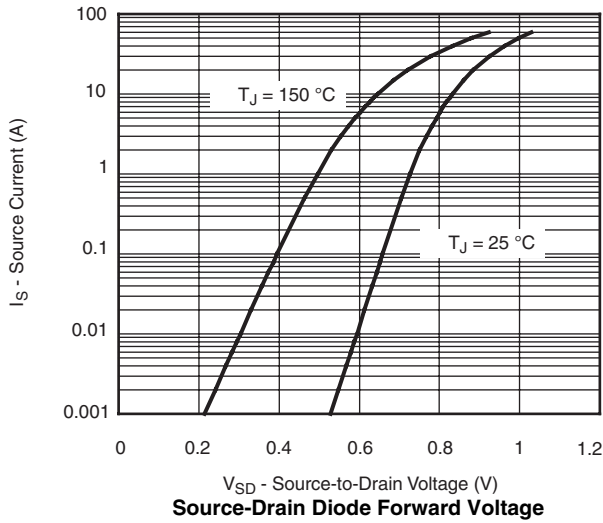


Gate Charge

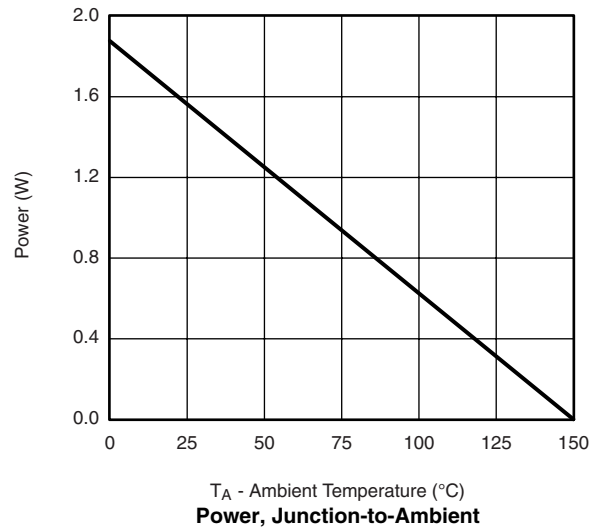
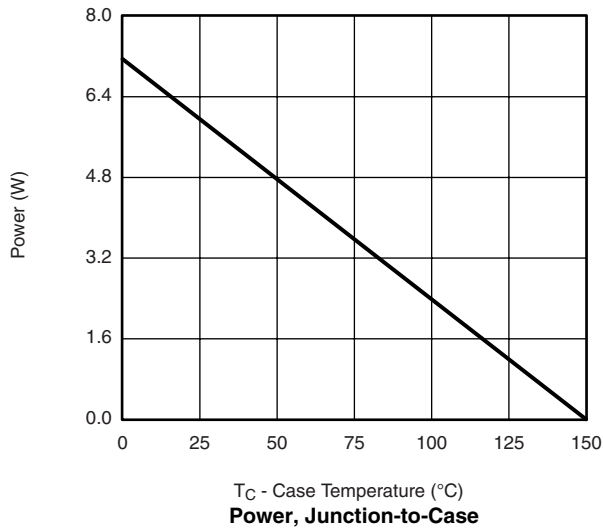
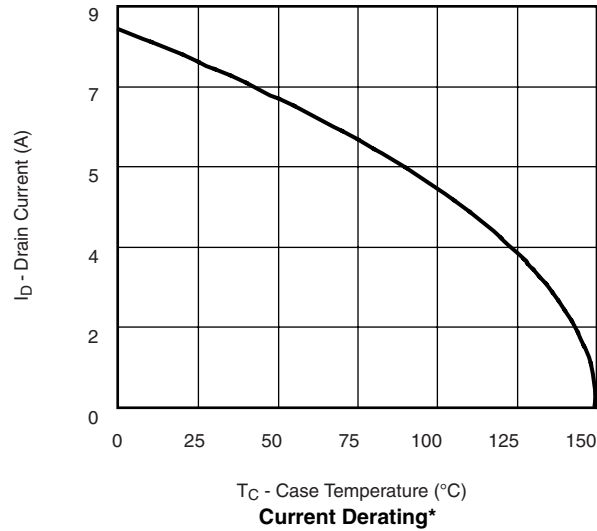


On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

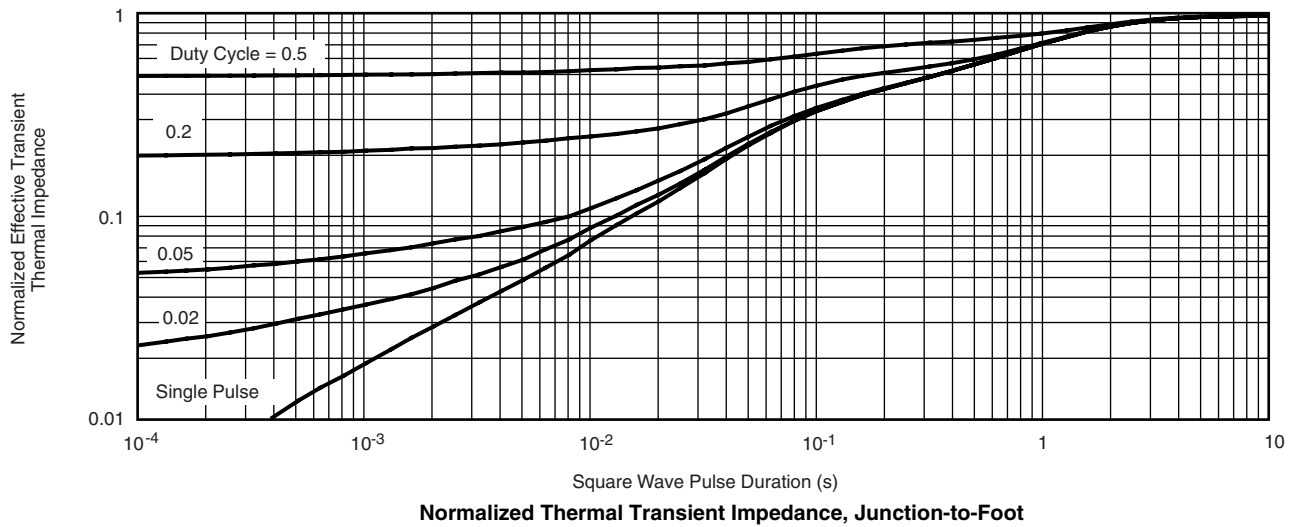
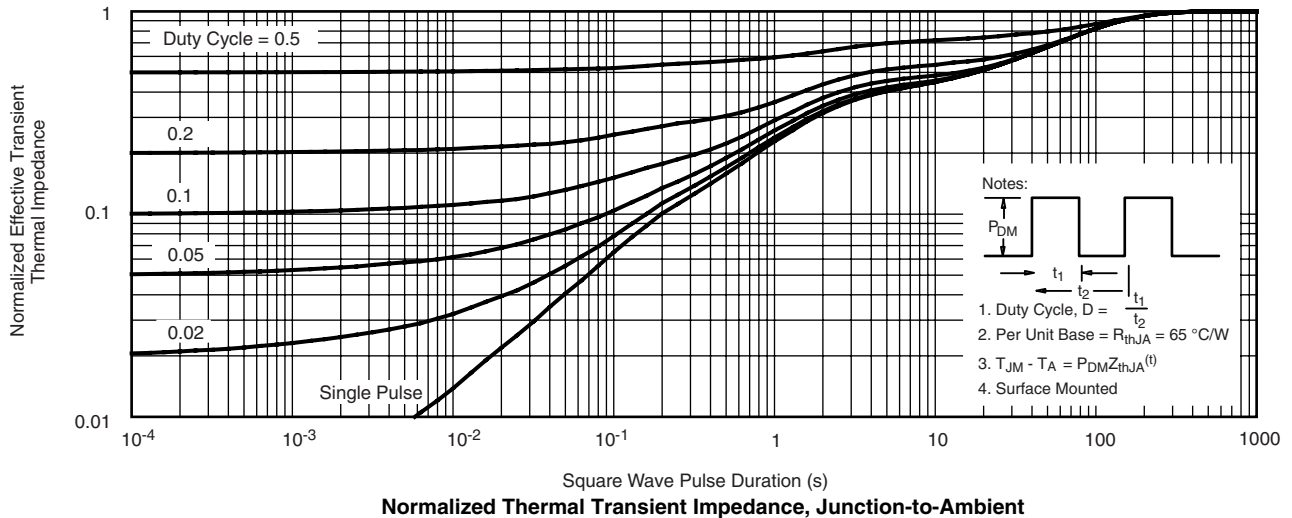


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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