National Semiconductor

DM74S289
64-Bit (16 x 4) Open-Collector RAM TRI-STATE® RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S289 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

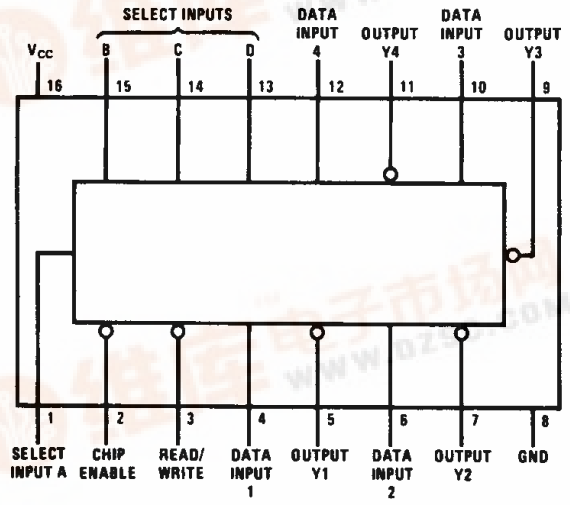
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

Features

- Commercial address access time 25 ns
- Features open-collector output
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74S289J or DM74S289N
See NS Package Number J16A or N16E

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 Sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM74S289	4.75	5.25	V
Temperature (T_A)			
DM74S289	0	+70	°C

DM74S289 Electrical Characteristics

Over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −6.5 mA	2.4	3.2		V
I_{CEX}	High Level Output Current	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA				0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{CC}	Supply Current (Note 4)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM74S289 Switching Characteristics

Over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM74S289 Min	DM74S289 Typ (Note 2)	DM74S289 Max	Units
t_{AA}	Access Time from Address		C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω *(Figure 4)*		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			12	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	20	ns
t_{WLH}	Disable Time from Read/Write				13	25	ns
t_{WP}	Width of Enable Pulse (Read/Write Low)			25			ns
t_{ASW}	Setup Time *(Figure 2)*	Address to Read/Write		0			ns
t_{DSW}		Data to Read/Write		25			ns
t_{CSW}		Chip-Enable to Read/Write		0			ns
t_{AHW}	Hold Time *(Figure 2)*	Address from Read/Write		0			ns
t_{DHW}		Data from Read/Write		0			ns
t_{CHW}		Chip-Enable from Read/Write		0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

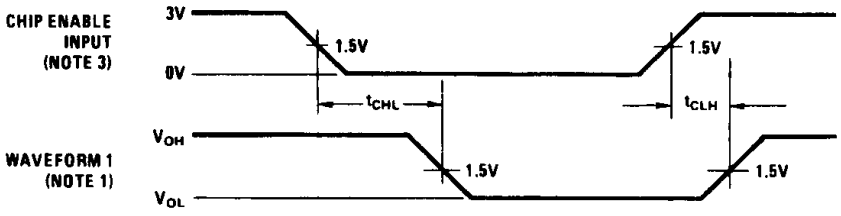
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to −70°C range for the DM74S189/289. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: I_{CC} is measured with all inputs grounded, and the outputs open.

DM74S289 Switching Time Waveforms

Enable and Disable Time from Chip-Enable



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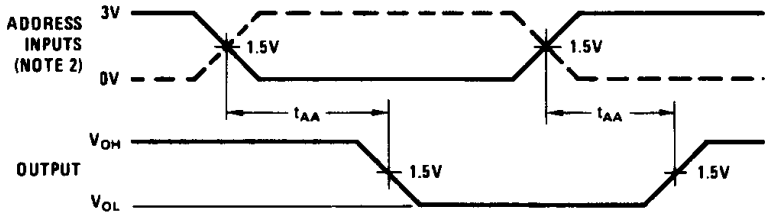
Access Time from Address Inputs



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Write Cycle

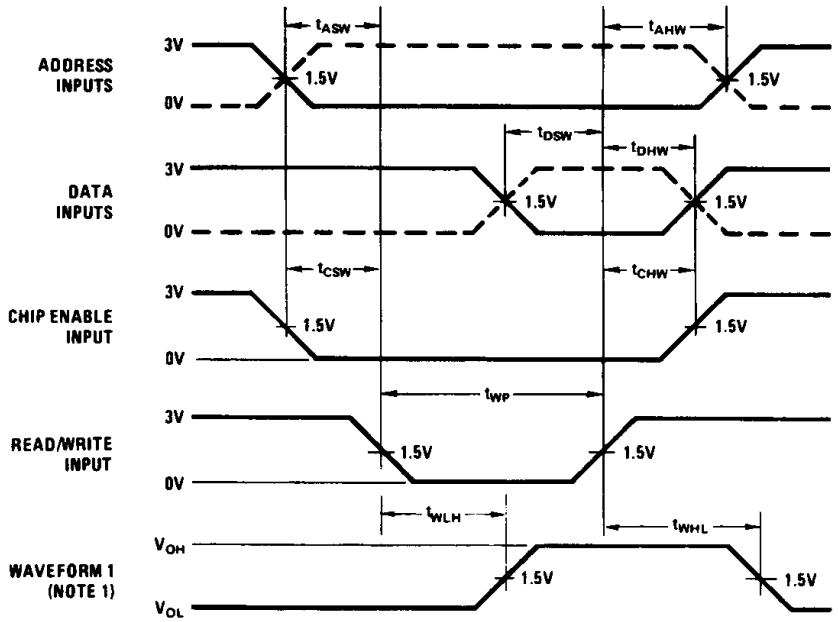

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FIGURE 2

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. PRR ≤ 1 MHz and $Z_{OUT} = 50\Omega$.

Block Diagram

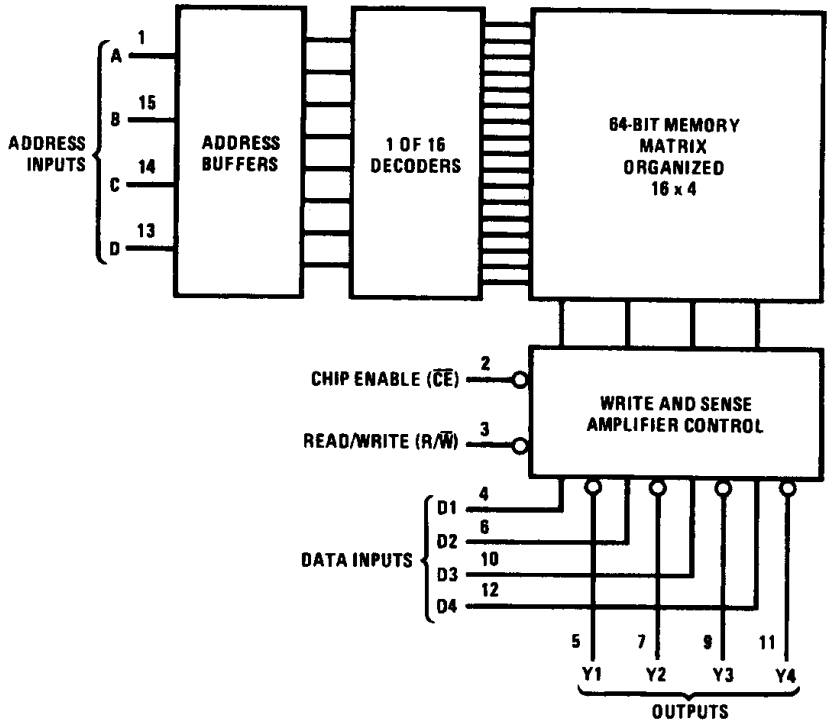

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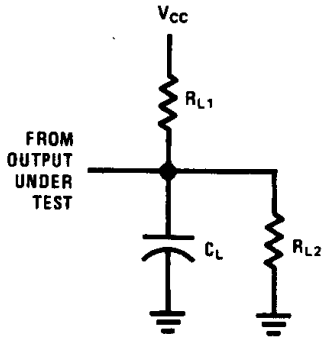
FIGURE 3

AC Test Circuit



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