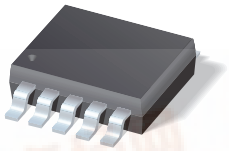
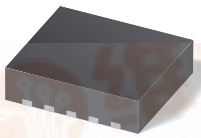




16-/14-/12-Bit, Dual-Channel, Ultralow-Glitch, Voltage-Output DIGITAL-TO-ANALOG CONVERTER With 2.5-V, 2-ppm/°C INTERNAL REFERENCE

Check for Samples: DAC8562, DAC8162, DAC7562

FEATURES

- **Relative Accuracy:**
  - **DAC8562 (16-Bit): 4 LSB INL**
  - **DAC8162 (14-Bit): 1 LSB INL**
  - **DAC7562 (12-Bit): 0.3 LSB INL**
- **Glitch Energy: 0.1 nV-s**
- **Internal Reference:**
  - **2.5-V Reference Voltage (Disabled by Default)**
  - **±5-mV Initial Accuracy (Max)**
  - **2-ppm/°C Temperature Drift (Typ)**
  - **5-ppm/°C Temperature Drift (Max)**
  - **20-mA Sink/Source Capability**
- **Power-On Reset to Zero Scale**
- **Ultralow Power Operation: 0.8 mA at 5 V Including Internal Reference Current**
- **Wide Power-Supply Range: 2.7 V to 5.5 V**
- **Monotonic Over Entire Temperature Range**
- **Low-Power Serial Interface With Schmitt-Triggered Inputs: Up to 50 MHz**
- **On-Chip Output Buffer Amplifier With Rail-to-Rail Operation**
- **Temperature Range: –40°C to 125°C**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control/Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation, Digital Gain, and Offset Adjustment**
- **Programmable Voltage and Current Sources**

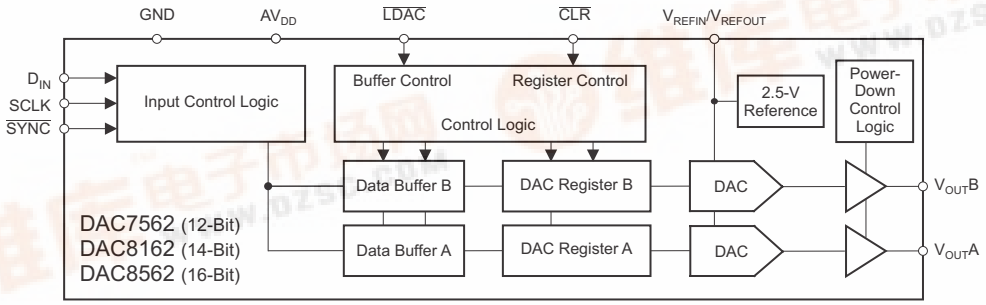
DESCRIPTION

The DAC8562, DAC8162, and DAC7562 are low-power, voltage-output, dual-channel, 16-, 14-, and 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 2-ppm/°C internal reference (disabled by default), giving a full-scale output voltage range of 2.5 V or 5 V. The internal reference has an initial accuracy of ±5 mV and can source up to 20 mA at the V_{REFIN}/V_{REFOUT} pin. These devices are monotonic, providing excellent linearity and minimizing undesired code-to-code transient voltages (glitch). They use a versatile three-wire serial interface that operates at clock rates up to 50 MHz. The interface is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces. The DAC8562, DAC8162, and DAC7562 incorporate a power-on-reset circuit that ensures the DAC output powers up at zero scale until a valid code is written to the device. These devices contain a power-down feature, accessed over the serial interface that reduces current consumption to typically 0.18 µA at 5 V. Power consumption (including internal reference) is typically 1.6 mW at 3 V, reducing to less than 9 µW in power-down mode. The low power consumption, internal reference, and small footprint make these devices ideal for portable, battery-operated equipment.

The DAC8562, DAC8162, and DAC7562 are drop-in and function-compatible with each other, and are available in MSOP-10 and QFN-10 packages.

Table 1. RELATED DEVICES

	16-BIT	14-BIT	12-BIT
Pin-and Functional-Compatible	DAC8562	DAC8162	DAC7562



PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 2. PACKAGING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	OUTPUT VOLTAGE FULL-SCALE RANGE	RESET TO	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8562	±12	±1	5	5 V	Zero	QFN-10	DSC	–40°C to 125°C	8562
						MSOP-10	DGS		
DAC8162	±3	±0.5	5	5 V	Zero	QFN-10	DSC	–40°C to 125°C	8162
						MSOP-10	DGS		
DAC7562	±0.75	±0.25	5	5 V	Zero	QFN-10	DSC	–40°C to 125°C	7562
						MSOP-10	DGS		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI Web site at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
AV_{DD} to GND	–0.3 to 6	V
Digital input voltage to GND	–0.3 to AV_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to AV_{DD} + 0.3	V
V_{REFIN}/V_{REFOUT} to GND	–0.3 to AV_{DD} + 0.3	V
Operating temperature range	–40 to 125	°C
Junction temperature, maximum ($T_{J\ max}$)	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC		(1)PINS	PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)			°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)			
θ_{JB}	Junction-to-board thermal resistance(4)			
ψ_{JT}	Junction-to-top characterization parameter(5)			
ψ_{JB}	Junction-to-board characterization parameter(6)			
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)			

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC8562	Resolution		16			Bits
	Relative accuracy	Measured by the line passing through codes 485 and 64,714		±4	±12	LSB
	Differential nonlinearity	16-bit monotonic		±0.2	±1	LSB
DAC8162	Resolution		14			Bits
	Relative accuracy	Measured by the line passing through codes 120 and 16,200		±1	±3	LSB
	Differential nonlinearity	14-bit monotonic		±0.1	±0.5	LSB
DAC7562	Resolution		12			Bits
	Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±0.75	LSB
	Differential nonlinearity	12-bit monotonic		±0.05	±0.25	LSB
Offset error		Extrapolated from two-point line(1), unloaded		±1	±4	mV
Offset error drift				±0.5		µV/°C
Full-scale error		DAC register loaded with all 1s		±0.03	±0.2	% of FSR
Zero-code error		DAC register loaded with all 0s		1	4	mV
Zero-code error drift				±2		µV/°C
Gain error		Extrapolated from two-point line(1), unloaded		±0.01	±0.15	% of FSR
Gain temperature coefficient				±1		ppm of FSR/°C
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		AV_{DD}	V
Output voltage settling time		DACs unloaded; 1/4 scale to 3/4 scale to ±0.024%		7		µs
		R_L = 1 MΩ		10		
Slew rate				0.75		V/µs
Capacitive load stability		R_L = ∞		1		nF
		R_L = 2 kΩ		3		
Code-change glitch impulse		1-LSB change around major carry		0.1		nV-s
Digital feedthrough		SCLK toggling, SYNC high		0.1		nV-s
Power-on glitch impulse		R_L = 2 kΩ, C_L = 470 pF, AV_{DD} = 5.5 V		10		mV
Channel-to-channel dc crosstalk		Full-scale swing on adjacent channel		0.1		LSB
Channel-to-channel ac crosstalk		R_L = 2 kΩ, C_L = 420 pF, 1-kHz full-scale sine wave, outputs unloaded		–109		dB
DC output impedance		At mid-code input		4		Ω
Short-circuit current		DAC outputs at full-scale, DAC outputs shorted to GND		11		mA
Power-up time, including settling time		Coming out of power-down mode		50		µs

(1) 16-bit: codes 485 and 64,714; 14-bit: codes 120 and 16,200; 12-bit: codes 30 and 4050
(2) Specified by design or characterization; not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE(3)					
Signal-to-noise ratio, SNR	T_A = 25°C, BW = 20 kHz, AV_{DD} = 5 V, f_{OUT} = 1 kHz, first 19 harmonics removed for SNR calculation, at 16-bit level		83		dB
Total harmonic distortion, THD			–63		dB
Spurious-free dynamic range, SFDR			63		dB
Signal-to-noise and distortion, SINAD			62		dB
DAC output noise density	T_A = 25°C, at zero-code input, f_{OUT} = 1 kHz		90		nV/√Hz
DAC output noise	T_A = 25°C, at mid-code input, 0.1 Hz to 10 Hz		2.6		μV_{PP}
REFERENCE					
Internal reference current consumption	AV_{DD} = 5.5 V		360		µA
	AV_{DD} = 3.6 V		348		
External reference current	External V_{REF} = 2.5 V (when internal reference is disabled), all channels active		15		µA
V_{REFIN} reference input range		0		AV_{DD}	V
Reference input impedance	Internal reference disabled		170		kΩ
REFERENCE OUTPUT					
Output voltage	T_A = 25°C	2.495	2.5	2.505	V
Initial accuracy	T_A = 25°C	–5	±0.1	5	mV
Output voltage temperature drift			2	5	ppm/°C
Output voltage noise	f = 0.1 Hz to 10 Hz		12		μV_{PP}
Output voltage noise density (high-frequency noise)	T_A = 25°C, f = 1 kHz, C_L = 0 µF		250		nV√Hz
	T_A = 25°C, f = 1 MHz, C_L = 0 µF		50		
	T_A = 25°C, f = 1 MHz, C_L = 4 µF		16		
Load regulation, sourcing(4)	T_A = 25°C		30		µV/mA
Load regulation, sinking(4)	T_A = 25°C		15		µV/mA
Output current load capability(3)			±20		mA
Line regulation	T_A = 25°C		10		µV/V
Long-term stability/drift (aging)(4)	T_A = 25°C, time = 0 to 1900 hours		100		ppm
Thermal hysteresis(4)	First cycle		200		ppm
	Additional cycles		50		
LOGIC INPUTS(3)					
Input current			±1		µA
Logic input LOW voltage $V_{IN}L$	2.7 V ≤ AV_{DD} ≤ 5.5 V			0.8	V
Logic input HIGH voltage $V_{IN}H$	2.7 V ≤ AV_{DD} ≤ 5.5 V	1.8			V
Pin capacitance				3	pF

(3) Specified by design or characterization; not production tested.
(4) Explained in more detail in the *Application Information* section of this data sheet

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

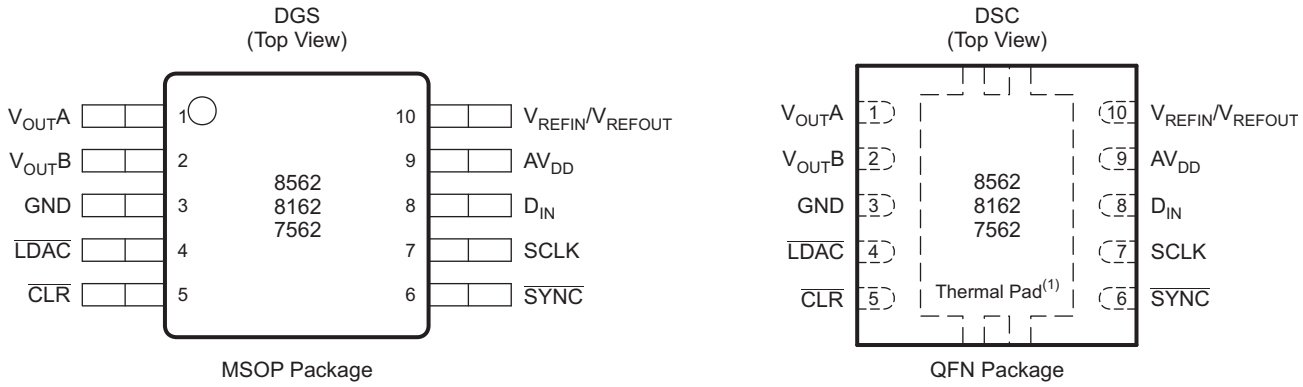
At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS					
Power supply voltage AV_{DD}		2.7		5.5	V
Current consumption(5)	Normal mode, internal reference switched off, AV_{DD} = 3.6 V to 5.5 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.25	0.45	mA
	Normal mode, internal reference switched off, AV_{DD} = 2.7 V to 3.6 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.2	0.4	
	Normal mode, internal reference switched on, AV_{DD} = 3.6 V to 5.5 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.8	1	
	Normal mode, internal reference switched on, AV_{DD} = 2.7 V to 3.6 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.6	0.9	
	All power-down modes(6), AV_{DD} = 3.6 V to 5.5 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.18	3	
	All power-down modes(6), AV_{DD} = 2.7 V to 3.6 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.15	2.5	
Power dissipation(5)	Normal mode, internal reference switched off, AV_{DD} = 3.6 V to 5.5 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.9	2.5	mW
	Normal mode, internal reference switched off, AV_{DD} = 2.7 V to 3.6 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.54	1.44	
	Normal mode, internal reference switched on, AV_{DD} = 3.6 V to 5.5 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		2.9	5.5	
	Normal mode, internal reference switched on, AV_{DD} = 2.7 V to 3.6 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		1.62	3.24	
	All power-down modes(6), AV_{DD} = 3.6 V to 5.5 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.65	16.5	µW
	All power-down modes(6), AV_{DD} = 2.7 V to 3.6 V, $V_{IN}H = AV_{DD}$, and $V_{IN}L$ = GND		0.41	9	
TEMPERATURE RANGE					
Specified performance		–40		125	°C

(5) Input code = midscale, no load
(6) Temperature range -40°C to 105°C

PRODUCT PREVIEW

PIN CONFIGURATION



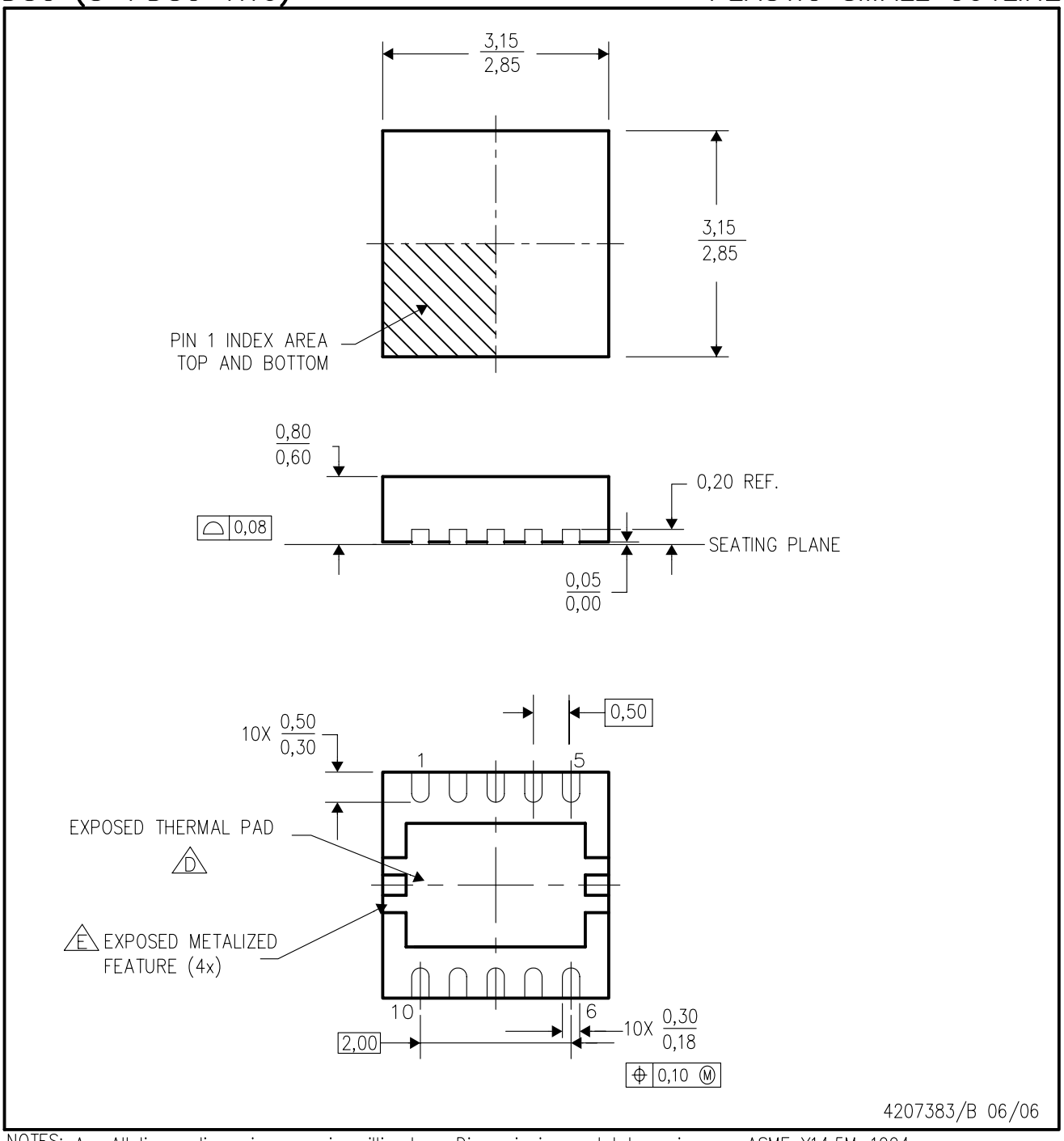
(1) It is recommended to connect the thermal pad to the ground plane for better thermal dissipation.

Table 3. PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
AV_{DD}	9	Power-supply input, 2.7 V to 5.5 V
$\overline{CLR}$	5	Asynchronous clear input
D_{IN}	8	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-trigger logic input
GND	3	Ground reference point for all circuitry on the device
$\overline{LDAC}$	4	Load DACs
SCLK	7	Serial clock input. Data can be transferred at rates up to 50 MHz. Schmitt-trigger logic input
$\overline{SYNC}$	6	Level-triggered control input (active-low). This input is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24th clock falling edge. If SYNC is taken high before the 23rd clock edge, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC7562/DAC8162/DAC8562. Schmitt-trigger logic input
$V_{OUT}A$	1	Analog output voltage from DAC A
$V_{OUT}B$	2	Analog output voltage from DAC B
V_{REFIN}/ V_{REFOUT}	10	Positive reference input / reference output 2.5V if internal reference used.

PRODUCT PREVIEW

DSC (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

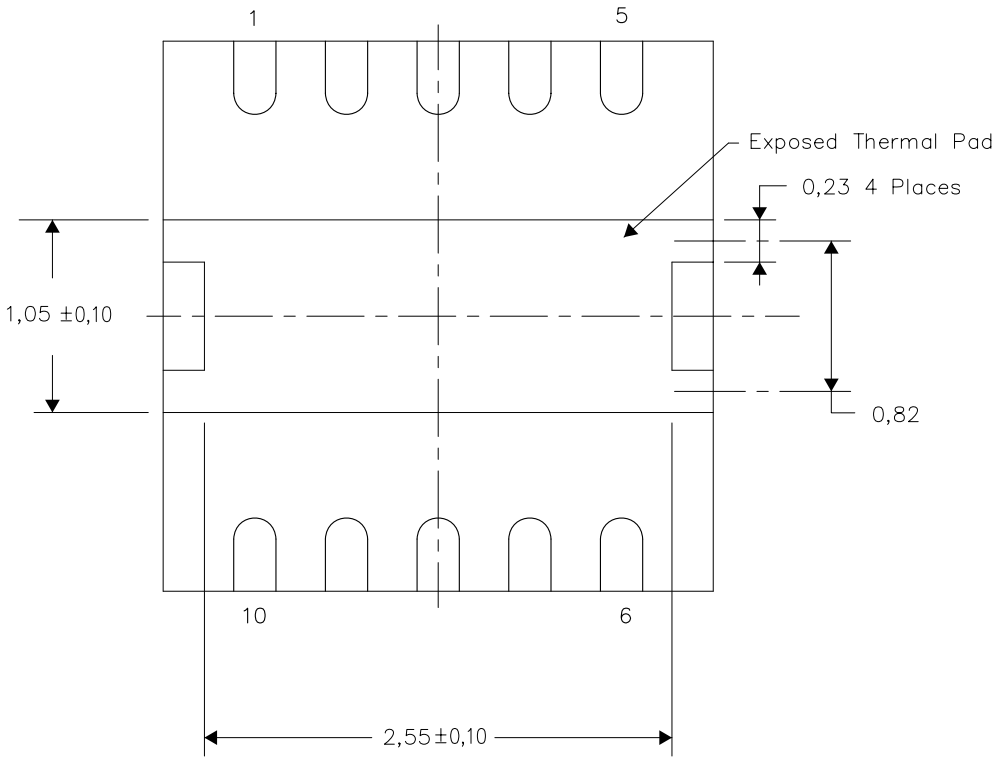
DSC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

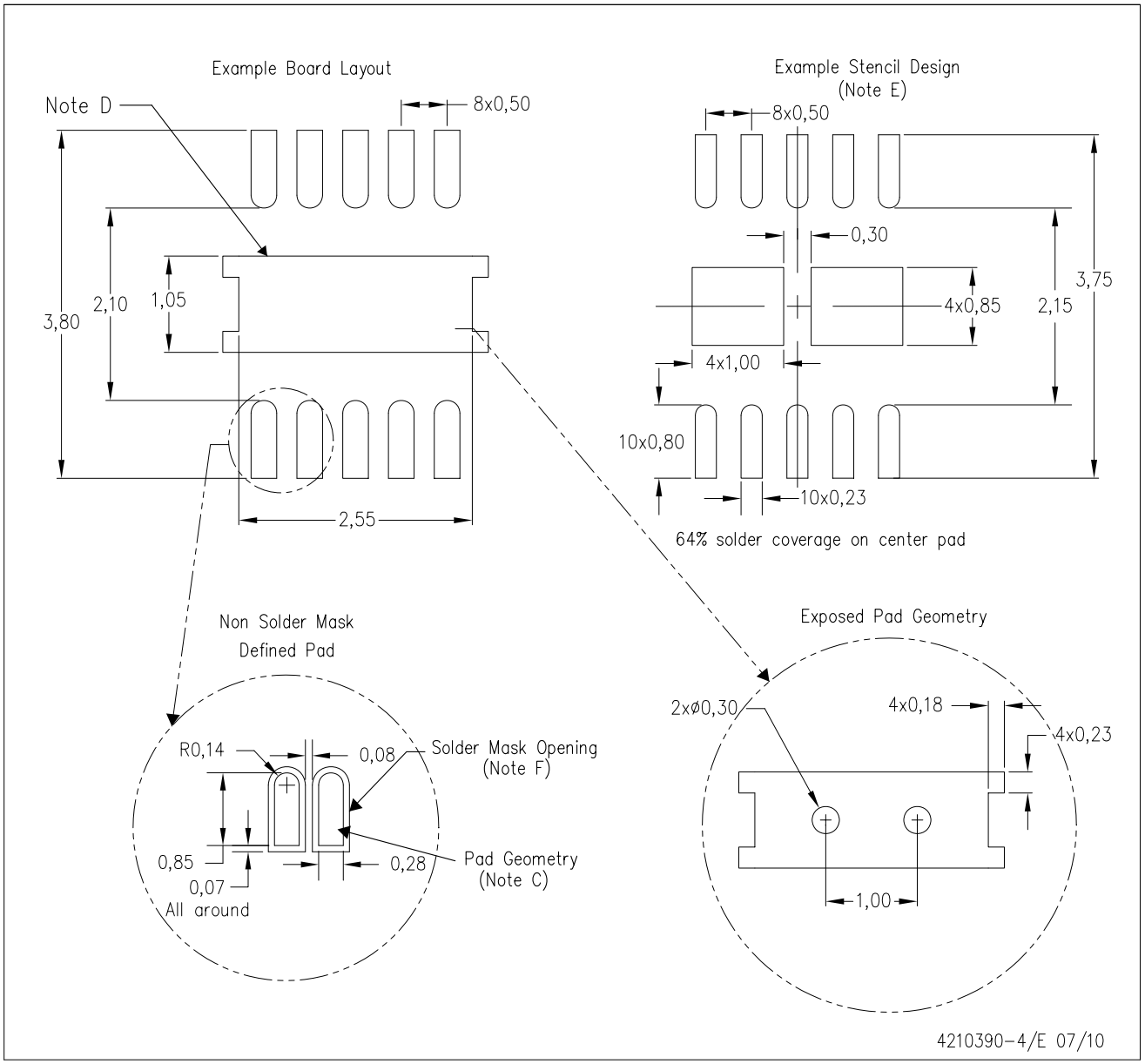


Bottom View

NOTE: All linear dimensions are in millimeters

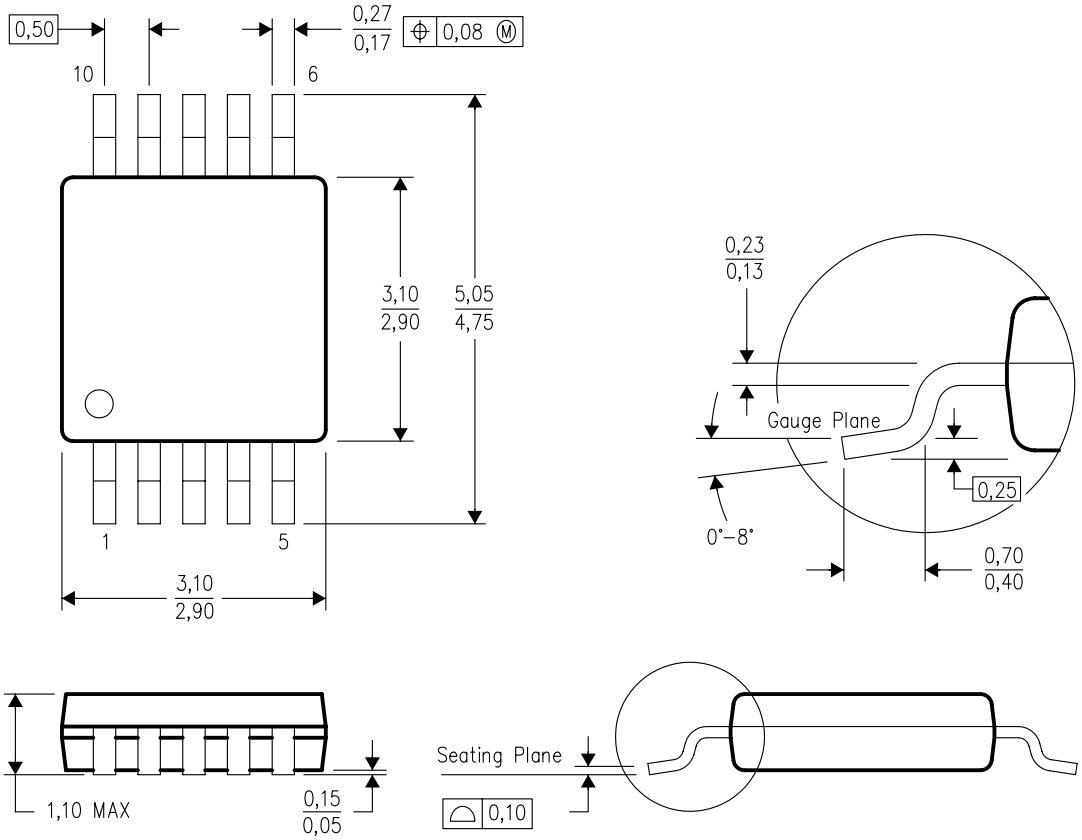
Exposed Thermal Pad Dimensions

DSC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
DAC7562SDGS	PREVIEW	MSOP	DGS	10		TBD	Call TI	Call TI
DAC7562SDSC	PREVIEW	SON	DSC	10		TBD	Call TI	Call TI
DAC8162SDGS	PREVIEW	MSOP	DGS	10		TBD	Call TI	Call TI
DAC8162SDSC	PREVIEW	SON	DSC	10		TBD	Call TI	Call TI
DAC8562SDGS	PREVIEW	MSOP	DGS	10		TBD	Call TI	Call TI
DAC8562SDSC	PREVIEW	SON	DSC	10		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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