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3SK233

**Silicon N Channel Dual Gate MOS FET
UHF TV Tuner RF Amplifier**

Feature

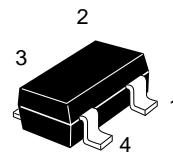
- Low voltage operation.
- Superior cross modulation characteristics.

Table 1 Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V _{DS}	12	V
Gate 1 to source voltage	V _{G1S}	±10	V
Gate 2 to source voltage	V _{G2S}	±10	V
Drain current	I _D	35	mA
Channel power dissipation	P _{ch}	150	mW
Channel temperature	T _{ch}	125	°C
Storage temperature	T _{stg}	-55 to +125	°C

MPAK-4



1. Source
2. Gate 1
3. Gate 2
4. Drain

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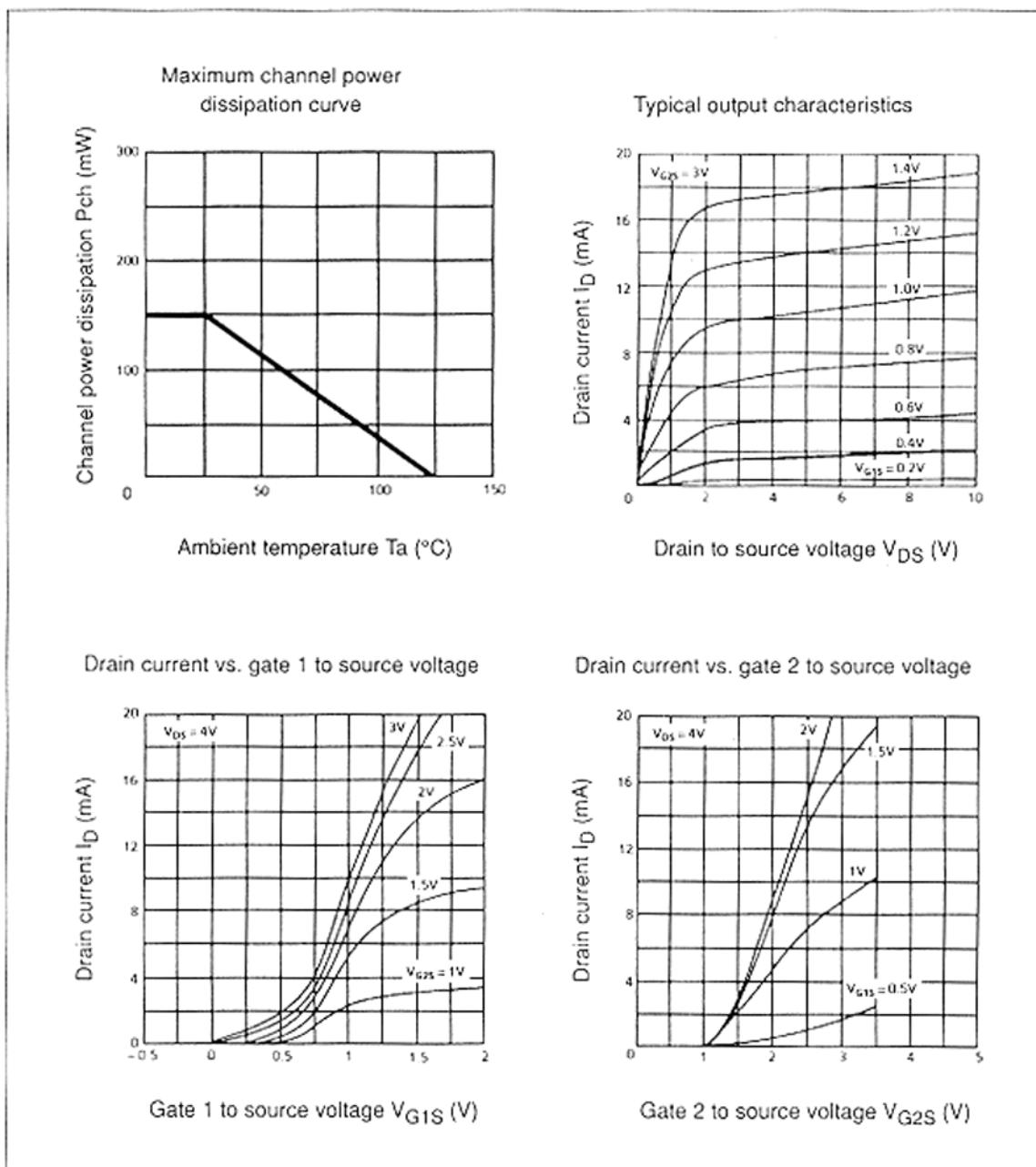
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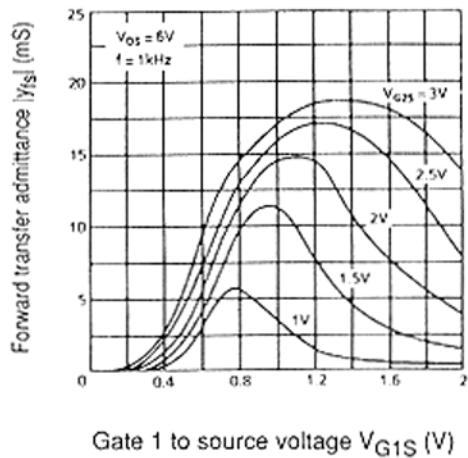
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test condition
Drain to source breakdown voltage	V _{(BR)DSX}	12	—	—	V	I _D = 200 μA, V _{G1S} = -5 V, V _{G2S} = -5 V
Gate 1 to source breakdown voltage	V _{(BR)G1SS}	±10	—	—	V	I _{G1} = ±10 μA, V _{G2S} = V _{DS} = 0
Gate 2 to source breakdown voltage	V _{(BR)G2SS}	±10	—	—	V	I _{G2} = ±10 μA, V _{G1S} = V _{DS} = 0
Gate 1 cutoff current	I _{G1SS}	—	—	±100	nA	V _{G1S} = ±8 V, V _{G2S} = V _{DS} = 0
Gate 2 cutoff current	I _{G2SS}	—	—	±100	nA	V _{G2S} = ±8 V, V _{G1S} = V _{DS} = 0
Drain current	I _{DSS}	0	—	2	mA	V _{DS} = 6 V, V _{G1S} = 0, V _{G2S} = 3 V
Gate 1 to source cutoff voltage	V _{G1S(off)}	-0.7	—	+0.7	V	V _{DS} = 10 V, V _{G2S} = 3 V, I _D = 100 μA
Gate 2 to source cutoff voltage	V _{G2S(off)}	-0.1	—	+0.8	V	V _{DS} = 10 V, V _{G1S} = 3 V, I _D = 100 μA
Forward transfer admittance	y _{fs}	14	—	—	mS	V _{DS} = 6 V, V _{G2S} = 3 V, I _D = 10 mA, f = 1 kHz
Input capacitance	C _{iss}	0.9	1.25	1.8	pF	V _{DS} = 6 V, V _{G2S} = 3 V, I _D = 10 mA, f = 1 MHz
Output capacitance	C _{oss}	0.4	0.7	1.2	pF	
Reverse transfer capacitance	C _{rss}	—	0.015	0.03	pF	
Power gain	PG	16	19.4	—	dB	V _{DS} = 4 V, V _{G2S} = 3 V, I _D = 10 mA, f = 900 MHz
Noise figure	NF	—	2.8	4	dB	

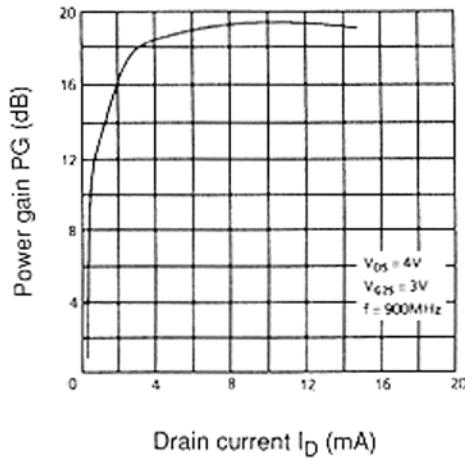
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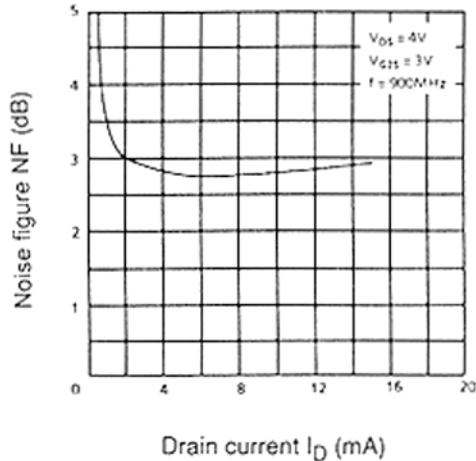


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vs. gate 1 to source voltage

Power gain vs. drain current

Gate 1 to source voltage V_{G1S} (V)Drain current I_D (mA)

Noise figure vs. drain current

Drain current I_D (mA)

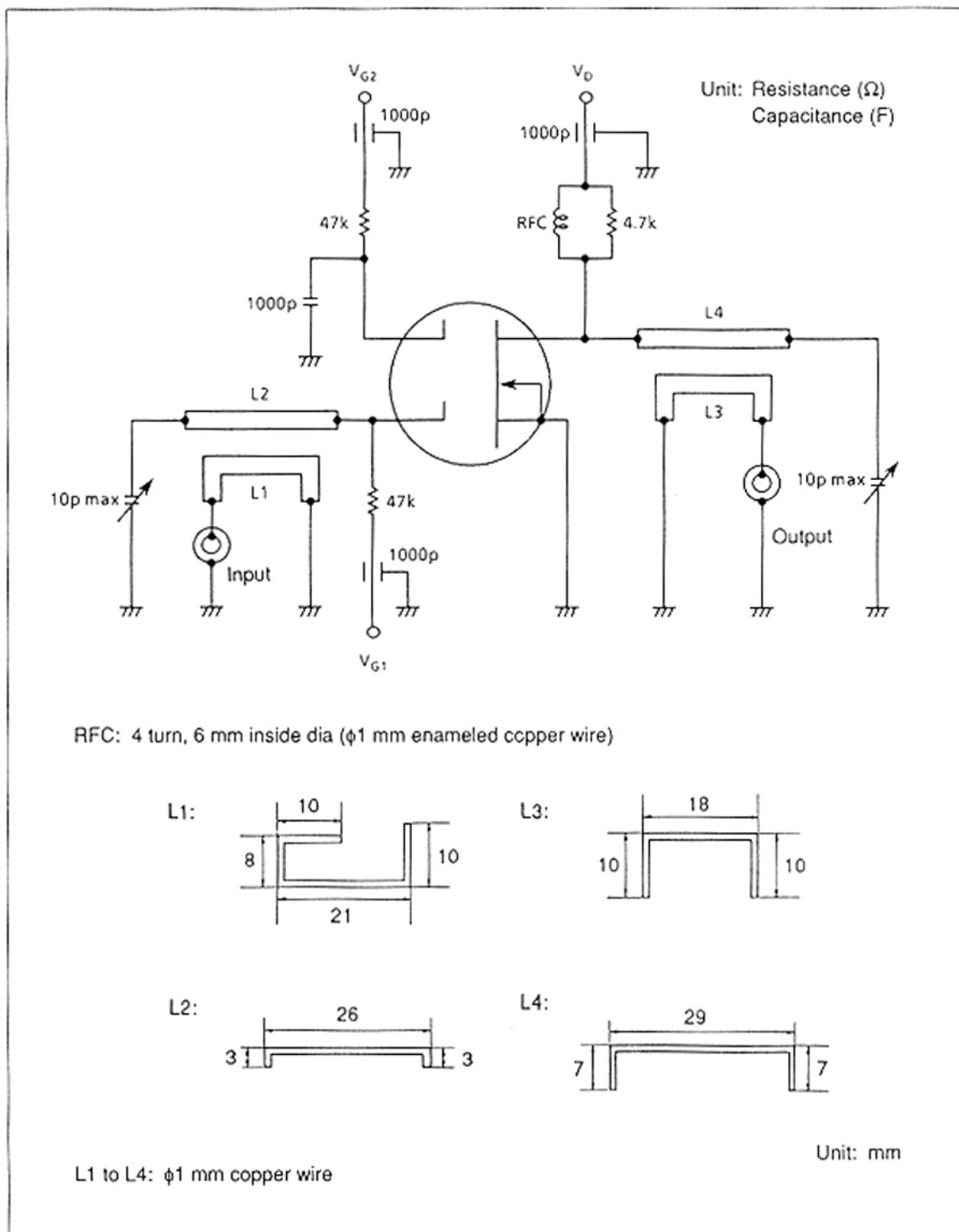
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Figure 1 900 MHz Power Gain, Noise Figure Test Circuit