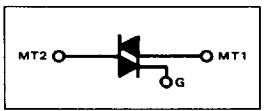
Triacs
Silicon Bidirectional Triode Thyristors

2N5444 thru 2N5446

TRIACs 40 AMPERES RMS 200 thru 600 VOLTS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants



CASE 263-04
STYLE 2
2N5444 thru 2N5446

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MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +110°C) (Note 1) 1/2 Sine Wave 50 to 60 Hz, Gate Open *Peak Principal Voltage 2N5444 2N5445 2N5446	V_{DRM}	200 400 600	Volts
*RMS On-State Current (T_C per Figure 2) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	40 20	Amps
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceded and followed by a 40 A RMS current, T_C = 100°C)	I_{TSM}	300	Amps
*Peak Gate Power (Pulse Width = 10 μs Max)	P_{GM}	40	Watts
*Average Gate Power	$P_{G(AV)}$	0.75	Watt
*Peak Gate Current (10 μs Max)	I_{GM}	4	Amps
*Peak Gate Voltage	V_{GM}	30	Volts
*Operating Junction Temperature Range	T_J	−65 to +110	°C
*Storage Temperature Range	T_{stg}	−65 to +150	°C
*Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case 2N5444, 2N5445, 2N5446	$R_{\theta JC}$	0.9	°C/W

*Indicates JEDEC Registered Data.

Note 1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

2N5444 thru 2N5446

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Gate Open, V_D = Rated V_{DRM}) T_C = 25°C	I_{DRM}	—	—	10	μA
T_C = 100°C		—	0.5	4	mA
*Peak On-State Voltage (I_{TM} = 56 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_{TM}	—	1.65	1.85	Volts
Gate Trigger Current (Continuous dc), Note 1 (Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms)	I_{GT}				mA
MT2(+), G(+)		—	—	70	
MT2(+), G(−)		—	—	70	
MT2(−), G(−)		—	—	70	
MT2(−), G(+)		—	—	100	
*MT2(+), G(+); MT2(−), G(−) T_C = −65°C		—	—	125	
*MT2(+), G(−); MT2(−), G(+) T_C = −65°C		—	—	240	
*Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms)	V_{GT}				Volts
MT2(+), G(+)		—	—	2	
MT2(+), G(−)		—	—	2	
MT2(−), G(−)		—	—	2	
MT2(−), G(+)		—	—	2.5	
*All Quadrants, T_C = −65°C		—	—	3.4	
*Main Terminal Voltage = Rated V_{DRM} = R_L = 10 k ohms, T_C = 100°C		0.2	—	—	
*Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open) (Initiating Current = 150 mA) T_C = 25°C	I_H	—	—	70	mA
*T_C = −65°C		—	—	100	
*Turn-On Time (Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 56 A, Gate Source Voltage = 12 V, R_S = 12 Ohms, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t_{gt}	—	1	2	μs
*Critical Rate-of-Rise of Commutation Voltage (Rated V_{DRM}, I_{TM} = 40 A, Commutating di/dt = 20 A/ms, gate unenergized) T_C = 65°C	dv/dt(c)	5	30	—	V/μs
Critical Rate-of-Rise of Off State Voltage (Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 110°C)	dv/dt				V/μs
2N5444		50			
2N5445		30			
2N5446		20			

*Indicates JEDEC Registered Data for 2N5541 thru 2N5446.

Note 1. All voltage polarities referenced to main terminal 1.

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FIGURE 1 – ON-STATE POWER DISSIPATION

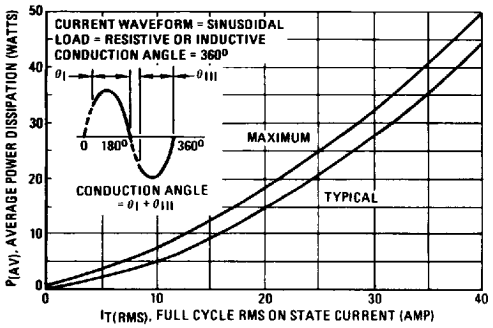

FIGURE 2 – RMS CURRENT DERATING

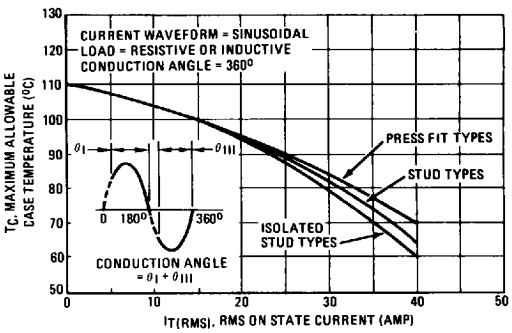

FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

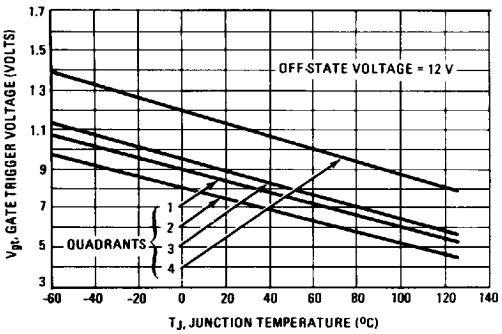

FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

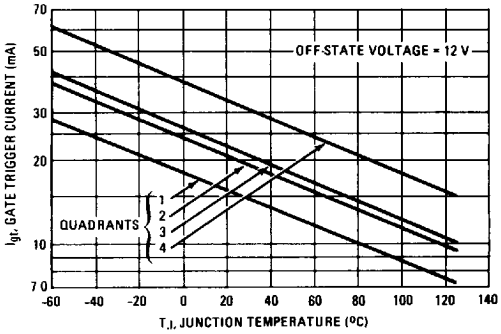

FIGURE 5 – TYPICAL THERMAL RESPONSE

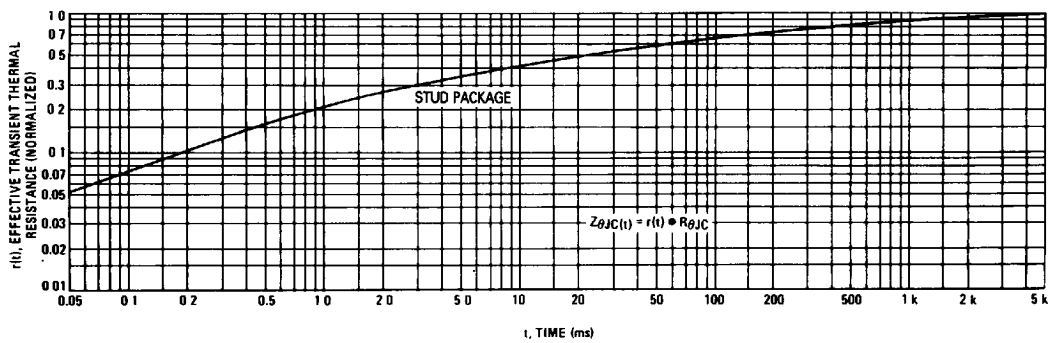

FIGURE 6 – ON-STATE CHARACTERISTICS

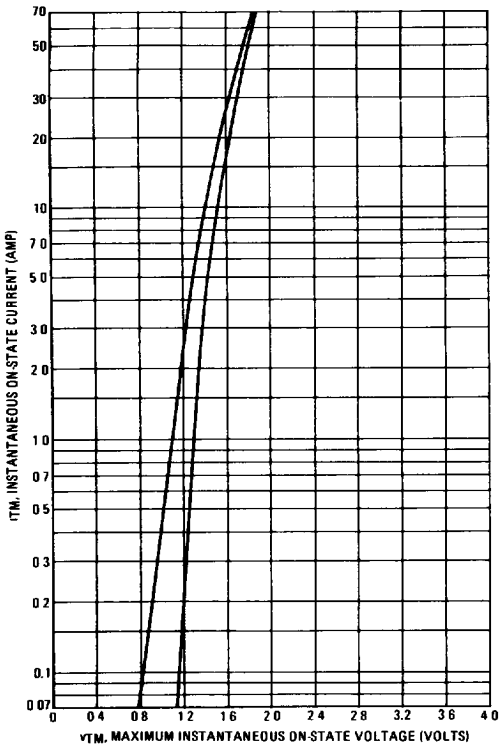

FIGURE 7 – TYPICAL HOLDING CURRENT

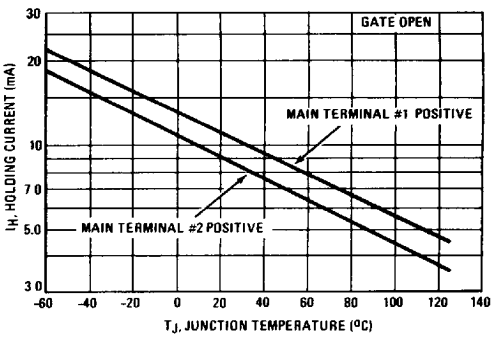

FIGURE 8 – MAXIMUM ALLOWABLE SURGE CURRENT