NCP3063, NCP3063B, NCV3063

1.5 A, Step-Up/Down/ Inverting Switching Regulators

The NCP3063 Series is a higher frequency upgrade to the popular MC34063A and MC33063A monolithic DC−DC converters. These devices consist of an internal temperature compensated reference, comparator, a controlled duty cycle oscillator with an active current limit circuit, a driver and a high current output switch. This series was specifically designed to be incorporated in Step−Down, Step−Up and Voltage−Inverting applications with a minimum number of external components.

Features

- Operation to 40 V Input
- Low Standby Current
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation of 150 kHz
- Precision 1.5% Reference
- New Features: Internal Thermal Shutdown with Hysteresis
  Cycle−by−Cycle Current Limiting
- Pb−Free Packages are Available

Applications

- Step−Down, Step−Up and Inverting supply applications
- High Power LED Lighting
- Battery Chargers

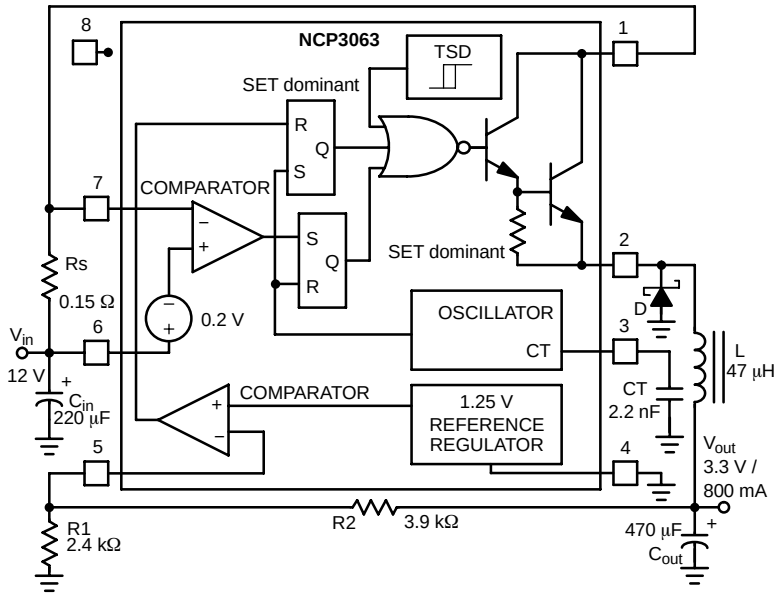


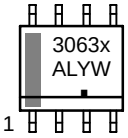
Figure 1. Typical Buck Application Circuit

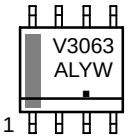
ON Semiconductor®

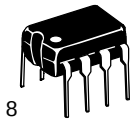
http://onsemi.com

MARKING DIAGRAMS

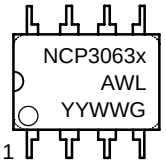
SOIC−8
D SUFFIX
CASE 751

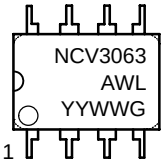


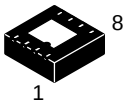




PDIP−8
P, P1 SUFFIX
CASE 626







DFN−8
SUFFIX
CASE 488

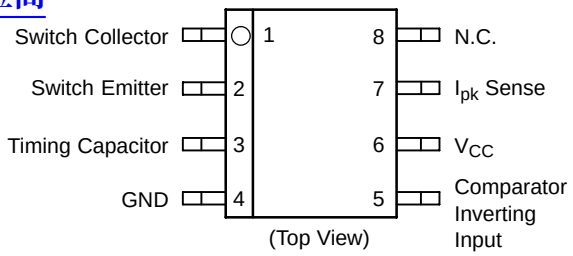
NCP3063x	=	Specific Device Code x = B
A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

PIN CONNECTIONS



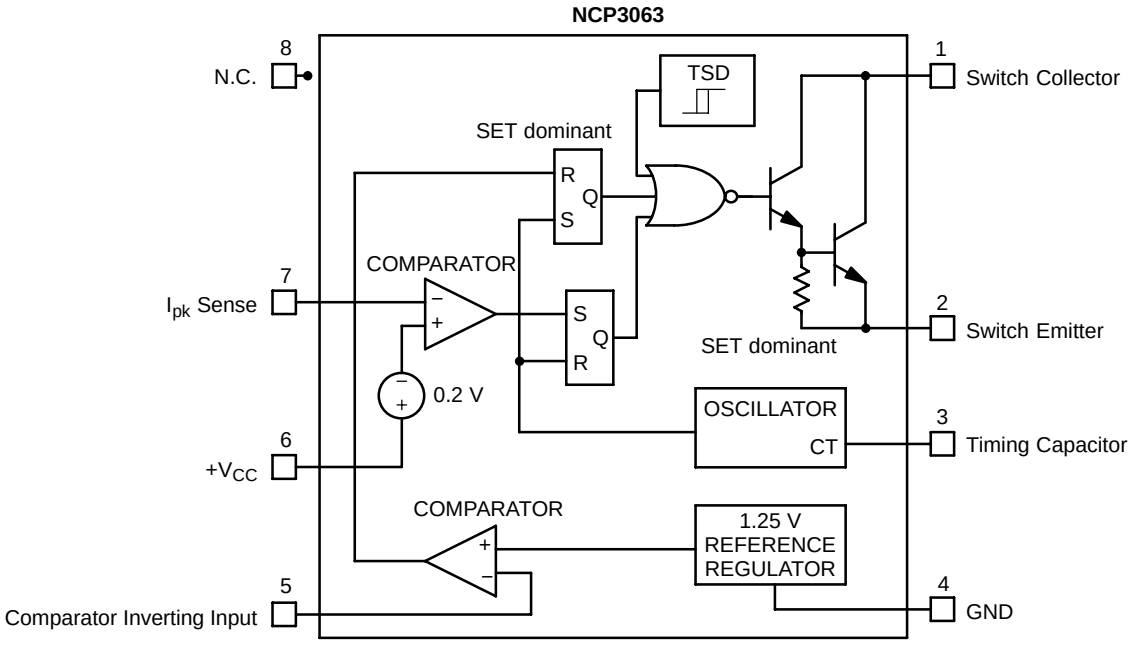


Figure 2. Block Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	Switch Collector	Internal Darlington switch collector
2	Switch Emitter	Internal Darlington switch emitter
3	Timing Capacitor	Timing Capacitor to control the switching frequency
4	GND	Ground pin for all internal circuits
5	Comparator Inverting Input	Inverting input pin of internal comparator
6	V_{CC}	Voltage supply
7	I_{pk} Sense	Peak Current Sense Input to monitor the voltage drop across an external resistor to limit the peak current through the circuit
8	N.C.	Pin not connected

MAXIMUM RATINGS (measured vs. pin 4, unless otherwise noted)

Rating	Symbol	Value	Unit
V_{CC} pin 6	V_{CC}	0 to +40	V
Comparator Inverting Input pin 5	V_{CII}	− 0.2 to + V_{CC}	V
Darlington Switch Collector pin 1	V_{SWC}	0 to +40	V
Darlington Switch Emitter pin 2 (transistor OFF)	V_{SWE}	− 0.6 to + V_{CC}	V
Darlington Switch Collector to Emitter pin 1−2	V_{SWCE}	0 to +40	V
Darlington Switch Current	I_{SW}	1.5	A
I_{pk} Sense pin 7	V_{IPK}	− 0.2 to V_{CC} + 0.2	V
Power Dissipation and Thermal Characteristics			
PDIP−8 Thermal Resistance Junction−to−Air	$R_{\theta JA}$	100	°C/W
SOIC−8 Thermal Resistance Junction−to−Air	$R_{\theta JA}$	180	°C/W
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	$T_{J\ MAX}$	+150	°C
Operating Junction Temperature Range (Note 3) NCP3063 NCP3063B, NCV3063	T_J	 0 to +70 −40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per AEC Q100−002; 003 or JESD22/A114; A115
   Machine Model Method 200 V
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_J = T_A + R_\theta \bullet P_D$
4. The pins which are not defined may not be loaded by external signals

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_J = T_{low} to T_{high} [Note 5], unless otherwise specified)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
f_{OSC}	Frequency	(VPin 5 = 0 V, CT = 2.2 nF, T_J = 25°C)	110	150	190	kHz
I_{DISCHG} / I_{CHG}	Discharge to Charge Current Ratio	(Pin 7 to V_{CC}, T_J = 25°C)	5.5	6.0	6.5	−
$V_{IPK(Sense)}$	Current Limit Sense Voltage	(T_J = 25°C) (Note 6)	165	200	235	mV
OUTPUT SWITCH (Note 7)						
$V_{SWCE(DROP)}$	Darlington Switch Collector to Emitter Voltage Drop	(I_{SW} = 1.0 A, Pin 2 to GND, T_J = 25°C) (Note 7)		1.0	1.3	V
$I_{C(OFF)}$	Collector Off−State Current	(V_{CE} = 40 V)		0.01	100	μA
COMPARATOR						
V_{TH}	Threshold Voltage	T_J = 25°C		1.250		V
		NCP3063	−1.5		+1.5	%
		NCP3063B, NCV3063	−2		+2	%
REG_{LiNE}	Threshold Voltage Line Regulation	(V_{CC} = 5.0 V to 40 V)	−6.0	2.0	6.0	mV
$I_{CII\ in}$	Input Bias Current	(V_{in} = V_{th})	−1000	−100	1000	nA
TOTAL DEVICE						
I_{CC}	Supply Current	(V_{CC} = 5.0 V to 40 V, CT = 2.2 nF, Pin 7 = V_{CC}, VPin 5 > V_{th}, Pin 2 = GND, remaining pins open)			7.0	mA
	Thermal Shutdown Threshold			160		°C
	Hysteresis			10		°C

5. NCP3063: T_{low} = 0°C, T_{high} = +70°C;
   NCP3063B, NCV3063: T_{low} = −40°C, T_{high} = +125°C
6. The $V_{IPK(Sense)}$ Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.
7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
8. NCV prefix is for automotive and other applications requiring site and change control.

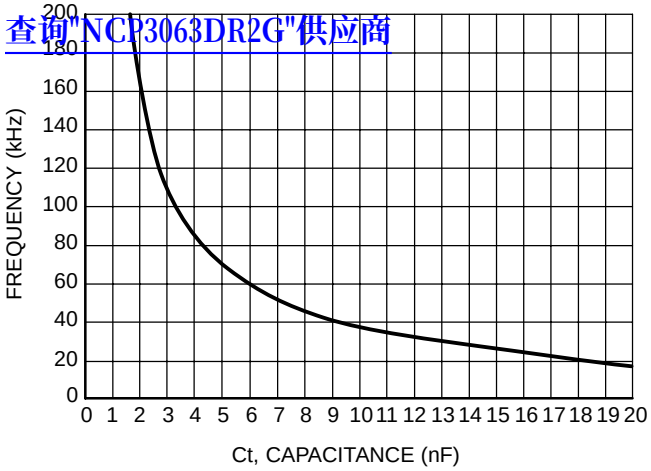


Figure 3. Oscillator Frequency vs. Oscillator Timing Capacitor

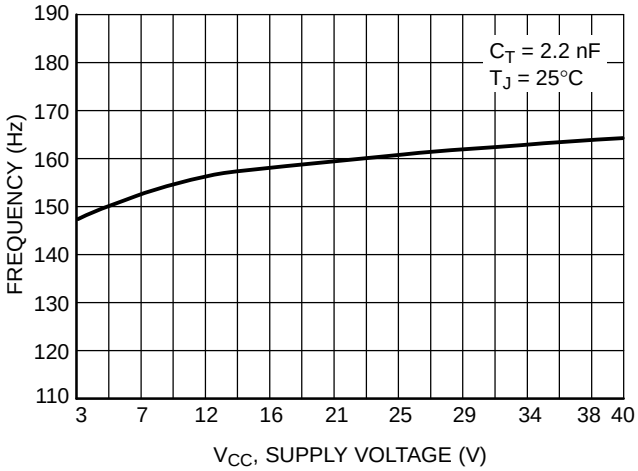


Figure 4. Oscillator Frequency vs. Supply Voltage

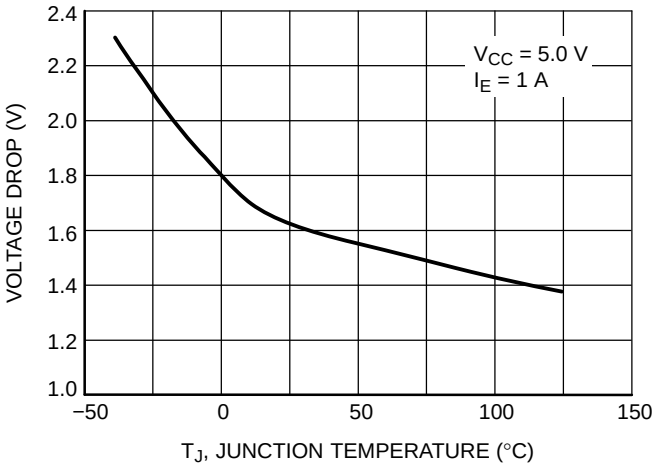


Figure 5. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Temperature

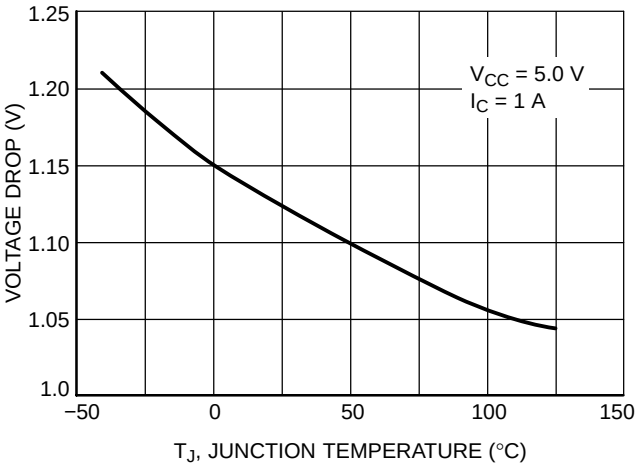


Figure 6. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Temperature

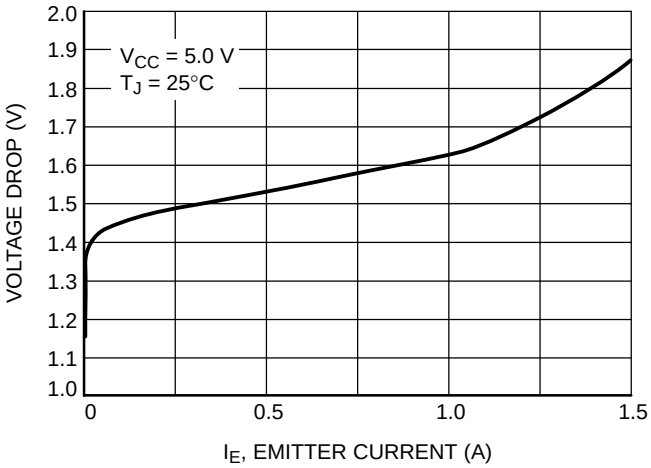


Figure 7. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Emitter Current

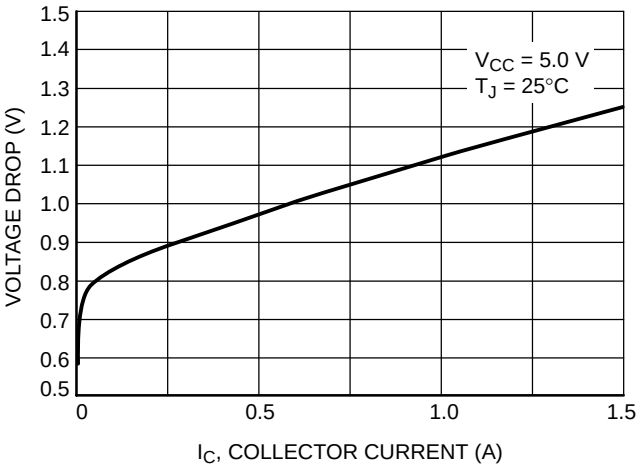


Figure 8. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Collector Current

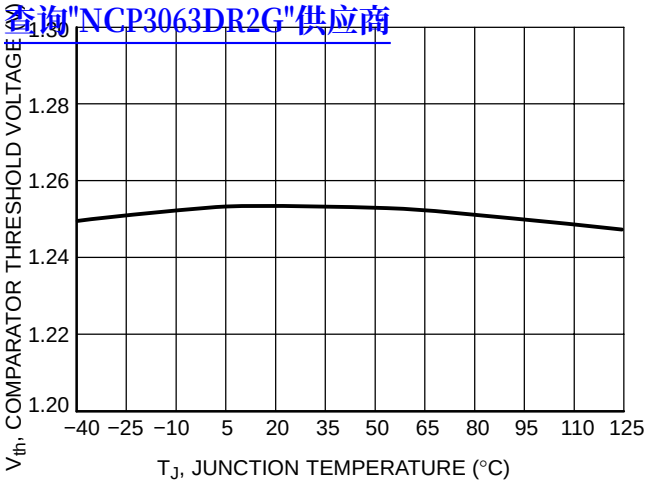


Figure 9. Comparator Threshold Voltage vs. Temperature

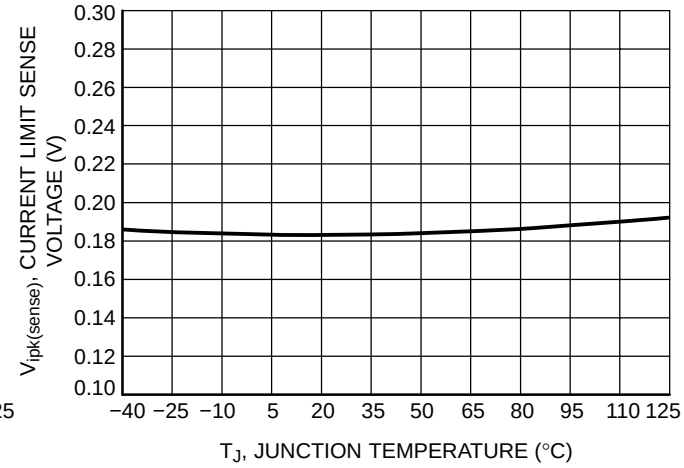


Figure 10. Current Limit Sense Voltage vs. Temperature

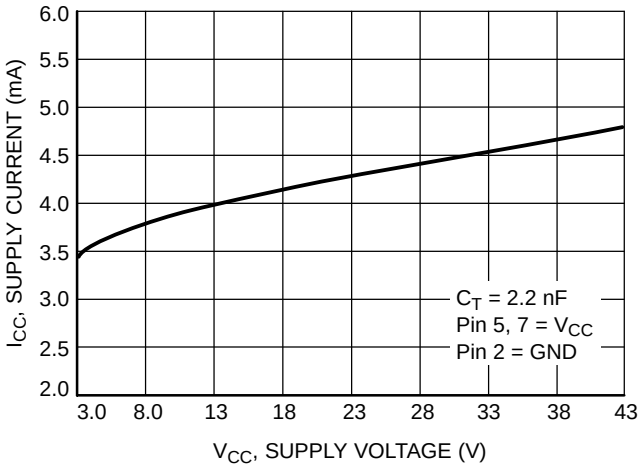


Figure 11. Standby Supply Current vs. Supply Voltage

INTRODUCTION

The NCP3063 is a monolithic power switching regulator optimized for dc to dc converter applications. The combination of its features enables the system designer to directly implement step−up, step−down, and voltage−inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for industrial markets. A representative block diagram is shown in Figure 2.

Operating Description

The NCP3063 is a hysteric, dc−dc converter that uses a gated oscillator to regulate output voltage. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 12. The output voltage waveform shown is for a step−down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the output switch next cycle turning on is inhibited. The feedback comparator will enable the switching immediately when the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be enabled for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles. (See AN920/D for more information).

Oscillator

The oscillator frequency and off−time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a positive going sawtooth waveform at Pin 3. The oscillator peak and valley voltage difference is 500 mV typically. To calculate the C_T capacitor value for required oscillator frequency, use the equations found in Figure 13. An Excel based design tool can be found at www.onsemi.com on the NCP3063 product page.

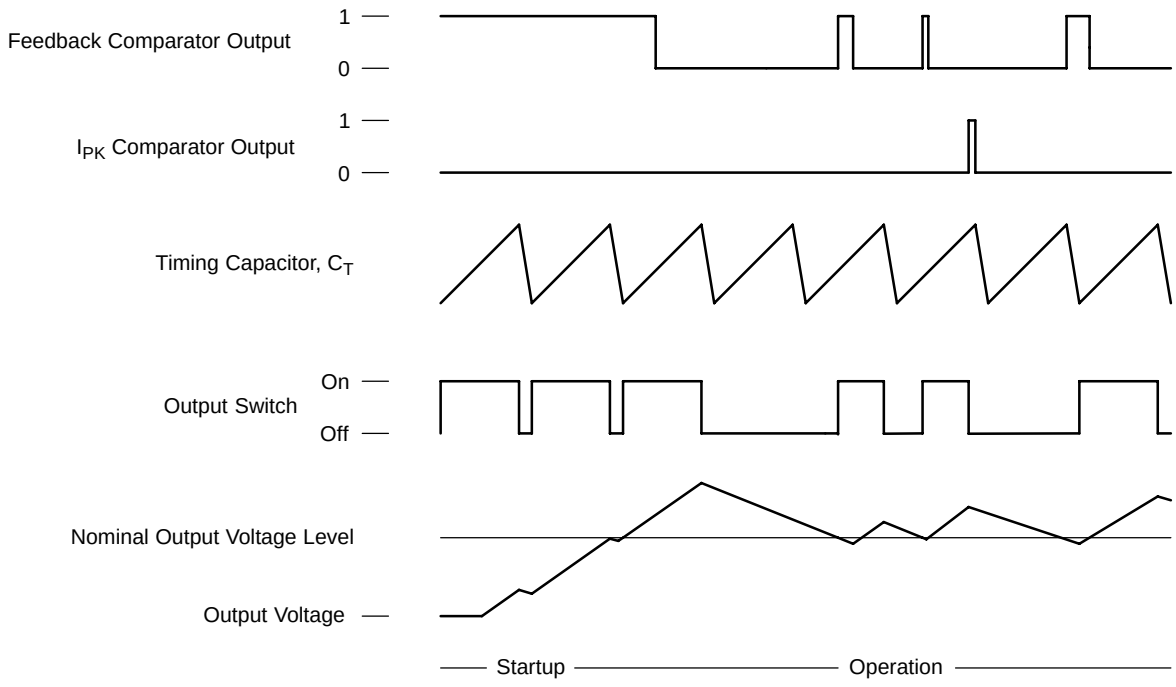
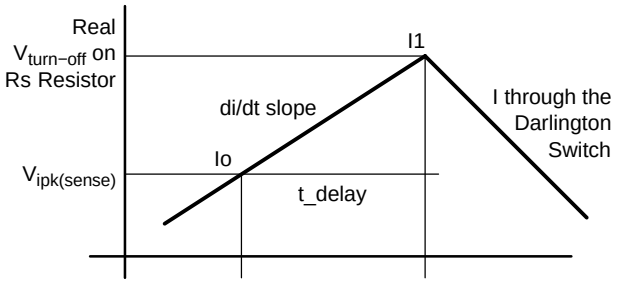


Figure 12. Typical Operating Waveforms

Peak Current Sense Comparator

With a voltage ripple gated converter operating under normal conditions, output switch conduction is initiated by the Voltage Feedback comparator and terminated by the oscillator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the I_{pk} Current Sense comparator will protect the Darlington output Switch. The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and the Darlington output switch. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 200 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle−by−cycle basis. **This Comparator/Latch configuration ensures that the Output Switch has only a single on−time during a given oscillator cycle.**



The $V_{IPK(Sense)}$ Current Limit Sense Voltage threshold is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope.

Real $V_{turn-off}$ on Rsc resistor

$$V_{turn\_off} = V_{ipk(sense)} + Rs \cdot (t\_delay \cdot di/dt)$$

Typical I_{pk} comparator response time t_delay is 350 ns. The di/dt current slope is growing with voltage difference on the inductor pins and with decreasing inductor value.

It is recommended to check the real max peak current in the application at worst conditions to be sure that the max peak current will never get over the 1.5 A Darlington Switch Current max rating.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the Output Switch is disabled. The temperature sensing circuit is designed with 10°C hysteresis. The Switch is enabled again when the chip temperature decreases to at least 150°C threshold. **This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.**

Output Switch

The output switch is designed in a Darlington configuration. This allows the application designer to operate at all conditions at high switching speed and low voltage drop. The Darlington Output Switch is designed to switch a maximum of 40 V collector to emitter voltage and current up to 1.5 A.

APPLICATIONS

Figures 14 through 22 show the simplicity and flexibility of the NCP3063. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 13 gives the relevant design equations for the key parameters. Additionally, a complete application design aid for the NCP3063 can be found at www.onsemi.com.

(See Notes 9, 10, 11)	Step−Down	Step−Up	Voltage−Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in} - V_{SWCE} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{SWCE}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{SWCE}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$C_T = \frac{381.6 \cdot 10^{-6}}{f_{osc}} - 343 \cdot 10^{-12}$		
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$	$\frac{0.20}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{SWCE} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O} + \Delta I_L \cdot ESR$	$\approx \frac{t_{on}\, I_{out}}{C_O} + \Delta I_L \cdot ESR$
V_{out}	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$

The Following Converter Characteristics Must Be Chosen:

V_{in} − Nominal operating input voltage.

V_{out} − Desired output voltage.

I_{out} − Desired output current.

ΔI_L − Desired peak−to−peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f − Maximum output switch frequency.

$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

9. V_{SWCE} − Darlington Switch Collector to Emitter Voltage Drop, refer to Figures 5, 6, 7 and 8.
10. V_F − Output rectifier forward voltage drop. Typical value for 1N5819 Schottky barrier rectifier is 0.4 V.
11. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio.

Figure 13. Design Equations

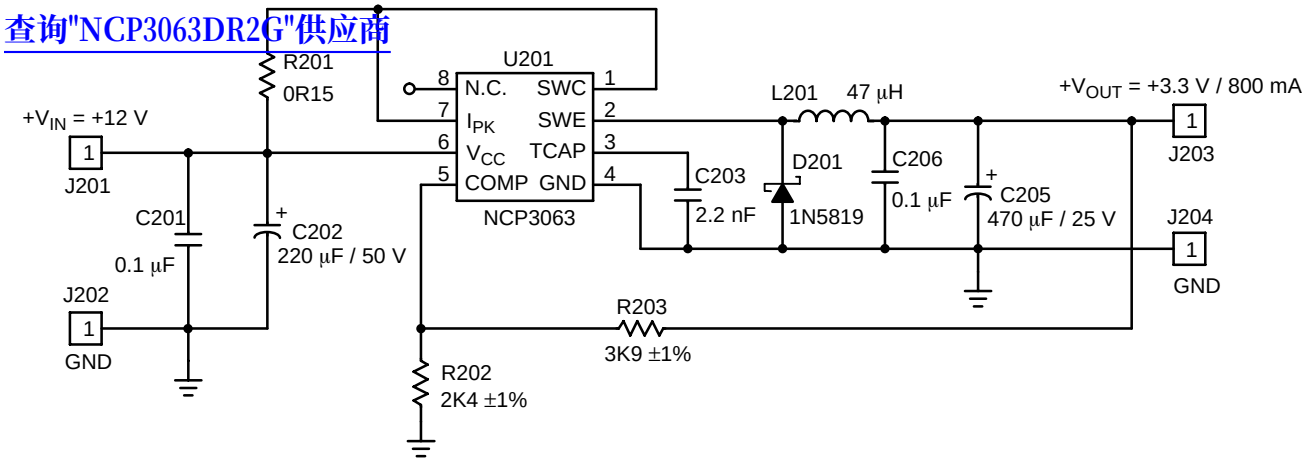


Figure 14. Typical Buck Application Schematic

Value of Components

Name	Value
L201	47 µH, I_{sat} > 1.5 A
D201	1 A, 40 V Schottky Rectifier
C202	220 µF, 50 V, Low ESR
C205	470 µF, 25 V, Low ESR
C203	2.2 nF Ceramic Capacitor

Name	Value
R201	150 mΩ, 0.5 W
R202	2.40 kΩ
R203	3.90 kΩ
C201	100 nF Ceramic Capacitor
C202	100 nF Ceramic Capacitor

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 9 V to 12 V, I_o = 800 mA	8 mV
Load Regulation	V_{in} = 12 V, I_o = 80 mA to 800 mA	9 mV
Output Ripple	V_{in} = 12 V, I_o = 40 mA to 800 mA	≤ 85 mV_{pp}
Efficiency	V_{in} = 12 V, I_o = 400 mA to 800 mA	> 73%
Short Circuit Current	V_{in} = 12 V, R_{load} = 0.15 Ω	1.25 A

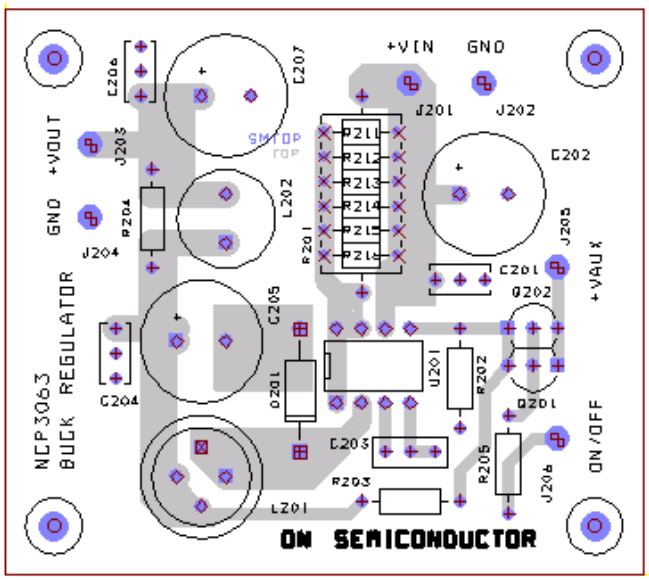


Figure 15. Buck Demoboard Layout

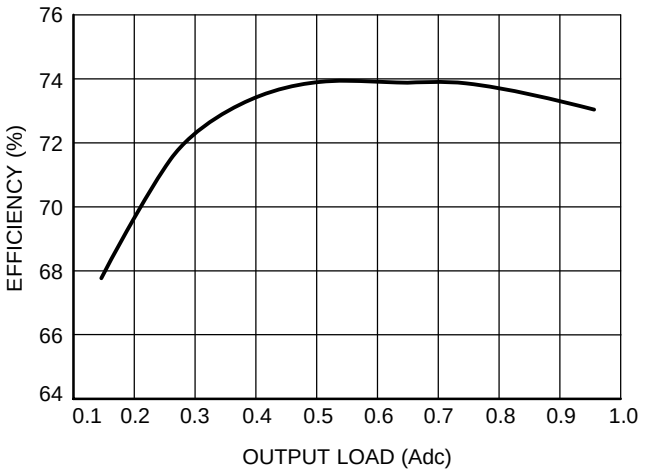


Figure 16. Efficiency vs. Output Current for the Buck Demo Board at V_{in} = 12 V, V_{out} = 3.3 V, T_A = 25°C

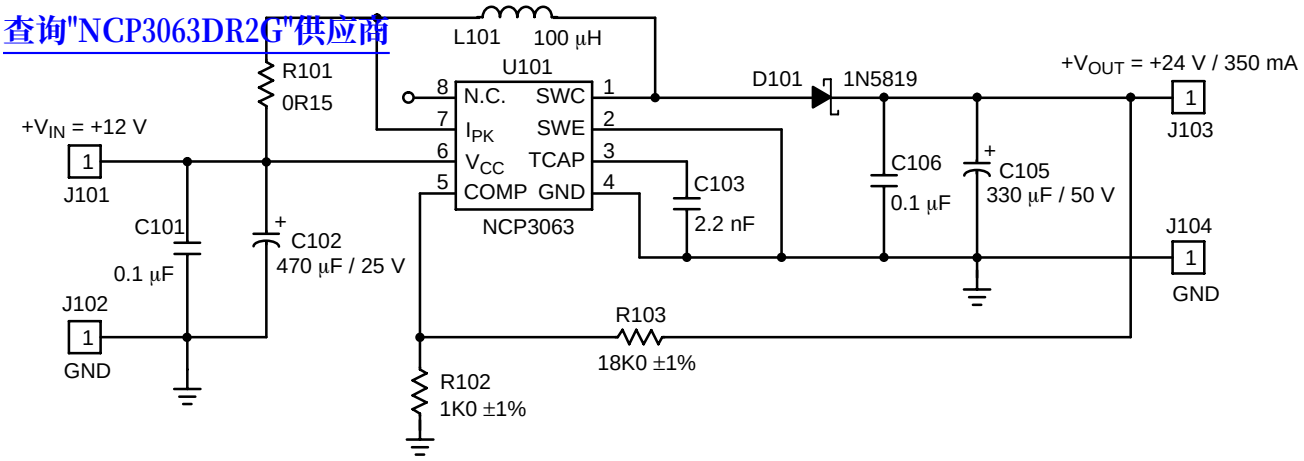


Figure 17. Typical Boost Application Schematic

Value of Components

Name	Value
L101	100 µH, I_{sat} > 1.5 A
D101	1 A, 40 V Schottky Rectifier
C102	470 µF, 25 V, Low ESR
C105	330 µF, 50 V, Low ESR
C103	2.2 nF Ceramic Capacitor

Name	Value
R101	150 mΩ, 0.5 W
R102	1.00 kΩ
R103	18.00 kΩ
C101	100 nF Ceramic Capacitor
C106	100 nF Ceramic Capacitor

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 9 V to 15 V, I_o = 250 mA	2 mV
Load Regulation	V_{in} = 12 V, I_o = 30 mA to 350 mA	5 mV
Output Ripple	V_{in} = 12 V, I_o = 10 mA to 350 mA	≤ 350 mV_{pp}
Efficiency	V_{in} = 12 V, I_o = 50 mA to 350 mA	> 85.5%

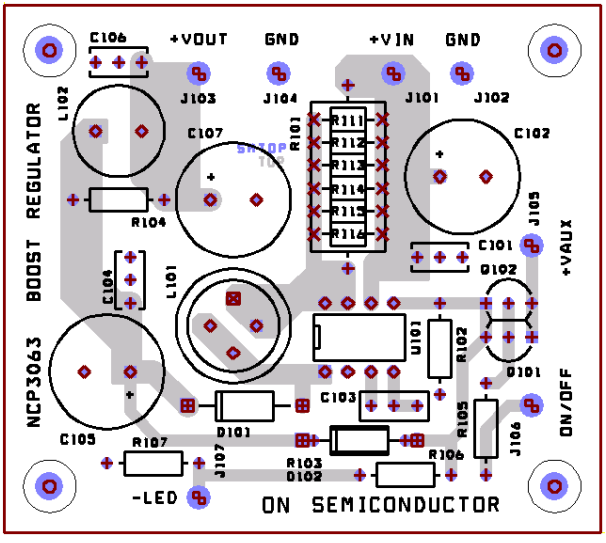


Figure 18. Boost Demoboard Layout

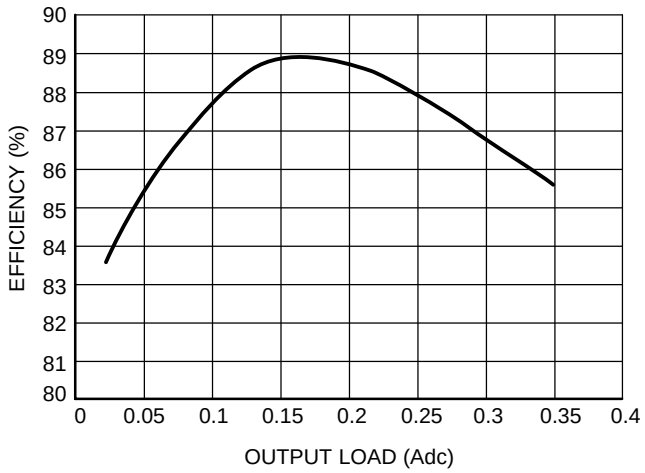


Figure 19. Efficiency vs. Output Current for the Boost Demo Board at V_{in} = 12 V, V_{out} = 24 V, T_A = 25°C

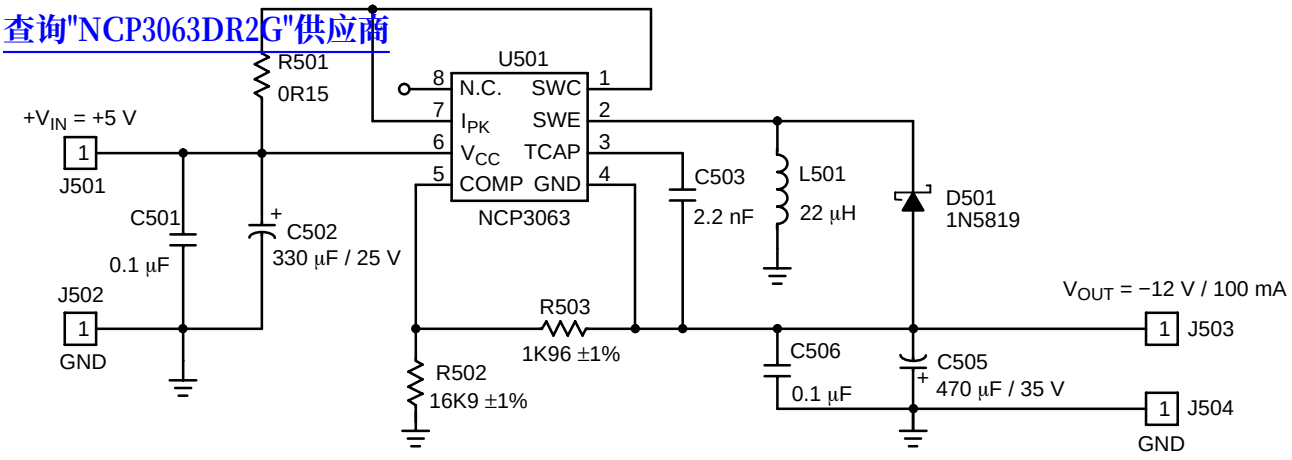


Figure 20. Typical Voltage Inverting Application Schematic

Value of Components

Name	Value
L501	22 µH, I_{sat} > 1.5 A
D501	1 A, 40 V Schottky Rectifier
C502	330 µF, 25 V, Low ESR
C505	470 µF, 35 V, Low ESR
C503	2.2 nF Ceramic Capacitor

Name	Value
R501	150 mΩ, 0.5 W
R502	16.9 kΩ
R503	1.96 kΩ
C501	100 nF Ceramic Capacitor
C506	100 nF Ceramic Capacitor

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 4.5 V to 6 V, I_o = 50 mA	1.5 mV
Load Regulation	V_{in} = 5 V, I_o = 10 mA to 100 mA	1.6 mV
Output Ripple	V_{in} = 5 V, I_o = 0 mA to 100 mA	≤ 300 mV_{pp}
Efficiency	V_{in} = 5 V, I_o = 100 mA	49.8%
Short Circuit Current	V_{in} = 5 V, R_{load} = 0.15 Ω	0.885 A

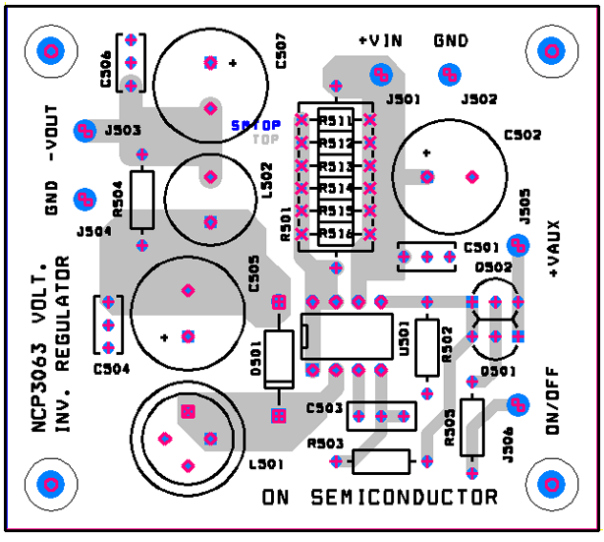


Figure 21. Voltage Inverting Demoboard Layout

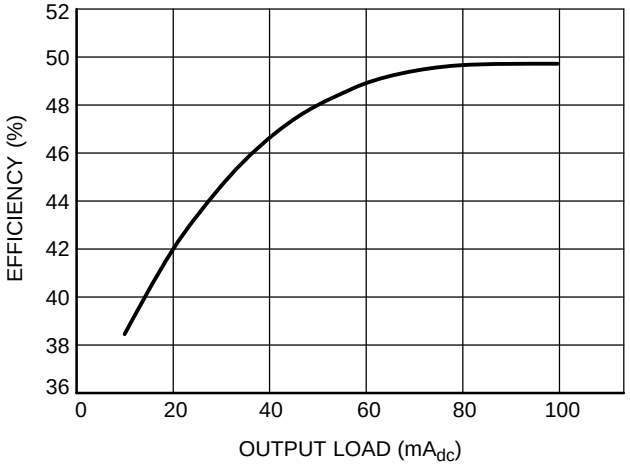


Figure 22. Efficiency vs. Output Current for the Voltage Inverting Demo Board at V_{in} = +5 V, V_{out} = −12 V, T_A = 25°C

ORDERING INFORMATION

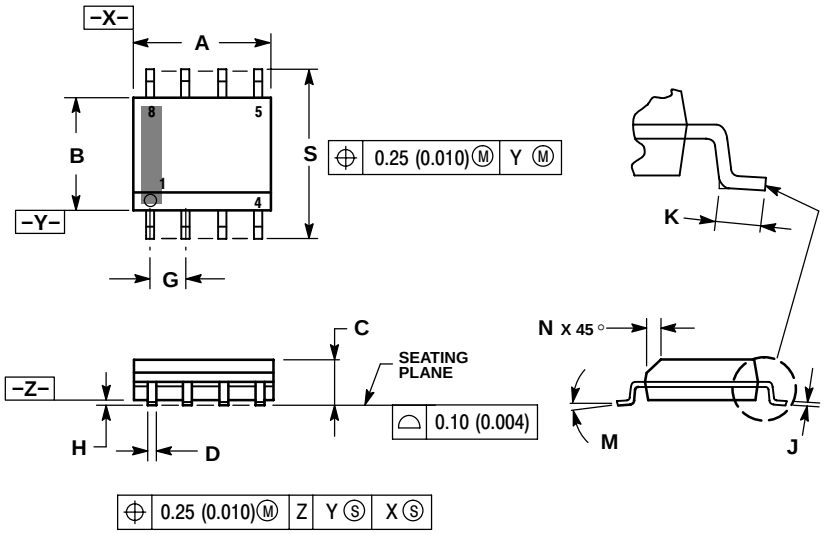
Device	Package	Shipping†
NCP3063PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP3063BPG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP3063DR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCP3063BDR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCP3063	DFN−8 (Pb−Free)	TBD
NCV3063PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCV3063DR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV prefix is for automotive and other applications requiring site and change control.

PACKAGE DIMENSIONS

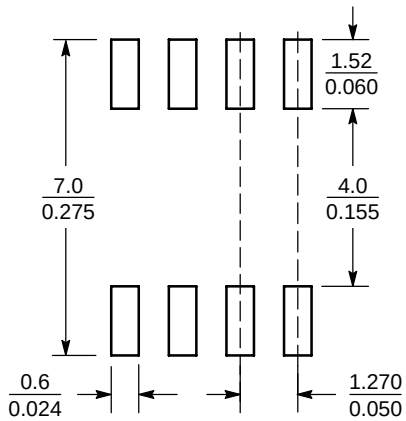
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

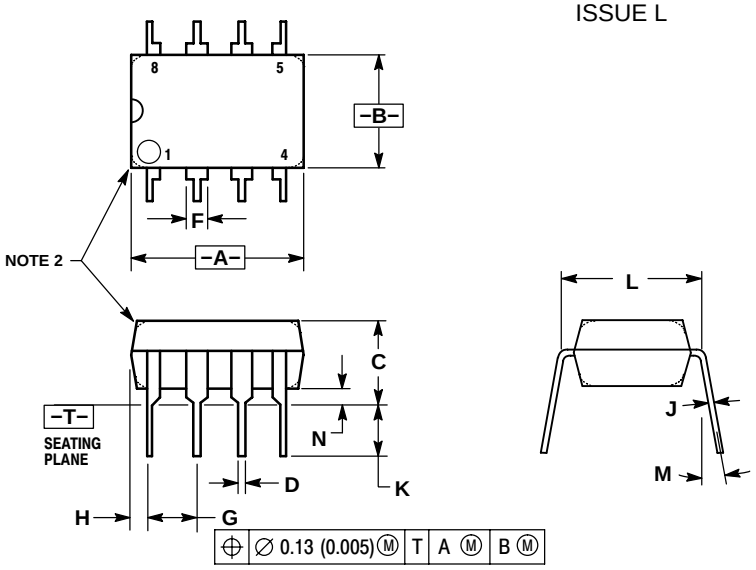


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

8 LEAD PDIP
CASE 626−05
ISSUE L



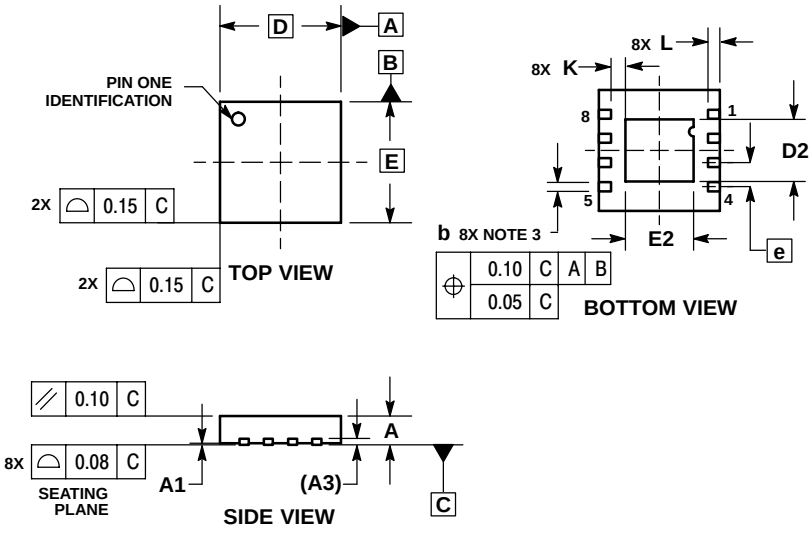
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

PACKAGE DIMENSIONS

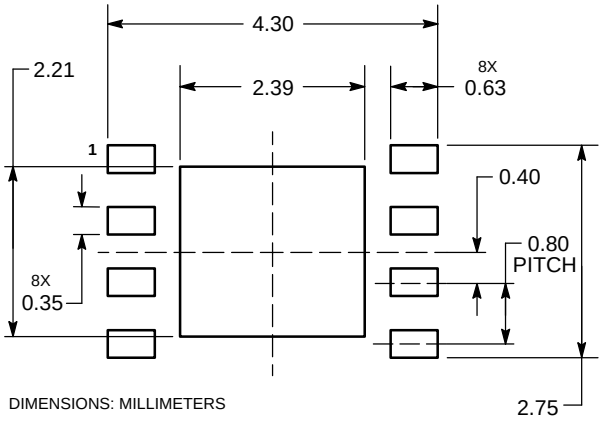
8 PIN DFN, 4x4
CASE 488AF−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	−−−
L	0.30	0.50

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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