EM78815

8 Bit Microcontroller

Product Specification

DOC. VERSION 2.4

ELAN MICROELECTRONICS CORP.

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Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	
1.1	Changed the FSK, DTMF and CW Power Control	2003/03/04
2.0	1. Removed the 256K byte data ROM 2. Removed the expand program/data memory interface 3. Embedded 1.2%, 2.0% and 5.5% CAS frequency range deviation	
2.1	1. Added 256K byte data ROM 2. Added expand program/data memory interface 3. Removed 1.2% CAS frequency range deviation 4. Removed UART function	
2.2	Modified the Current DA resolution from 7 bit to 10 bit	2003/08/19
2.3	Added UART function	2003/10/08
2.4	1. Removed Idle mode 2. Added application note item 7	2006/02/17

1 General Description

The EM78815 is an 8-bit CID (Call Identification) RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on chip watchdog (WDT), programmable real time clock/counter, external/internal interrupt, power down mode, EMC65132 LCD controller, FSK decoder, Call waiting decoder, Energy Detector (DED) , DTMF receiver, Programming Tone generator, build-in Keytone clock generation, Comparator and tri-state I/O. The EM78815 provides a single chip solution to design a CID of calling message display.

2 Features

2.1 CPU

- Operating voltage range: 2.2V~3.6V(Normal mode), 2.0V~3.6V(Green mode)
- 64K×13 on-chip Program ROM, supports a max. of 128K word program
- 256K×8 on-chip data ROM, supports a max. of 2M byte data
- 4Kx8 data RAM
- 128×8 common register
- Up to 56 bidirectional tri-state I/O ports
- IO with internal Pull high, wake-up and interrupt functions
- Stack: 24-level stack for subroutine nesting
- TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
- Counter 1: 16 bit counter with 8-bit prescaler can be an interrupt source
- Counter 2: 8-bit counter with 8-bit prescaler can be an interrupt source
- Watchdog: Programmable free running on-chip watchdog timer
- CPU modes:

Mode	CPU Status	Main Clock	32.768kHz Clock Status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- 15 interrupt source: 8 external, 7 internal
- Key Scan: Port key scan function up to 16×4 keys
- Sub-Clock: 32.768kHz crystal
- Main-clock: 3.5862MHz multiplied by 0.5, 1, 1.5 or 3 generated by internal PLL
- Keytone output: 4kHz, 2kHz, 1kHz (shared with IO)
- Comparator: 3-channel comparators, internal (16 level) or external reference voltage (shared with IO)

2.2 Serial Transmitter/Receiver Interface

- Serial Peripheral Interface (SPI): Interrupt flag available for the read buffer full, Programmable baud rates of communication, Three-wire synchronous communication (shared with IO)
- Universal asynchronous receiver transmitter interface. User can select (7/8/9 bits) with/without parity bit, Baud rate setting and error detection function. Interrupt available for RX buffer full or TX buffer empty. Two wire asynchronous communication (shared with IO)

2.3 Current D/A

- Operating Voltage: 2.5V~3.6V
- 10-bit resolution and 3-bit output level control
- Current DA output can drive the speaker through a transistor for sound playing. (shared with IO)

2.4 Programmable Tone Generators

- Operating Voltage: 2.2V~3.6V
- Programmable Tone 1 and Tone 2 generators
- Independent single tone generation for Tone 1 and Tone 2
- Mixed dual tone generation by Tone 1 and Tone 2 with 2dB difference
- Can be programmed for DTMF tone generation
- Can be programmed for FSK signal (Bell202 or V.23) generation

2.5 CID

- Operating Voltage: 2.4V~3.6V for FSK
- Operating Voltage: 2.4V~3.6V for DTMF receiver
- Compatible with Bellcore GR-30-Core (formerly as TR-NWT-000030)
- Compatible with British Telecom (BT) SIN227 & SIN242
- FSK demodulator for Bell 202 and ITU-T V.23 (formerly as CCITT V.23)
- Differential Energy Detector (DED) for line energy detection

2.6 Call Waiting

- Operating Voltage: 2.4V~3.6V
- Compatible with Bellcore special report SR-TSV-002476
- Call-Waiting (2130Hz plus 2750Hz) Alert Signal Detector
- Good talk-down and talk-off performance
- Sensitivity compensated by adjusting input OP gain

2.7 External LCD controller (64 × 256 dot max for a pair of Master and Slave LCD Driver)

- Multi-chip operation (Master, Slave) available for external LCD device

2.8 Package Type

- 105-pin Chip: EM78815H
- 128-pin QFP: (EM78815AQ, POVD disable) (EM78815BQ, POVD enable)

3 Application

- SMS phone
- Feature phones

4 Pin Configuration

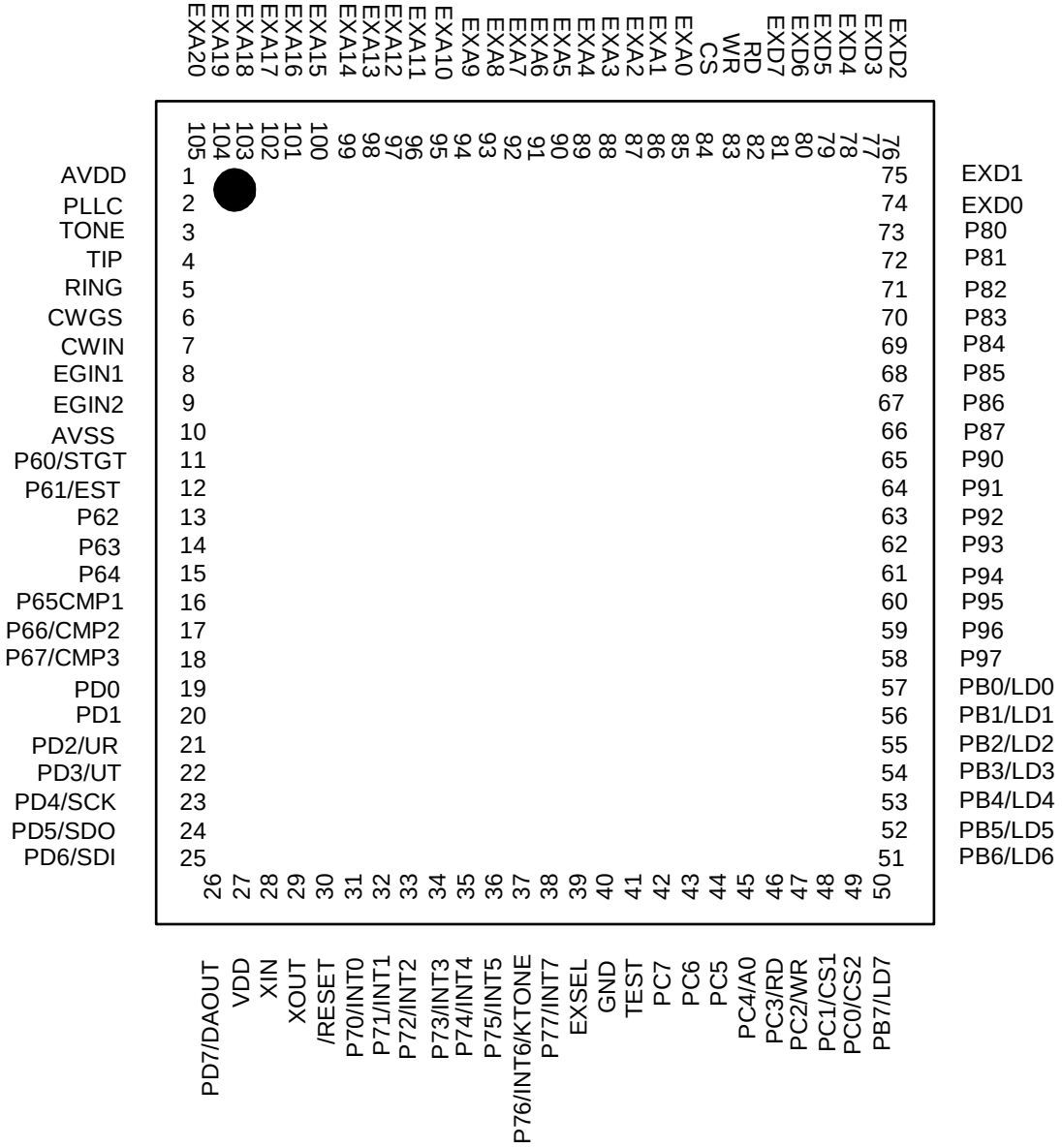


Fig.1a 105-pin Chip Assignment

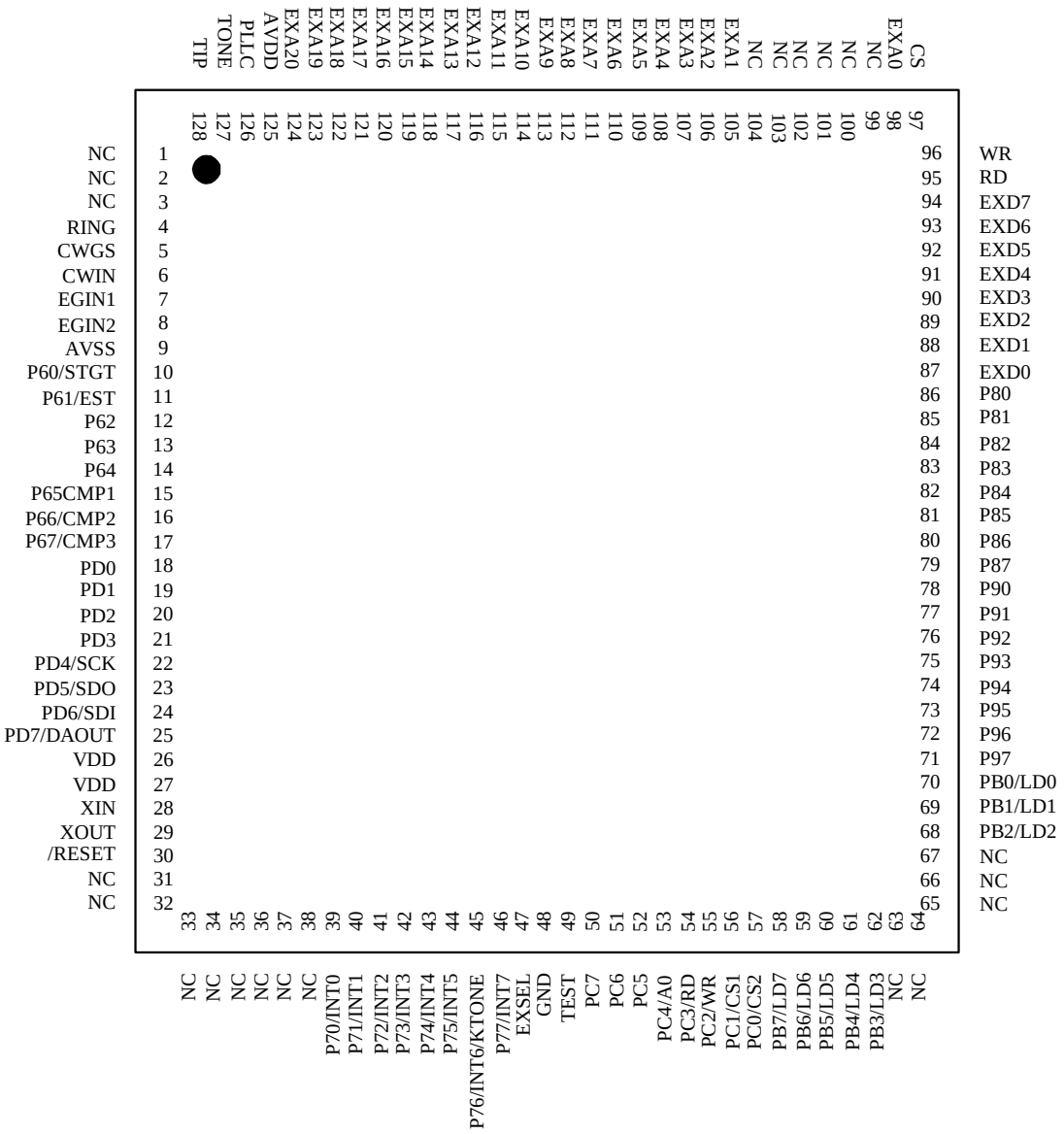


Fig. 1b 128-pin QFP Assignment

5 Functional Block Diagram

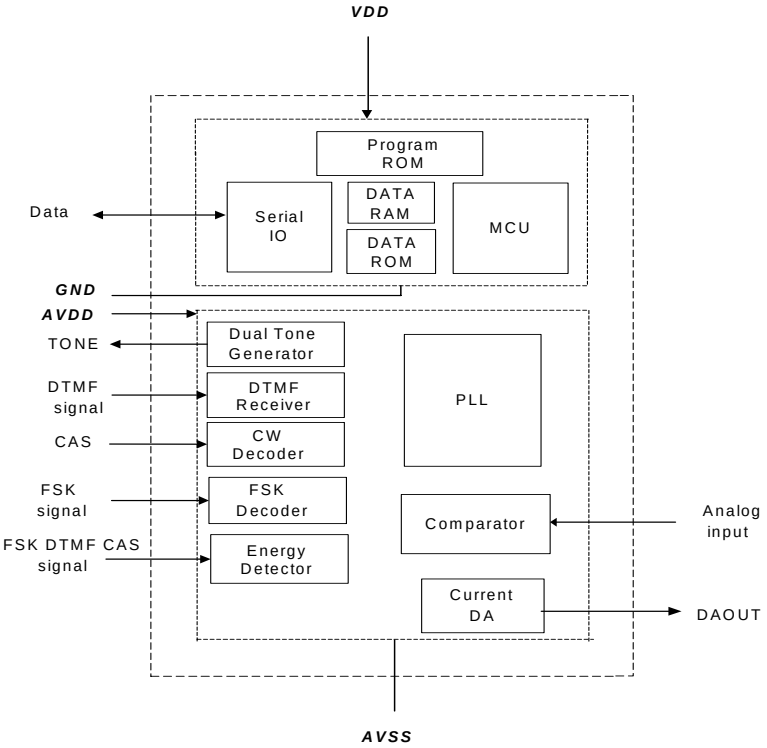


Fig. 2 Block Diagram 1

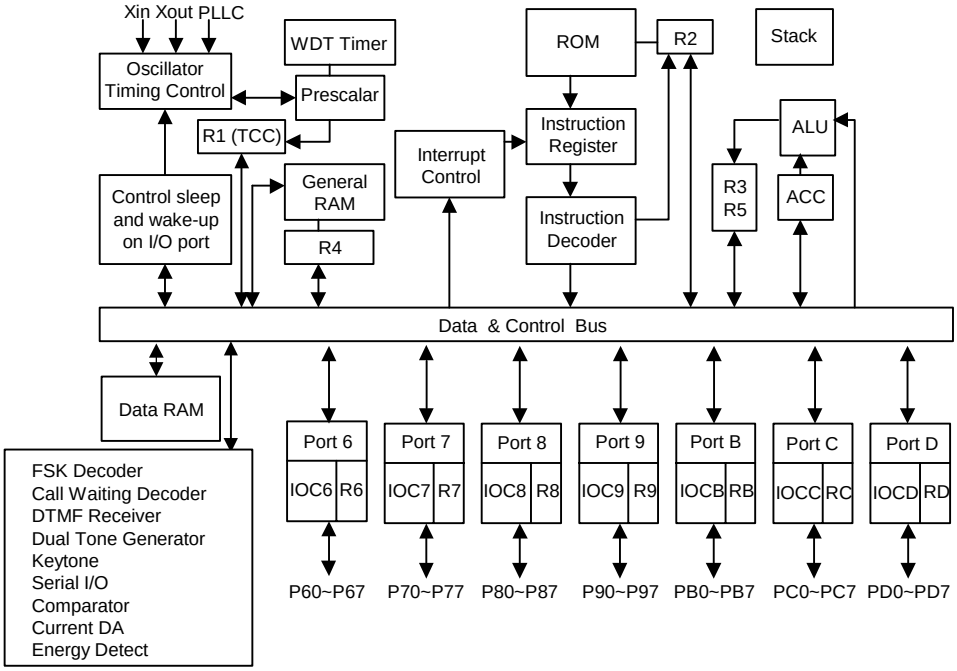


Fig. 3 Block Diagram 2

6 Pin Descriptions

6.1 Power Pin

Pin	I/O	Description
VDD	Power	Digital Power
AVDD	Power	Analog Power
GND	Power	Digital Ground
AVSS	Power	Analog Ground

6.2 Clock Pin

Pin	I/O	Description
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase lock loop capacitor, connect a 0.01µ capacitor to 0.047µ with GND.

6.3 External LCD Device Control Pin

Pin	I/O	Description
LCDD0~LCDD7	I/O	External LCD driver data bus. This is pin-shared with Port B0~Port B7.
/WR	O	Write enable output (active low signal). This is pin-shared with Port C2.
/RD	O	Read enable output (active low signal). This is pin-shared with Port C3.
A0	O	Used as register selection. When A0 is equal to 1, the data bus transmits LCD Data. When A0 is equal to 0, the data bus transmits LCD Address. This is pin-shared with Port C4.
/CS1 ~ /CS2	O	Chip Select signal output. This is pin-shared with Port C1~ Port C0

6.4 FSK, CW

Pin	I/O	Description
TIP	I	Should be connected to the TIP side of the twisted pair lines for FSK.
RING	I	Should be connected to the RING side of the twisted pair lines for FSK.
CWGS	O	Gain adjustment of single-ended input OP Amp.
CWIN	I	Single-ended input OP Amp for call waiting decoder.

6.5 DTMF Receiver, OP

Pin	I/O	Description
EST	O	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause the EST to return to a logic low. This is pin-shared with Port 61.
STGT	I/O	Steering input/guard time output (bi-directional). A voltage greater than Vtst detected at ST causes the device to register the detected tone-pair and update the output latch. A voltage less than Vtst frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of EST and the voltage on ST. This is pin-shared with Port 60.

6.6 Serial IO, Comparator, Current DA, Tone

Pin	I/O	Description
SCK	I/O	Master: output pin, Slave: input pin. This is pin-shared with Port D4.
SDO	O	Output pin for serial data transferring. This is pin-shared with Port D5.
SDI	I	Input pin for receiving data. This is pin-shared with Port D6.
UR	I	Data receiver pin for UART. This pin shared with Port D2
UT	O	Data transmitter pin for UART. This is pin-shared with Port D3.
CMP1	I	Comparator input pins. This is pin-shared with Port 65.
CMP2	I	Comparator input pins. This is pin-shared with Port 66
CMP3	I	Comparator input pins. This is pin-shared with Port 67.
DAOUT	O	Current DA output pin. It can be a control signal for sound generation. This is pin-shared with Port D7.
KTONE	O	Key tone output. This is pin-shared with Port 76.
TONE	O	Dual tone output pin

6.7 IO

Pin	I/O	Description
P60 ~P67	I/O	Each bit in Port 6 can be Input or Output port. Internal pull high.
P70 ~ P77	I/O	Each bit in Port 7 can be Input or Output port. Internal Pull high function, Auto key scan function, and Interrupt function.
P80 ~ P87	I/O	Each bit in Port 8 can be Input or Output port.
P90 ~ P97	I/O	Each bit in Port 9 can be Input or Output port.
PB0 ~ PB7	I/O	Each bit in Port B can be Input or Output port.
PC0 ~ PC7	I/O	Each bit in Port C can be Input or Output port.
PD0 ~ PD7	I/O	Each bit in Port D can be Input or Output port. This is pin-shared with SPI pin and CMP input pin.
P70 ~ P76	I	Interrupt sources. When any pin from Port 70 to Port 76 has a falling edge signal, it will generate a corresponding interrupt.
P77	I	Interrupt source. Once Port 77 has a falling edge or rising edge signal (controlled by CONT register), it will generate an interrupt.
/RESET	I	Low reset

6.8 Expand Program/Data ROM Interface

Pin	I/O	Description
EXD0 ~ EXD7	I/O	Expand Program/Data memory Data Bus
/RD	O	Expand Program/Data memory Read request output
/WR	O	Expand Program/Data memory Write request output
/CS	O	Expand Program/Data memory CS request output
EX0~EXA20	O	Expand Program/Data memory Address Bus
EXSEL	I	**0/1** → Internal 64K Program ROM used/unused

EXSEL pin : **0/1** → On-chip program ROM used/unused switch.

The EM78815 supports a max. of 128K Program. User can support program for both 64K EM78815 on-chip ROM and 64K expanded ROM. User can also ignore the 64K EM78815 on-chip ROM and support all programs for an external 128K ROM. Using this function, user can easily upgrade programs or download new functions.

The EM78815 provides Data ROM expanded function. When user access data of which address is over 256K, the external ROM will be loaded. User must set the expanded start address of the Data ROM to RF Page 1, Page 2 and IOCB Page 1. A diagram of the expanded function is shown below.

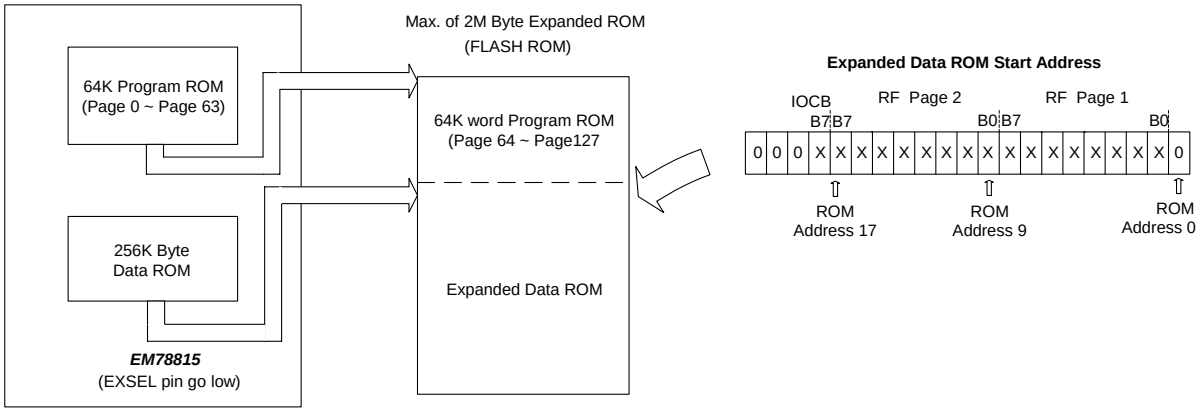


Fig. 4a EXSEL = 0, Both Internal and External Programs are Used

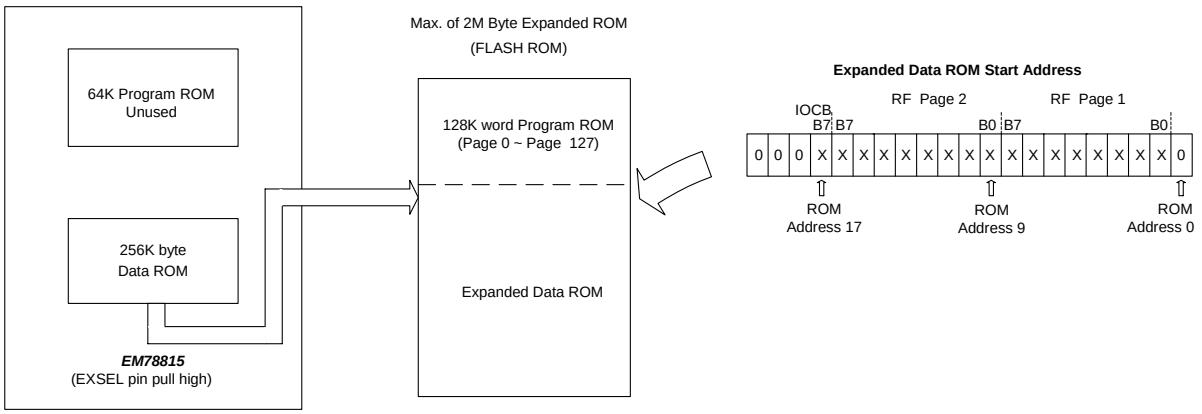


Fig. 4b EXSEL = 1, Only External Program is Used

Setting the expanded Data ROM's Starting Address

The EM78815 supports a maximum of 2M Bytes expanding data memory, but user must fix the start address of the external program at 0x00000 and set the start address of the expanded Data ROM since the program ROM size is adjustable. In this way, the MCU will get data from the external memory if the data ROM is over 256K.

The instruction width is 13 bits and the data bus for external memory is 8 bits, so an instruction will capture two address sizes and the LSB address of the start address at the external ROM will be 0. Besides, the EM78815 only supports a max of 128K program, so the start address of the Data ROM will be smaller than 256K+2 and A20, A19 and A18 will also be 0. User must set the expanded start address of the Data ROM at A17~A1 to IOCB Page 2, Bit 7, RF Page 3 and RF Page 2.

7 Function Description

7.1 Operational Register

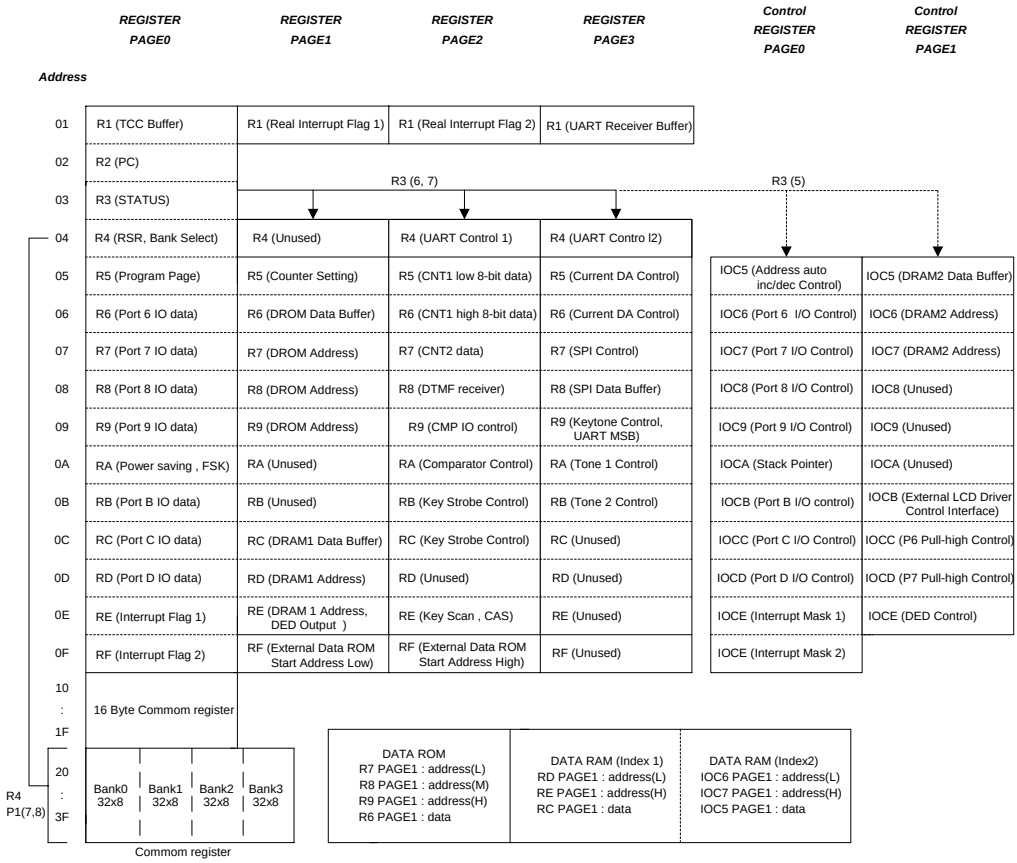


Fig. 5 Control Register Configuration

7.2 Operational Register Detail Description

7.2.1 R0 Indirect Addressing Register

R0 is not a physically implemented register. It is provided as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed to by the RAM Select Register (R4).

Example:

```
mov     A  ,  @0x20       ;store an address at R4 for indirect
                          ;addressing
mov     0x04 ,  A
mov     A  ,  @0xAA       ;write data 0xAA to R20 at Bank 0
                         ;through R0
mov     0x00 ,  A
```

7.2.2 R1 Page 0 TCC Data Buffer

This is increased by 16.38 kHz or by the instruction cycle clock (controlled by CONT register). Written and read by the program as any other register.

7.2.3 R1 Page 1 Interrupt Flag 1 Real Value

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTR7	INTR6	INTR5	INTR4	INTR3	INTR2	INTR1	INTR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(INTR0~INTR7) : Interrupt Flag 1 real value. User can clear this page from 1 to 0 but cannot set this register to 1. The relation of R1 Page1, RE Page 0 and IOCE Page 0 is shown in the figure. When user disables the interrupt mask, whether an interrupt occurs or not, the interrupt flag (RE Page 0) will appear "0". Opposite of RE Page 0, R1 Page 1 will show real interrupt occur status regardless whether this interrupt mask is enabled or disabled. ***User can clear the corresponding external interrupt flag in RE Page 0 or R1 Page 1.***

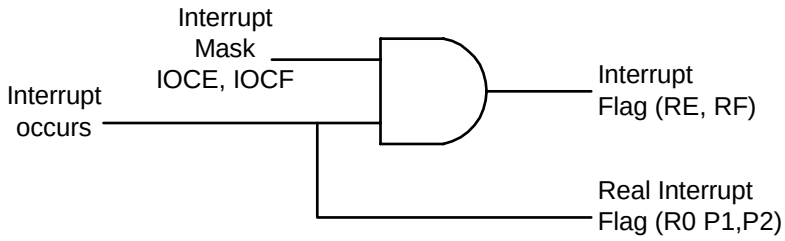


Fig. 6 Relationship between Interrupt Mask, Flag and Real Flag

7.2.4 R1 Page 2 Interrupt Flag 2 Real Value

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF/STD	FSK/CW	-	UART	DED	CNT2	CNT1	TCC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 (Internal Interrupt Flag Real Value) : Interrupt Flag 1 real value. User can clear this page from 1 to 0 but cannot set this register to 1. The relationship between R1 Page 2, RF Page 0 and IOCF Page 0 is shown in Fig. 6. When user disables an interrupt mask, whether an interrupt occurs or not, the interrupt flag (RF Page 0) will appear "0". Opposite of RF Page 0, R1 Page 1 will show real interrupt occur status regardless whether this interrupt mask is enabled or disabled. ***User can clear the corresponding interrupt flag in RF Page 0 or R1 Page 2.***

7.2.5 R1 Page 3 UART Receiver Data Buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URR7	URR6	URR5	URR4	URR3	URR2	URR1	URR0
R	R	R	R	R	R	R	R

Bit 0~Bit 7(URR0~URR7) : UART receiver low 8 bit data buffer. UART receiver data buffer is a read-only register.

7.2.6 R2 Program Counter

There are 128K × 13 External Program ROM addresses at the relative programming instruction codes. The structure is depicted on Fig. 5.

"JMP" instruction allows a direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then pushed into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits do not change. The most significant bit (A10~A14) will be loaded with the contents of bits PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2,A" instruction.

If there is an interrupt trigger, the Program ROM will jump to Address 8 at Page 0. The CPU will store ACC, R3 status and R5 Page automatically, it will restore after instruction RETI.

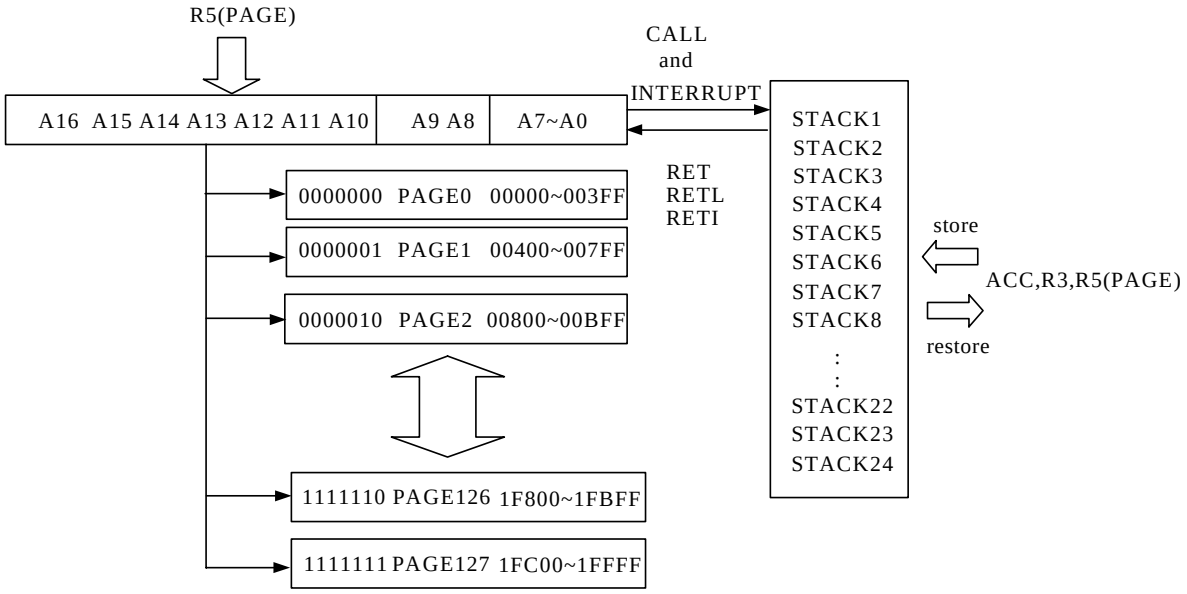


Fig. 7 Program Counter Organization

7.2.7 R3 Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RS1	RS0	IOCS	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 (C) : Carry

Bit 1 (DC) : Auxiliary carry flag

Bit 2 (Z) : Zero flag

Bit 3 (P) : Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	×	×	×: don't care

Bit 5 (IOCS) : IOC register select bit. Change IOC5 ~ IOCE to another page

Bit 6~Bir 7 (RS0 ~ RS1) : R register select bits. Change R1, R2, R4 ~ RE to another page.

RS1	RS0	R Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

7.2.8 R4 RAM Select for Common Registers R20~R3F, UART Control Register

7.2.8.1 Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks of the 32 registers (R20 to R3F).

Refer to Fig. 4 Control Register Configuration for details.

7.2.8.2 Page 1 Undefined Register

This register is un*implemented, not *for use.

7.2.9 Page 2 UART Control Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRS2	TRS1	TRS0	URM1	URM0	ERE	TXE	RXE

Bit 0 (RXE) : Enable UART receiving function & UART interrupt mask

1 → Enable

0 → Disable

Bit 1 (TXE) : Enable UART transmission function & UART interrupt mask

1 → Enable

0 → Disable

Bit 2 (ERE) : Enable UART receiver error interrupt mask

ERR	TXE	REX	RF Bit 4 (UART) Interrupt Trigger Event	I/O Status
×	0	0	UART interrupt disable	PD2→IO PD3→IO
0	0	1	UART read buffer full	PD2→UART receiver pin PD3→IO
1	0	1	UART read buffer full or Receiver Data Error	PD2→UART receiver pin PD3→IO
×	1	0	UART transmitter buffer empty	PD2→IO PD3→UART transmitter pin
0	1	1	UART read buffer full or UART transmitter buffer empty	PD2→UART receiver pin PD3→UART transmitter pin
1	1	1	UART read buffer full or UART transmitter buffer empty or Receiver Data Error	PD2→UART receiver pin PD3→UART transmitter pin

Bit 4~Bit 3 (URM1~URM0) : UART Mode Select

URM1	URM0	Mode Status
0	0	7 bit data
0	1	8 bit data
1	0	9 bit data
1	1	×

Bit 7~Bit 5 (TRS2~TRS0) : Baud Rate Select

TRS2	TRS1	TRS0	Baud Rate
0	0	0	600 baud
0	0	1	1200 baud
0	1	0	2400 baud
0	1	1	9600 baud
1	0	0	19200 baud
1	0	1	38400 baud
1	1	0	57600 baud
1	1	1	115200 baud

Note: 600 and 1200 baud rates can be run in green mode

7.2.10 Page 3 UART Control Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	EVEN	PRE	PRERR	OVERR	FMERR	UTBE	URBF
×	R/W-X	R/W-0	R/W-0	R/W-0	R/W-0	R	R

Bit 0 (URBF) : UART read buffer full flag . Set to 1 when one character is received.

Reset to 0 automatically when read from UART data buffer.

Bit 1 (UTBE) : UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when writing into the UART data buffer.

Bit 2 (FMERR) : Receiver error flag . Set to 1 when frame error occurs. Clear this bit to 0 by software.

Bit 3 (OVERR) : Receiver error flag . Set to 1 when over running error occurs. Clear this bit to 0 by software.

Bit 4 (PRERR) : Receiver error flag . Set to 1 when parity error occurs. Clear this bit to 0 by software.

Bit 5 (PRE) : Enable parity addition

1 → Enable

0 → Disable

Bit 6(EVEN) : EVEN/ODD parity check select

1 → Even parity

0 → Odd parity

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the mark state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or more “0” are detected during 3 samples, it is recognized as normal start bit and the receiving operation is started.

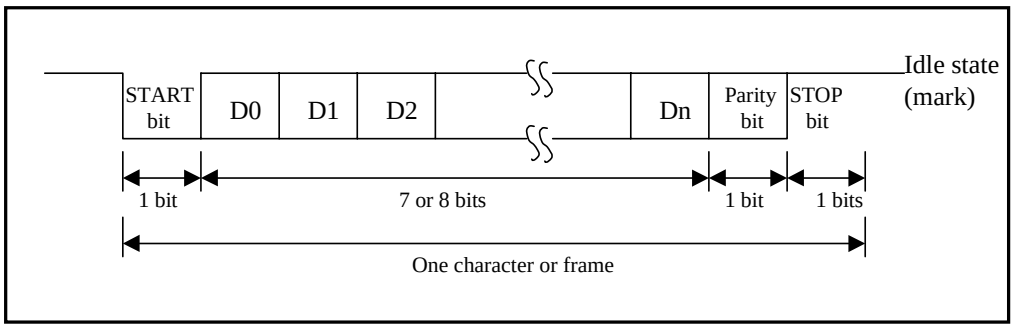


Fig. 8 UART Data Frame

There are three modes in UART. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. The Figure below shows the data format in each mode.

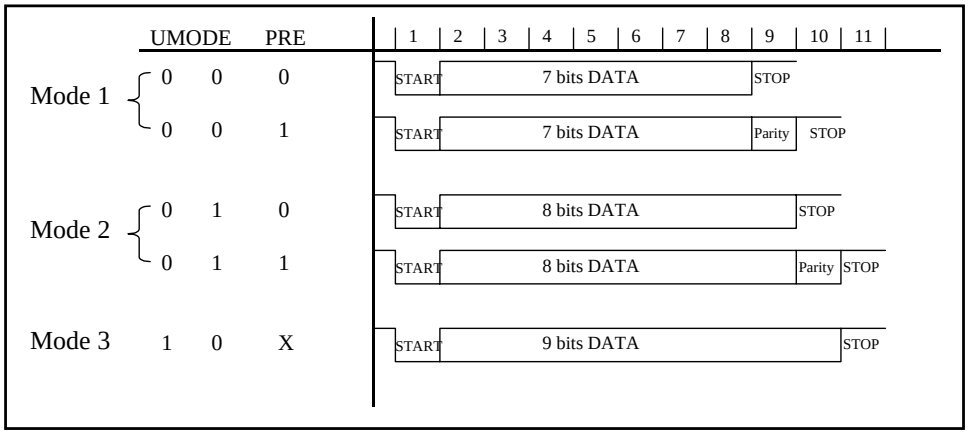


Fig. 9 UART Mode

In transmitting serial data, the UART operates as follows.

1. Set **TXE** bit of the UARTCON register to enable the UART transmission function.
2. Write data into the UART data buffer. Then start transmitting.
3. Serial transmit data are transmitted in the following order from UT (Port C7) pin.
   (a) Start bit: output one “0” bit
   (b) Transmit data: 7, 8 or 9 bits data are output from LSB to MSB
   (c) Parity bit: output one parity bit (odd or even selectable)
   (d) Stop bit: output one “1” bit (stop bit)
   (e) Mark state: output “1” continues until the start bit of the next transmit data
4. After transmitting the stop bit, the UART generates a UART interrupt (if enabled)
5. UTBE bit will be set to 1

In receiving, the UART operates as follows:

1. Set the **RXE** bit of the UARTCON register to enable the UART receiving function.

   The UART monitors the UR (Port C6) pin and synchronizes internally when it detects a start bit.

2. Receive data is shifted into the UARTRx register in the order from LSB to MSB.

3. The parity bit and the stop bit are received.

   After one character is received, the UART generates a **UART** interrupt (if enabled). **URBF** bit will be set to 1.

4. The UART makes the following checks:

   (a) Parity check: The number of 1 in receive data must match the even or odd parity setting of the **EVEN** bit in the UARTSTA register.

   (b) Frame check: The start bit must be 0 and the stop bit must be 1.

   (c) Overrun check: **URBF** bit of UARTCON register must be cleared (which means that the UARTRx register should be read out) before the next received data is loaded into the UARTRx register.

   If any checks failed, a UART interrupt will be generated (if enabled). The error flag should be cleared by software else a UART interrupt will occur when the next byte is received.

5. Read received data from the UART register. **URBF** bit will be cleared by hardware.

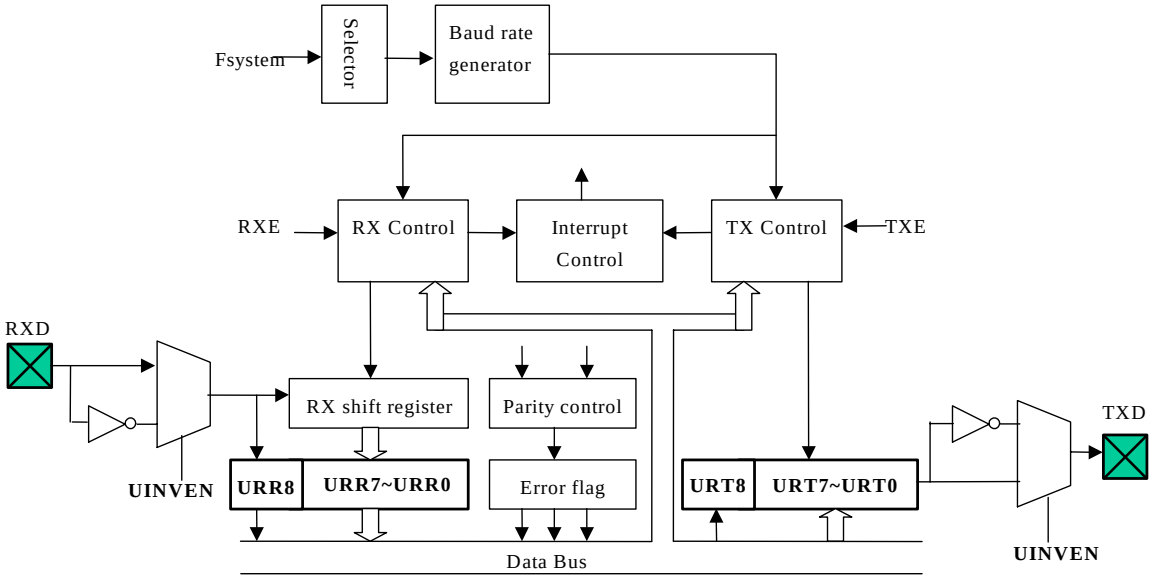


Fig. 10 UART Function Block

Bit 7 : Unused

7.2.11 R5 Program Page Selection, CNT CLK & Scale Setting, CNT1 Data (L)

7.2.11.1 Page 0 Program Page

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PS6	PS5	PS4	PS3	PS2	PS1	PS0
×	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 6 (PS0 ~ PS6) : Program page selection bits

PS6	PS5	PS4	PS3	PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	0	0	0	0	Page 0
0	0	0	0	0	0	1	Page 1
0	0	0	0	0	1	0	Page 2
0	0	0	0	0	1	1	Page 3
		:	:	:	:	:	:
		:	:	:	:	:	:
1	1	1	1	1	1	0	Page 126
1	1	1	1	1	1	1	Page 127

User can use the Page instruction to change page and maintain user's program page.

Bit 7 : This bit is undefined, not for use.

7.2.11.2 Page 1 Counter 1 Counter 2 CLK and Scale Setting

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	C2P2	C2P1	C2P0	CNT1S	C1P2	C1P1	C1P0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 2(C1P0~C1P2) : Counter 1 scaling

C1P2	C1P1	C1P0	Counter 1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S) : Counter 1 clock source

0/1 → 16.384kHz/instruction clock

Bit 4~Bit 6 (C2P0~C2P2) : Counter 2 scaling. Prescaler is different for Bit 0~Bit 2.

C2P2	C2P1	C2P0	Counter 2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7 (CNT2S) : Counter 2 clock source

0/1 → 16.384kHz / instruction clock

7.2.11.3 Page 2 Counter 1 Low 8-bit Data Buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 (CN10~CN17) : Counter 1 data buffer

Counter 1 is a 16 bits up-counter with 8-bit prescaler and user can read or write into the counter through R5 Page 2 and R6 Page 2. After an interrupt, it will reload the preset value.

Example: write: MOV 0x05,A ; write the accumulator data to Counter 1 (preset)

Example: read: MOV A,0x05 ; read R5 data and write into the accumulator

Example: write: MOV 0x06,A ; write the accumulator data (high 8 bits) to Counter 1

Example: read: MOV A,0x06 ; read R6 data (high 8 bits) and write into the accumulator

7.2.11.4 Page 3 DA Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	CDAS	CDAL2	CDAL1	CDAL0
–	–	–	–	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (CDAL0 ~ CDAL2) : Change output level of the current DA

CDAL2	CDAL1	CDAL0	Output Level
0	0	0	L0 (ratio = 1/8)
0	0	1	L1 (ratio = 2/8)
0	1	0	L2 (ratio = 3/8)
0	1	1	L3 (ratio = 4/8)
1	0	0	L4 (ratio = 5/8)
1	0	1	L5 (ratio = 6/8)
1	1	0	L6 (ratio = 7/8)
1	1	1	L7 (ratio =1)

Bit 3 (CDAS) : Current DA switch

0 → normal Port D7

1 → Current DA output

Bit 4 ~ Bit 7 : Undefined Register. These bits are undefined and not for use.

7.2.12 R6 Port 6 I/O Data, Data ROM Data Buffer, CNT1 Data (H), DA Control

7.2.12.1 Page 0 Port 6 I/O Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P60 ~ P67) : 8-bit Port 6 (0~7) I/O data register

User can use IOC register to define whether each bit is input or output.

7.2.12.2 Page 1 Data ROM Data Buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DRD7	DRD6	DRD5	DRD4	DRD3	DRD2	DRD1	DRD0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (DRD0 ~ DRD7) : Data ROM data buffer for ROM reading.

Example.

```
MOV   A,@1

MOV   R7_PAGE1,A

MOV   A,@0

MOV   R8_PAGE1,A

MOV   A,@0

MOV   R9_PAGE1,A

MOV   A,R6_PAGE1    ;read the data at the Data ROM, of which
                    ;address is "00001".
```

7.2.12.3 Page 2 Counter 1 High 8-bit Data Buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN1F	CN1E	CN1D	CN1C	CN1B	CN1A	CN19	CN18
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 (CN18~CN1F) : Counter 1 high 8 bits data buffer. Refer to R5 Page 2 Counter 1 low 8-bit data buffer for details.

7.2.12.4 Page 3 DA Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (DA2 ~ DA9) : Current DA most significant 8 bits of Current DA output buffer

Combine these 8 bits and R9 Page 3 Bit 4~Bit 5, 2 bits as complete 10 bits Current DA output data. Control register Bit 3 is Current DA power control.

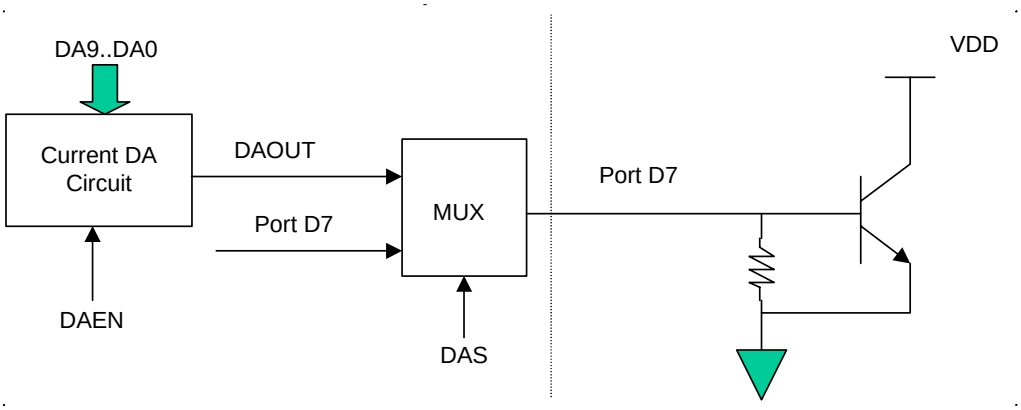


Fig 11 s Current DA structure

7.2.13 R7 Port 7 I/O Data, Data ROM Address, CNT2 Data, SPI Control

7.2.13.1 Page 0 Port 7 I/O Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit Port 7(0~7) I/O data register

User can use the IOC register to define whether each bit is input or output.

7.2.13.2 Page 1 Data ROM Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DRA7	DRA6	DRA5	DRA4	DRA3	DRA2	DRA1	DRA0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (DRA0 ~ DRA7) : Data ROM address (0~7) for ROM reading

7.2.13.3 Page 2 Counter 2 Data Buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(CN20~CN27) : Counter 2's data buffer

User can read and write into this buffer. Counter 2 is an 8-bit up-counter with 8-bit prescaler that user can use R7 page2 to preset and read the counter (write = preset). After an interrupt, it will reload the preset value.

Example: write: MOV 0x07 , A ; write the data at accumulator to counter1 (preset)

Example: read: MOV A , 0x07 ; read R7 data and write to accumulator

7.2.13.4 Page 3 SPI Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Fig.12 shows how SPI to communicate with other device by SPI module. If SPI is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted basing on the clock rate and the selected edge.

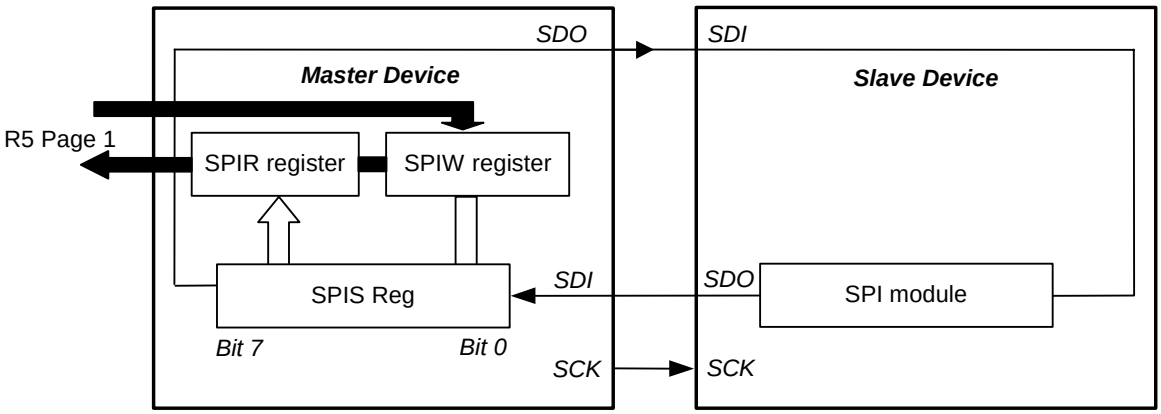


Fig 12: Single SPI Master / Salve Communication

Bit 0 ~ Bit 2 (SBR0 ~ SBR2) : SPI baud rate selection bits

SBR2	SBR1	SBR0	Mode	Baud Rate
0	0	0	Master	Fsco
0	0	1	Master	Fsco/2
0	1	0	Master	Fsco/4
0	1	1	Master	Fsco/8
1	0	0	Master	Fsco/16
1	0	1	Master	Fsco/32
1	1	0	Slave	
1	1	1	×	

Note: Fsco = CPU Instruction Clock

Example:

If PLL enable and RA Page 0 (Bit 5, Bit 4) = (1, 1), instruction clock is 3.58 MHz/2 → Fsco=3.5862MHz/2

If PLL enable and RA Page 0 (Bit 5, Bit 4) = (0, 0), instruction clock is 0.895 MHz/2 → Fsco=0.895 MHz/2

If PLL disable, instruction clock is 32.768kHz/2 → Fsco=32.768kHz/2.

Bit 3 (SCES) : SPI clock edge selection bit

0 → Data shifts out on a rising edge, and shifts in on falling edge. Data is hold during the low level.

1 → Data shifts out on falling edge, and shifts in on rising edge. Data is hold during the high level.

Bit 4 (SE) : SPI shift enable bit

0 → Reset as soon as the shifting is complete, and the next byte is ready to shift.

1 → Start to shift, and remain a 1 while the current byte is still being transmitted.

NOTE
This bit has to be reset by software.

Bit 5 (SRO) : SPI read overflow bit

0 → No overflow

1 → A new data is received while the previous data is still being hold in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users have to read the SPIB register even if only the transmission is implemented. Note that this can only occur in slave mode.

Bit 6 (SPIE) : SPI enable bit

0 → Disable SPI mode

1 → Enable SPI mode

Bit 7 (RBF) : SPI read buffer full flag

0 → Receive is not finished yet, SPIB is empty.

1 → Receive is finished, SPIB is full.

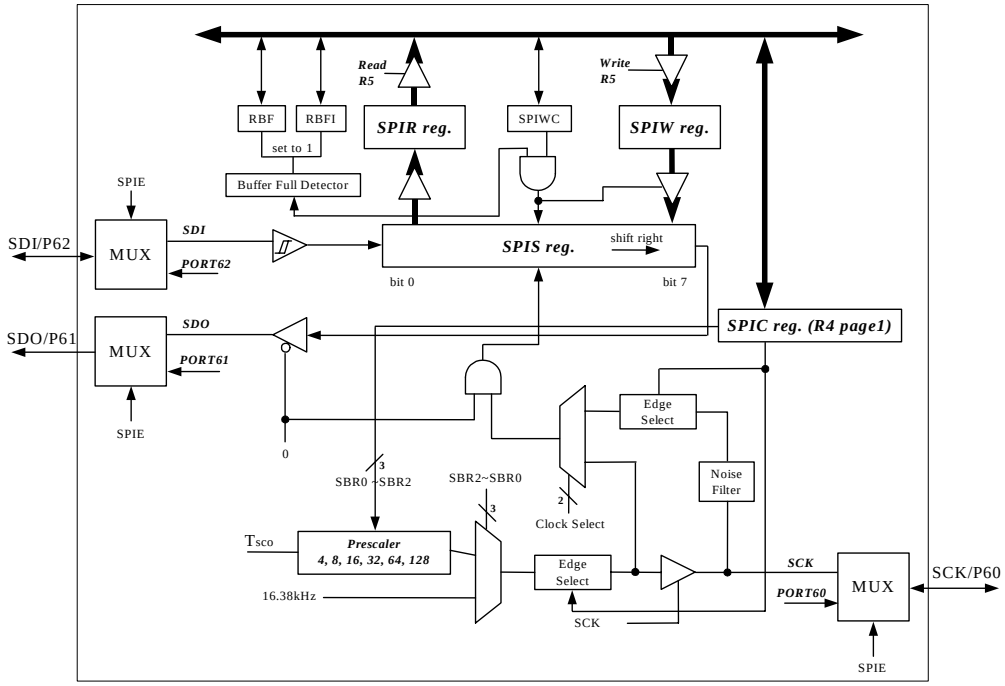


Fig. 13 SPI Structure

SPIC reg : SPI control register

SDO/P61 : Serial data out

SDI/P62 : Serial data in

SCK/P60 : Serial clock

RBF : Set by buffer full detector, and reset by software.

RBFI : Interrupt flag. Set by buffer full detector, and reset in software.

Buffer Full Detect : Set to 1, while an 8-bit shifting is complete.

SE : Loads the data in SPIW register, and begins to shift

SPIE : SPI control register

SPIS reg. :Shifting byte out and in. The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data is being written to, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the RBFI (Read Buffer Full Interrupt) flag are set.

SPIR reg. : Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register is read.

SPIW reg. : Write buffer. The buffer will deny any write until the 8-bit shifting is completed. The SE bit will be kept in 1 if the communication is still undergoing. This flag must be cleared as the shifting is finished. Users can determine if the next write attempt is available.

SBR2 ~ SBR0: Programs the clock frequency/rates and sources.

Clock Select : Selects either the internal instruction clock or the external 16.338kHz clock as the shifting clock.

Edge Select : Selects the appropriate clock edges by programming the SCES bit

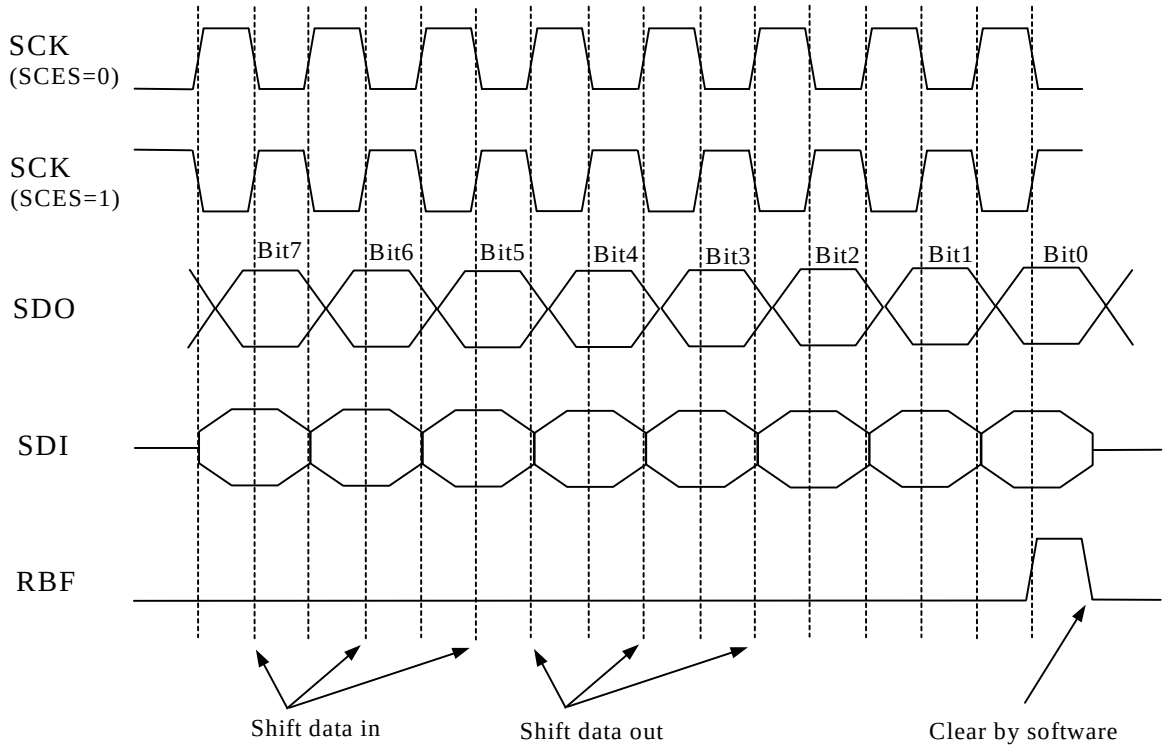


Fig. 14 SPI Timing

7.2.14 R8 Port 8 I/O Data, Data ROM Address, DTMF Receiver, SPI Data

7.2.14.1 Page 0 Port 8 I/O Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P80 ~ P87) : 8-bit Port 8 (0~7) I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.14.2 Page 1 Data ROM address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DRA15	DRA14	DRA13	DRA12	DRA11	DRA10	DRA9	DRA8
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (DRA8 ~ DRA15) : Data ROM address (8~15) for ROM reading

7.2.14.3 Page 2 DTMF Receiver

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPFLAG	STD	–	–	Q4	Q2	Q1	Q0
R	R/W-0	×	×	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (Q1 ~ Q4) : DTMF receiver decoding data

These provide the code corresponding to the last valid tone-pair received (see code table). The STD signal with steering output presents a logic high when a received tone-pair has been registered and the Q4 ~ Q1 output latch updated, and generates an interrupt (IOCF has enabled); returns to logic low when the voltage on ST/GT falls below Vtst.

F low	F high	Key	DREN	Q4~Q1
697	1209	1	1	0001
697	1336	2	1	0010
697	1477	3	1	0011
770	1209	4	1	0100
770	1336	5	1	0101
770	1477	6	1	0110
852	1209	7	1	0111
852	1336	8	1	1000
852	1477	9	1	1001
941	1209	0	1	1010
941	1336	*	1	1011
941	1477	#	1	1100
697	1633	A	1	1101
770	1633	B	1	1110
852	1633	C	1	1111
941	1633	D	1	0000
Any	Any	Any	0	××××

Note: "×" means unknown

Bit 4~Bit 5 : Undefined Register

Bit 6 (STD) : Delayed steering output

Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below Vtst.

0/1 → Data invalid/data valid

Be sure to open the main clock before using the DTMF receiver circuit. A logic "0, 0" applied to R5 Page 3 B 4 and B 3 will shut down power of the device to minimize the power consumption in standby mode. It stops functions of the filters.

In many situations not requiring independent selection of received and paused, the simple steering circuit is applicable. Component values are chosen according to the following formula:

t REC = t DP + t GTP t ID = t DA + t GTA

The value of t DP is a parameter of the device and t REC is the minimum signal duration to be recognized by the receiver. A 0.1 µF value for C is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t REC of 30mS would be 300k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t GTP) and tone-absent (t GTA). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter digital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t REC improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. On the other hand, a relatively short t REC with a long t DO would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be required.

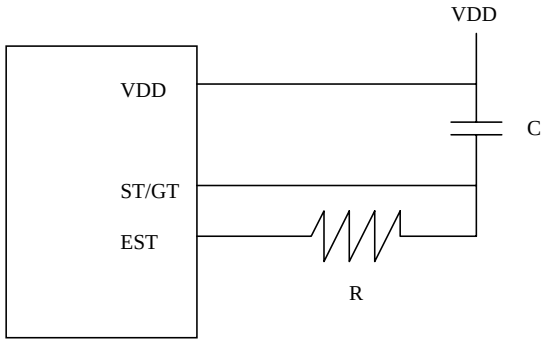


Fig. 15 DTMF Receiver Delay Time Control

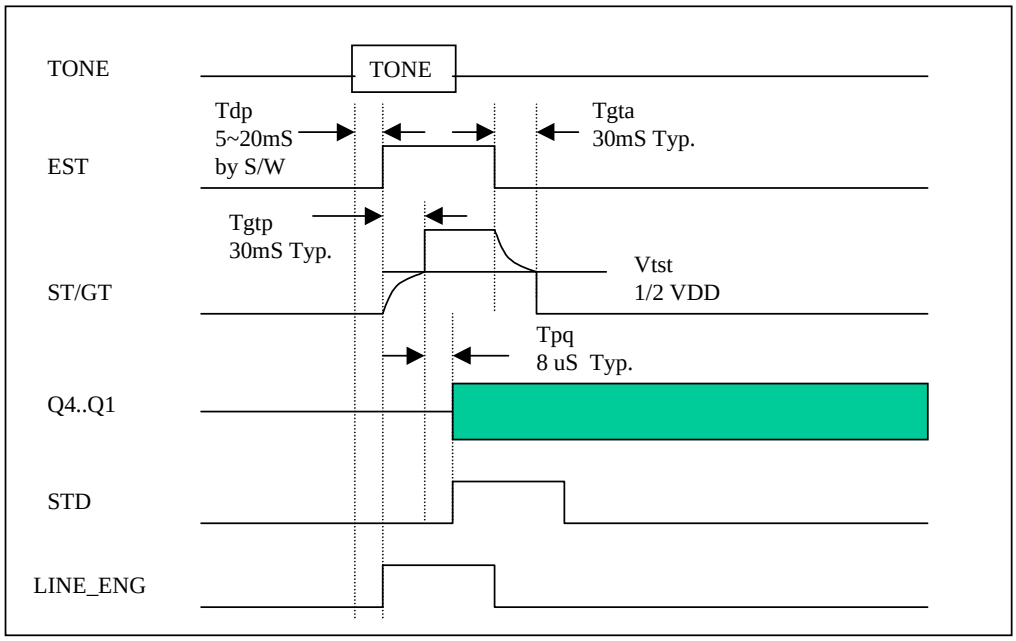


Fig. 16 DTMF Receiver Timing

Bit 7 (CMPFLAG) : Comparator output flag

0 → Input voltage < reference voltage

1 → Input voltage > reference voltage

NOTE
Refer to Sec. 7.2.16.3 RA Page 2 Comparator Control Register.

7.2.14.4 Page 3 SPI Data Buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer

If you write data to this register, the data will be written to the SPIW register. If you read this data, it will read the data from the SPIR register. Refer to Fig. 9.

7.2.15 R9 Port 9 I/O Data, Data ROM Address, Keytone Control

7.2.15.1 Page 0 Port 9 I/O Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit Port 9 (0~7) I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.15.2 Page 1 Data ROM Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	DRA20	DRA19	DRA18	DRA17	DRA16
-	-	-	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 4 (DRA16 ~ DRA20) : Data ROM address (16~20) for ROM reading..

Bit 5~Bit 7 : Unused

7.2.15.3 Page 2 FSK/CW/DTMF Power Select

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCTRL1	PCTRL0	ADCS3	ADCS2	ADCS1	-	-	-
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	-	-	-

Bit 0 ~ Bit 1 : Unused

Bit 3 ~ Bit 5(ADCS1 ~ ADCS3) : PORT65 ~ Port 67 normal IO / CMP input control bit.

ADCSX = 1 → Comparator input

ADCSX = 0 → Normal IO

Bit 6~Bit 7 (PCTRL0~PCTRL1) : FSK and DTMF power control bits

PCTRL1	PCTRL0	Select	Relation Register
0	0	FSK and DTMFr power off	-
0	1	FSK power on	RA Page 0
1	0	DTMF receiver power on	R8 Page 2
1	1	***Cannot be used***	-

* Do not set both the bits to 1, or FSK and DTMF function will fail.

* When User turns on the DTMF receiver power, Port 60 and Port 61 will switch to /STGT and EST pin.

7.2.15.4 Page 3 Keytone Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URT8	URR8	DA1	DA0	URINV	KT1	KT0	KTS
R/W-X	R	R/W-X	R/W-X	R/W-X	R/W-0	R/W-0	R/W-0

Bit 0 (KTS) : Key tone output switch

0 → Normal Port 76

1 → Keytone output

Bit 1 ~ Bit 2 (KT0 ~ KT1) : Keytone output frequency and its power control

KT1	KT0	Keytone Frequency and Power
0	0	32.768kHz/32 = 1.024kHz clock and enable
0	1	32.768kHz/16 = 2.048kHz clock and enable
1	0	32.768kHz/8 = 4.096kHz clock and enable
1	1	Power-off keytone

Bit 3 (URINV) : Enable UART TXD, RXD port inverse output

0 → Disable UART TXD, RXD port inverse output

1 → Enable UART TXD, RXD port inverse output

Bit 4 ~ Bit 5 (DA0~DA1) : These two bits are the least significant bits of the Current DA. Combine R6 Page 3 and these 2 bits as complete 10 bits Current DA output data.

Bit 6 (URR8) : MSB of UART receiver data buffer.

Bit 7 (URT8) : MSB of UART transmitter data buffer.

7.2.16 RA CPU Power Saving, Main CLK Select, FSK, WDT Timer Comparator Control, Tone 1 Generator

7.2.16.1 Page 0 Power Saving, Main CLK Select, FSK, WDT Timer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PLLEN	CLK1	CLK0	**ROMRI**	FSKDATA	/CD	WDTEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R	R	R/W-0

Bit 0 (WDTEN) : Watchdog control register

User can use WDTC instruction to clear the watchdog counter. The counter's clock source is 32768/2 Hz. If the prescaler is assigned to TCC, the Watchdog will time out by (1/32768)*2 * 256 = 15.616ms. If the prescaler is assigned to WDT, the time out will be more times depending on the prescaler ratio.

0/1 → disable/enable

Bit 1 (/CD) : FSK carrier detect indication

0/1 → Carrier Valid/Carrier Invalid

It is a read only signal. If the FSK decoder detects the energy of the marked or space signal, the Carrier signal will go to low level. Otherwise it will go to high. Note that this should be in normal mode.

Bit 2 (FSKDATA) : FSK decoding data output

It is a read only signal. If the FSK decodes the mark or space signal, it will output a high level signal or low level signal at this register. It is a raw data type. That means the decoder just decodes the signal and has no process on the FSK signal. Note that this should be in normal mode.

User can use FSK data falling edge interrupt function to help in data decoding.

Example:

```
MOV     A,@01000000
IOW     IOCF            ;enable FSK interrupt function
CLR     RF
ENI                     ;wait for FSK data's falling edge
:
```

0 = Space data (2200 Hz)

1 = Mark data (1200 Hz)

FSK block power is controlled by R5 Page 3 Bit 3, 4. When PCTRI1=0 and PCTRL0=1, FSK power is turned on.

The relation between R5 Bit 3 to Bit 4 and RA Bit 1 to Bit 2 are shown in Fig.17. You have to power up the FSK decoder first, then wait for a setup time (Tsup) and check carrier signal (/CD). If the carrier is low, the program can process the FSK data.

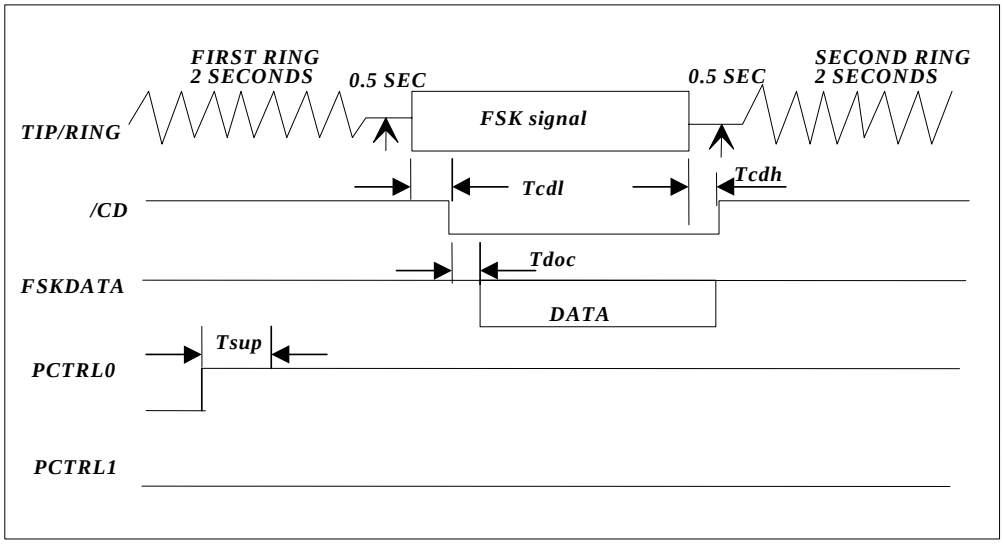


Fig. 17 Relationship between R5 Bit 3 to Bit 4 and RA Bit 1 to Bit 2

The controller is a CMOS device designed to support the Caller Number Deliver feature which is offered by the Regional Bell Operating Companies. The FSK block comprises one path: the signal path. The signal path consist of an input differential buffer, a band pass filter, an FSK demodulator and a data valid with carrier detect circuit.

In a typical application, user can use his own external ring detect output as a triggering input to IO port. User can use this signal to wake up the chip by external ring detect signal. Setting “0, 1” to R5 B4 and B3 (PCTRL1 & PCTRL0) of the RA register activates the FSK decoder block. If B4 and B3 of register R5 is set to “0, 1”, the FSK decoder block will be powered down.

The input buffer accepts a differential AC coupled input signal through the TIP and RING input and feeds this signal to a band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post filter. The output data is then made available at Bit 2 (FSKData) of register RA. This data, as sent by the central office, includes the header information (alternate "1" and "0") and 150 ms of marking which precedes the date, time and calling number. If no data is present, the Bit 2 (Data) of register RA is held at “1” state. This is accomplished by a carrier detect circuit which determines if the in-band energy is high enough. If the incoming signal is valid, Bit 1 (/CD) of register RA will be “0” otherwise it will be held at “1”. Thus the demodulated data is transferred to Bit 2 (Data) of register RA. If it is not, then the FSK demodulator is blocked.

Bit 3 (ROMRI) : External Data ROM read data address auto_increase enable.

RO_IDEN	ROMRI	Result
0	×	Regardless Read/Write external Data ROM, Address flag cannot increase or decrease.
1	0	Address flag will auto_increase or decrease after a Read/Write of the external Data ROM.
1	1	Address flag will auto_increase or decrease after a Write to the external Data ROM, but the address flag is constant after reading the external Data ROM.

Bit 4 ~ Bit 5 (CLK0 ~ CLK1) : Main clock selection bits

User can choose different frequency for the main clock by CLK1 and CLK2. All the clock selection is listed below.

PLLEN	CLK1	CLK0	Sub Clock	Main Clock	CPU Clock
1	0	0	**32.768kHz**	**5.374MHz**	**5.374MHz (Normal mode)**
1	0	1	32.768kHz	1.7913MHz	1.7913MHz (Normal mode)
1	1	0	32.768kHz	10.7479MHz	10.7479MHz (Normal mode)
1	1	1	32.768kHz	3.5826MHz	3.5826MHz (Normal mode)
0	Don’t care	don’t care	32.768kHz	Don’t care	32.768kHz (Green mode)
0	Don’t care	don’t care	32.768kHz	Don’t care	32.768kHz (Green mode)
0	Don’t care	don’t care	32.768kHz	Don’t care	32.768kHz (Green mode)
0	Don’t care	don’t care	32.768kHz	Don’t care	32.768kHz (Green mode)

Bit 6 (PLLEN) : PLL enable control bit

It is CPU mode control register. If PLL is enabled, the CPU will operate in normal mode (high frequency, main clock), otherwise it will run in green mode (low frequency, 32768 Hz).

0/1 → disable/enable

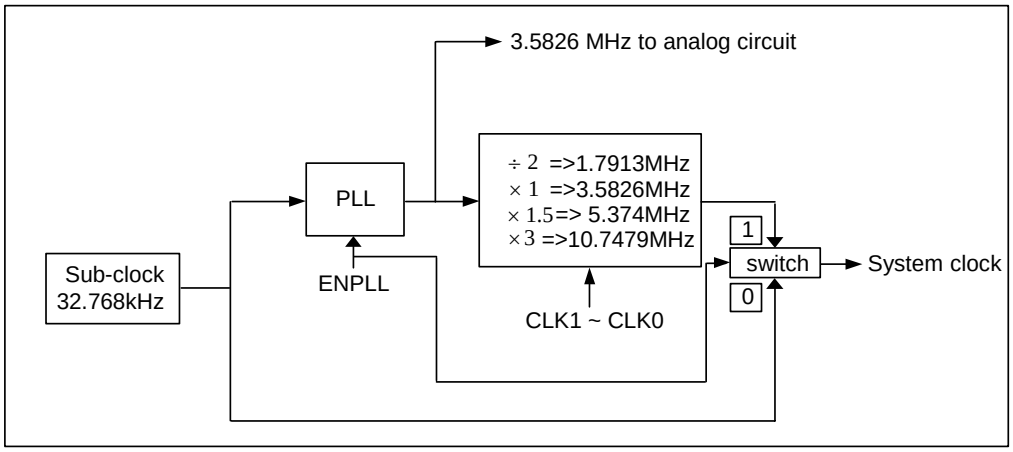


Fig. 18 Relationship between 32.768kHz and PLL

Bit 7: Unused Register. Always keep this bit to 0, otherwise some un-expected error will occur.

Wake-up Signal	Sleep Mode	Green Mode	Normal Mode
	RA (7, 6) = (0, 0) + SLEP	RA (7, 6) = (x, 0) no SLEP	RA (7, 6) = (x, 1) no SLEP
TCC time out IOCF Bit 0=1 And "ENI"	No function	Interrupt (jump to Address 8 at Page 0)	Interrupt (jump to Address 8 at Page 0)
Counter 1 time out IOCF Bit 1=1 And "ENI"	No function	Interrupt (jump to Address 8 at Page 0)	Interrupt (jump to Address 8 at Page 0)
Counter 2 time out IOCF Bit 2=1 And "ENI"	No function	Interrupt (jump to Address 8 at Page 0)	Interrupt (jump to address 8 at Page 0)
WDT time out	RESET and Jump to Address 0	RESET and Jump to Address 0	RESET and Jump to Address 0
Port 7 Any one bit in IOCE Page 0 = 1 And "ENI"	RESET and Jump to Address 0	Interrupt (jump to Address 8 at Page 0)	Interrupt (jump to Address 8 at Page 0)
DED interrupt IOCE page1 bit 6 = 1 And RF Bit 3 logic level variation (switch by EDGE bit) And “ENI”	No function	Interrupt (jump to Address 8 at Page 0)	Interrupt (jump to Address 8 at Page 0)

NOTE

- *Port 70 ~ Port 76's wake-up function is controlled by IOCE Page 0 Bit 0~Bit 6 and ENI instruction. They are falling edge trigger.*
- *Port 77's wake-up function is controlled by IOCE Page 0 Bit 7. It can be triggered by a falling edge or rising edge (controlled by CONT register).*

7.2.16.2 Page 1 Undefined Register: This register is not for use.

7.2.16.3 Page 2 Comparator Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPEN	CMPREF	CMPS1	CMPS0	CMPB3	CMPB2	CMPB1	CMPB0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

If user defines Port 63, Port 64 or Port 65 (by ADCS1, ADCS2, ADCS3 at R9 Page 2) as a comparator input or Port 6, then user can use this register to control the comparator's function.

Bit 0~Bit 3(CMPB0 ~ CMPB3) : Reference voltage selection of the internal bias circuit for the comparator.

Reference voltage for comparator = VDD x (N + 0.5) / 16, N = 0 to 15

Bit 4~Bit 5(CMPS0~CMPS1) : Channel selection from CMP1 to CMP3 for comparator

CMPS1	CMPS0	Input
0	0	CMP1
0	1	CMP2
1	0	CMP3
1	1	Reserved

Bit 6(CMPREF) : Switch for comparator reference voltage type

0 → internal reference voltage

1 → external reference voltage

Bit 7(CMPEN) : Enable control bit of comparator.

0/1 → disable/enable, when CMPEN bit is set to “0” , the 2.0V ref circuit will be powered off.

The relationship between these registers is shown in Fig.19.

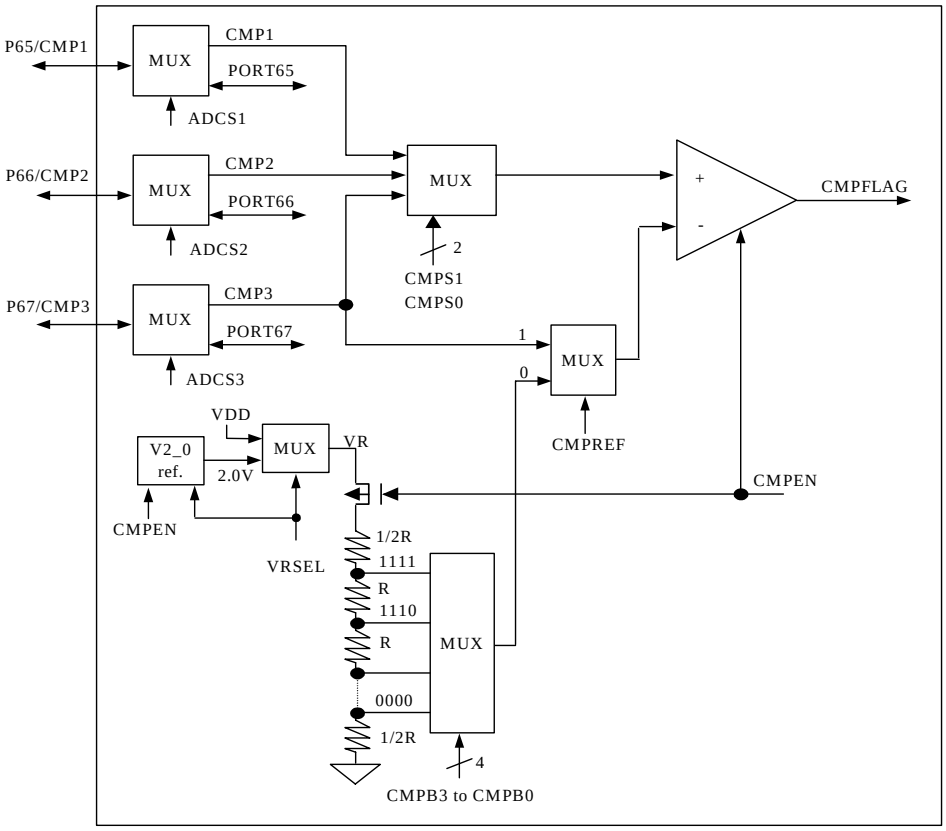


Fig. 19 Comparator Circuit

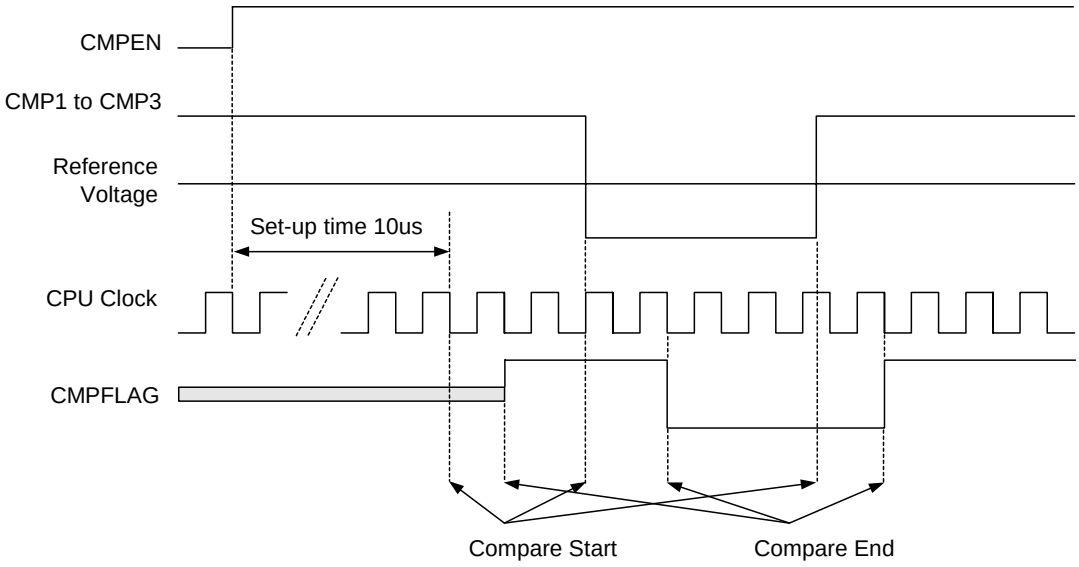


Fig. 20 Comparator Timing

7.2.16.4 Page 3 Tone 1 Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T17	T16	T15	T14	T13	T12	T11	T10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 (T10~T17) : Tone Generator 1 frequency divider and power control. Run in Normal mode.

Clock source = 85300Hz

T17~T10 = '11111111' → Tone Generator 1 will has 334 (85300/255) Hz Sine wave output.

:

T17~T10 = '00000010' → Tone Generator 1 will has 41150(85300/2) Hz Sine wave output.

T17~T10 = '00000001' → DC bias voltage output

T17~T10 = '00000000' → Power off

Built-in tone generator can generate dialing tone signals for dialing tone type telephones or just a single tone. In DTMF application, there are two kinds of tones, One is the row frequency group (Tone 1), the other is the column frequency group (Tone 2). Each group has four kinds of frequency, user can get a total of 16 kinds of DTMF frequency. A Tone generator contains a row frequency sine wave generator for generating the DTMF signal which is selected by RA Page 3 and a column frequency sine wave generator for generating the DTMF signal which is selected by RB Page 3. This block can generate a single tone by filling one of these two registers.

If all the values are low, the power of the tone generators will be turned off.

		Tone 2 (RB Page 3) High Group Freq.			
		1201.4Hz (0X47)	1332.8Hz (0X40)	1470.7Hz (0X3A)	1640.4Hz (0X34)
Tone 1 (RA page3)	699.2Hz (0x07A)	1	2	3	A
	768.5Hz (0x06F)	4	5	6	B
Low group freq.	853.0Hz (0x064)	7	8	9	C
	937.4Hz (0x05B)	*	0	#	D

Tone 1 and Tone 2 are asynchronous tone generators and both can be used to generate Caller ID FSK signal. In FSK generator application, Tone 1 or Tone 2 can generate 1200Hz Mark bit and 2200Hz Space bit for Bell202 or 1300Hz Mark bit and 2100Hz Space bit for V.23. See the following table.

Tone 1 (IOCC Page 1) or Tone 2 (IOCD Page 1)	Freq. (Hz)	Description
0×47	1201.4	Bell202 FSK Mark bit
0×27	2187.2	Bell202 FSK Space bit
0×42	1292.4	V.23 FSK Mark bit
0×29	2080.5	V.23 FSK Space bit

The Tone generator can also generate CW or SMS signal. See the following table.

Tone 1 (IOCC Page 1) or Tone 2 (IOCD Page 1)	Freq. (Hz)	Description
0×28	2132.5	CAS freq
0×1F	2751.6	CAS freq

7.2.17 RB Port B I/O Data, Key Strobe, Tone 2 Generator

7.2.17.1 Page 0 Port B I/O Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (PB0 ~ PB7) : 8-bit Port B (0~7) I/O data register.

User can use the IOC register to define each bit as either input or output.

7.2.17.2 Page 1 Undefined Register: This register is not for use.

7.2.17.3 Page 2 Key Strobe Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (STRB0 ~ STRB7) : Key strobe control bits.

These key strobe control registers correspond to Port 80 ~ Port 87. Refer to Keystobe explanation (RE Page 3).

7.2.17.4 Page 3 Tone 2 Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T27	T26	T25	T24	T23	T22	T21	T20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(T20~T27) : Tone Generator 1 frequency divider and power control. Refer to RA Page 3 Tone 1 control register for details.

7.2.18 RC Port C I/O Data, Data RAM Data Buffer, Tone 2 Generator

7.2.18.1 Page 0 Port C I/O Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (PC0 ~ PC7) : 8-bit Port C (0~7) I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.18.2 Page 1 Data RAM Data Buffer 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM1D7	RAM1D6	RAM1D5	RAM1D4	RAM1D3	RAM1D2	RAM1D1	RAM1D0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (RAM1D0 ~ RAM1D7) : Data RAM data Buffer 1 for RAM reading or writing.

Example.

```
MOV     A,@1
MOV     RD_PAGE1,A
MOV     A,@0
MOV     RE_PAGE1,A
MOV     A,@0x55
MOV  RC_PAGE1,A         ;write data 0x55 to DATA RAM
                        ;which is address "0001"
MOV     A,RC_PAGE1            ;read data
:
```

7.2.18.3 Page 2 Key Strobe Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB15	STRB14	STRB13	STRB12	STRB11	STRB10	STRB9	STRB8
R	R	R	R	R	R	R	R

Bit 0 ~ Bit 7 (STRB8 ~ STRB15) : Key strobe control bits

These key strobe control registers correspond to Port 90 ~ Port 97. Refer to Key stobe explanation (RE Page 3).

7.2.18.4 Page 3 Undefined Register:

This register is unimplemented, not for use.

7.2.19 RD Port D I/O Data, Data RAM Address

7.2.19.1 Page 0 Port D I/O Data, Data RAM Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (PD0 ~ PD7) : 7-bit Port D (0~6) I/O data register

User can use the IOC register to define each bit either as input or output.

7.2.19.2 Page 1 Data RAM Address 1 (Low 8 bits)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM1A7	RAM1A6	RAM1A5	RAM1A4	RAM1A3	RAM1A2	RAM1A1	RAM1A0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 7 (RAM1A0 ~ RAM1A7) : Data RAM address1 (Address 0 to Address 7) for RAM reading or writing

7.2.19.3 Page 2 Undefined Register

7.2.19.4 Page 3 Undefined Register

These two register are unimplemented, not for use.

7.2.20 RE Interrupt Flag 1, Data RAM Address 1 (H) CAS, Key Scan

7.2.20.1 Page 0 Interrupt Flag 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Interrupt flag registers. User can only clear these bits from 1 to 0 but cannot set them from 0 to 1.

Bit 0 (INT0) : External INT0 pin interrupt flag

If Port 70 has a falling edge trigger signal, the CPU will set this bit.

Bit 1 (INT1) : External INT1 pin interrupt flag

If Port 71 has a falling edge trigger signal, the CPU will set this bit.

Bit 2 (INT2) : External INT2 pin interrupt flag

If Port 72 has a falling edge trigger signal, the CPU will set this bit.

Bit 3 (INT3) : External INT3 pin interrupt flag

If Port 73 has a falling edge trigger signal, the CPU will set this bit.

Bit 4 (INT4) : External INT4 pin interrupt flag

If Port 74 has a falling edge trigger signal, the CPU will set this bit.

Bit 5 (INT5) : External INT5 pin interrupt flag

If Port 75 has a falling edge trigger signal, the CPU will set this bit.

Bit 6 (INT6) : External INT6 pin interrupt flag

If Port 76 has a falling edge trigger signal, the CPU will set this bit.

Bit 7 (INT7) : External INT7 pin interrupt flag

If Port 77 has a falling (or rising and falling) edge trigger signal, the CPU will set this bit.

Signal	Trigger	Remark
INT0 : INT6	Falling edge	
INT7	Falling/Falling & Rising Edge	Controlled by CONT register

7.2.20.2 Page 1 Data RAM Address 1(H)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	RAM1A11	RAM1A10	RAM1A9	RAM1A8
×	×	×	×	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 3 (RAM1A8 ~ RAM1A11) : Data RAM address (Address 8 to Address 11) for RAM reading.

Bit 4~Bit 7 Undefined Register. These registers are not certain whether 0 or 1. Do not use these registers.

7.2.20.3 Page 2 CAS Detected Flag, Keyscan

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CAS	–	Key strobe	Keyscan	LCD1	LCD0	–	–
R	×	R/W-0	R/W-0	R/W-0	R/W-0	×	×

Bit 0~Bit 1 : Undefined register. These bits are unimplemented, not for use.

Bit 2~Bit 3 (LCD0~LCD1) : These two bits are used to enable/disable key scan and the LCD controller.

LCD1	LCD0	Sates
0	0	Keyscan disable (ignore Keyscan bit) External LCD controller disable
0	1	Keyscan disable (ignore Keyscan bit) External LCD controller disable
1	0	Keyscan disable (ignore Keyscan bit) External LCD controller disable
1	1	Keyscan enable (Keyscan bit must = 1) External LCD controller enable

Bit 4 (Keyscan) : Key scan function enable control bit.

0/1 → disable/enable

If Keyscan function is enabled (LCD0, LCD1 and Keyscan =1), Port 8 and Port 9 will be pulled high automatically and become key strobe pins.

The key scan waveform is as follows.

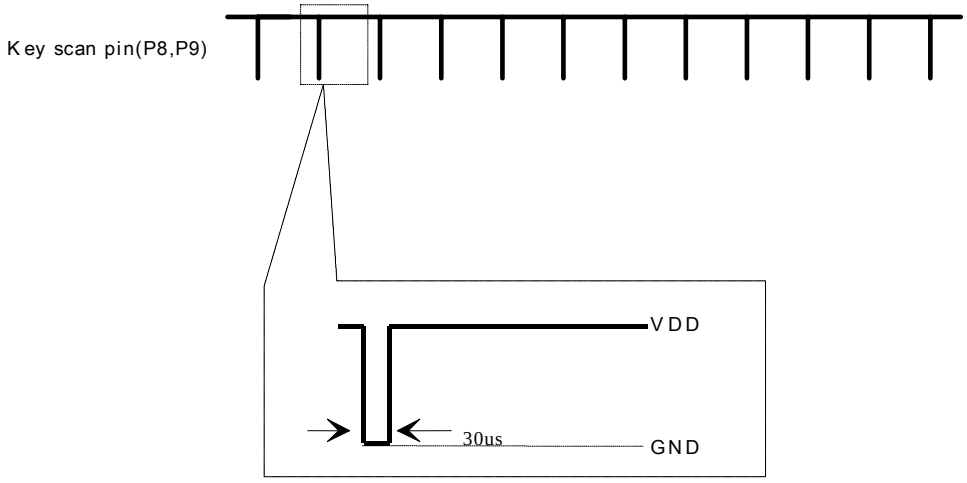


Fig.21 Keyscan Waveform

Bit 5 (KEYSTRB) : Key strobe enable control bit

0/1 → disable/enable

Key strobe signal , if you set this bit , the segment will switch to strobe signal temporally and output a zero signal (one instruction long) one by one from Port 80 to Port 87 and Port 90 to Port 97. During one strobe time, the CPU will check whether Port 7 (0:3) is equal to "1111" or not. If not, the CPU will latch a zero at RB Page 1 and RC Page 1 one by one depending on which segment strobe. After strobe, this bit will be cleared. Fig. 22 is a key strobe signal.

One instruction

	REGISTER															
STROBE	RB(0)	RB(1)	RB(2)	RB(3)	RB(4)	RB(5)	RB(6)	RB(7)	RC(0)	RC(1)	RC(2)	RC(3)	RC(4)	RC(5)	RC(6)	RC(7)
PORT80	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PORT81	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PORT82	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
PORT83	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
PORT84	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
PORT85	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
PORT86	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
PORT87	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
PORT90	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
PORT91	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
PORT92	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
PORT93	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
PORT94	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
PORT95	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
PORT96	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
PORT97	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Fig.22 Key strobe Signal

Bit 6 Unused

The following figure shows the relationship between Keyscan, and Key strobe. Fig.24 is a Keyscan flow by interrupt trigger.

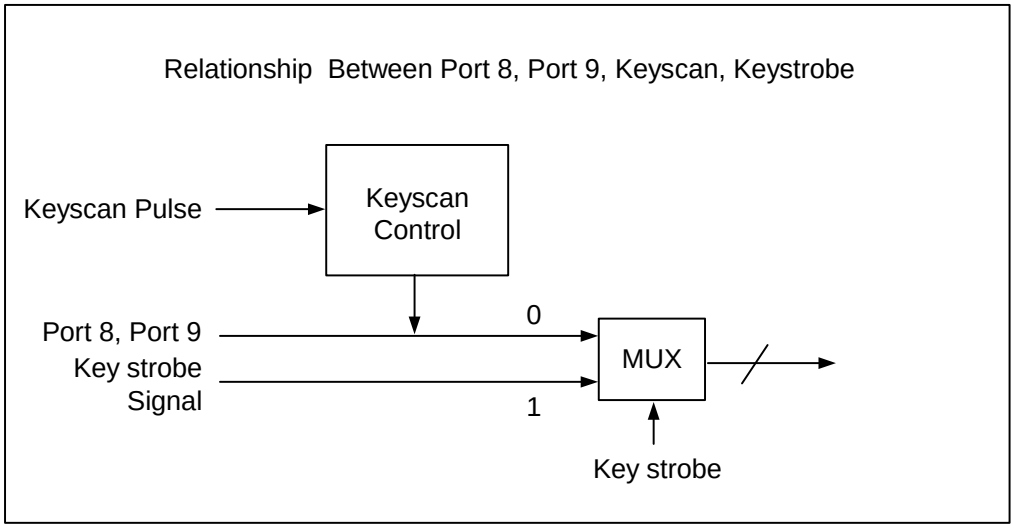


Fig. 23 Keyscan, Key strobe and Segments

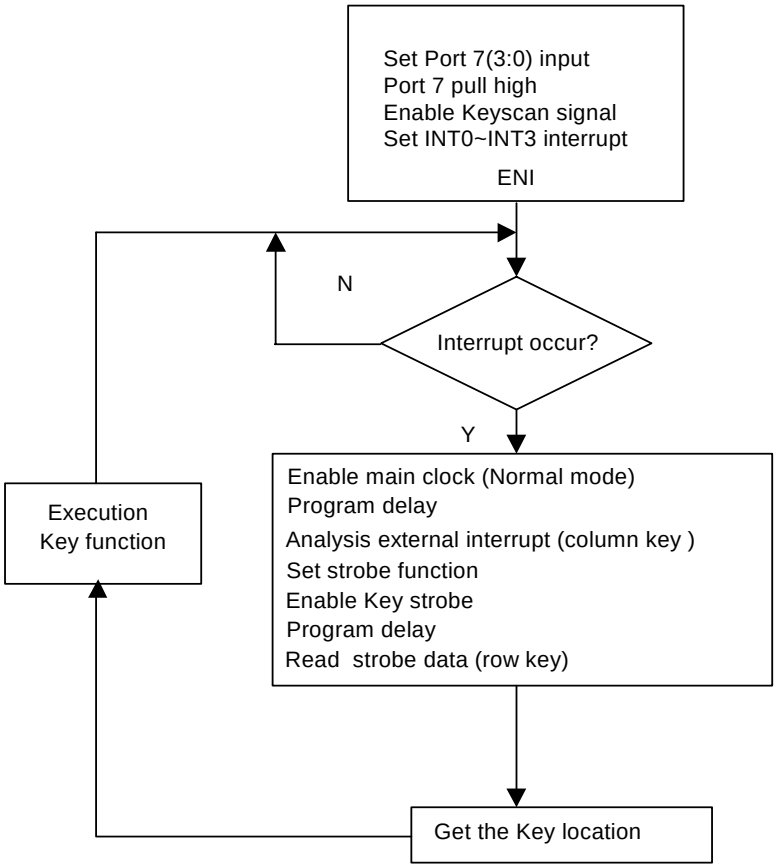


Fig. 24 Key Scan Flow By Interrupt Trigger

Bit 7 (CAS) : Call Waiting decoding output

0/1 → CW data valid / No data

7.2.20.4 Page 3 UART transmitter data buffer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URT7	URT6	URT5	URT4	URT3	URT2	URT1	URT0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 7(URT0~URT7) : Low 8-bit UART transmitter data buffer

7.2.21 RF Interrupt flag

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF/STD	FSK/CW	–	UART	DED	CNT2	CNT1	TCC
R/W-0	R/W-0	×	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Note: "1" means interrupt request

"0" means non-interrupt

Bit 0 (TCC) : TCC timer overflow interrupt flag

Set when TCC timer overflows.

Bit 1 (CNT1) : Counter 1 timer overflow interrupt flag

Set when Counter 1 timer overflows.

Bit 2 (CNT2) : Counter 2 timer overflow interrupt flag

Set when Counter 2 timer overflows.

Bit 3 (DED) : Differential Energy Detector (DED) Interrupt flag output data. If DEDD (RE Page 2 Bit 7) has a falling edge signal (or falling & rising edge signal, switch by IOCE Page 1 Bit 5), the CPU will set this bit.

Bit 4 (UART) : Universal Asynchronous Receiver Transmitter interrupt flag. When the transmitter buffer is empty, receiver buffer full or receiver data error, this bit will be set.

Bit 5: Undefined register. These bits are unimplemented, not for use.

Bit 6 (FSK/CW) : FSK data or Call waiting data interrupt flag.

If FSKDATA or CAS has a falling edge trigger signal, the CPU will set this bit.

Bit 7 (RBF/STD) : SPI data transfer complete or DTMF receiver signal valid interrupt

If serial IO's RBF signal has a rising edge signal (RBF set to "1" when data is transferred completely), the CPU will set this bit. Or when the DTMF receiver's STD signal has a rising edge signal (the DTMF decodes a DTMF signal).

IOCF is the interrupt mask register. User can read and clear.

Trigger edge is shown in the following table:

Signal	Trigger	Remark
TCC	Time out	
Counter 1	Time out	8/16 bits select by CONT register
Counter 2	Time out	
DED	Signal detect	
UART	Receiver full, Transmitter empty or error (if enabled)	
FSK	Falling edge	
RBF/STD	Rising edge	

EM78815 MCU will store ACC, R3 status and R5 Page automatically after an interrupt is triggered. It will be restored after instruction "RETI".

7.2.21.1 Page 1 External Data ROM

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA8	EXA7	EXA6	EXA5	EXA4	EXA3	EXA2	EXA1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(EXA1~EXA8) : Expanding Data ROM start address A1~A8

7.2.21.2 Page 2 External Data ROM

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA16	EXA15	EXA14	EXA13	EXA12	EXA11	EXA10	EXA9
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(EXA9~EXA16) : Expanding Data ROM start address A9~A16,,IOCB Page 1 Bit 7 is the MSB (EXA17) for Expanding Data ROM start address.

7.2.21.3 Page 3 Unused

7.2.22 R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : All of them are general purpose registers

7.3 Special Purpose Registers

7.3.1 A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

7.3.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT/EDGE	INT	TS	DAEN	PAB	RSR2	RSR1	RSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB) : Prescaler assigned bit

0/1 → TCC/WDT

Bit 4 (DAEN) : Current DA enable control

0/1 → disable/enable

Bit 5 (TS) : TCC signal source

Instruction clock / 16.384kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See Fig.15.

Bit 6 (INT) : INT enable flag

0 → interrupt masked by DISI or hardware interrupt

1 → interrupt enabled by ENI/RETI instructions

Bit 7(INT_EDGE) : interrupt edge type of P77

0 → P77 's interrupt source is a rising and falling edge signal.

1 → P77 's interrupt source is a falling edge signal.

The CONT register is readable (CONTR) and writable (CONTW). There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8-bit counter is available for TCC or WDT determined by the status of Bit 3 (PAB) of the CONT register. See the prescaler ratio in the CONT register. Fig. 25 depicts the circuit diagram of TCC/WDT. Both TCC and prescaler will be cleared by instructions which write to TCC each time. The prescaler will be cleared by the WDTC and SLEP instructions, when in WDT mode.

The prescaler will not be cleared by SLEP instructions, when in TCC mode.

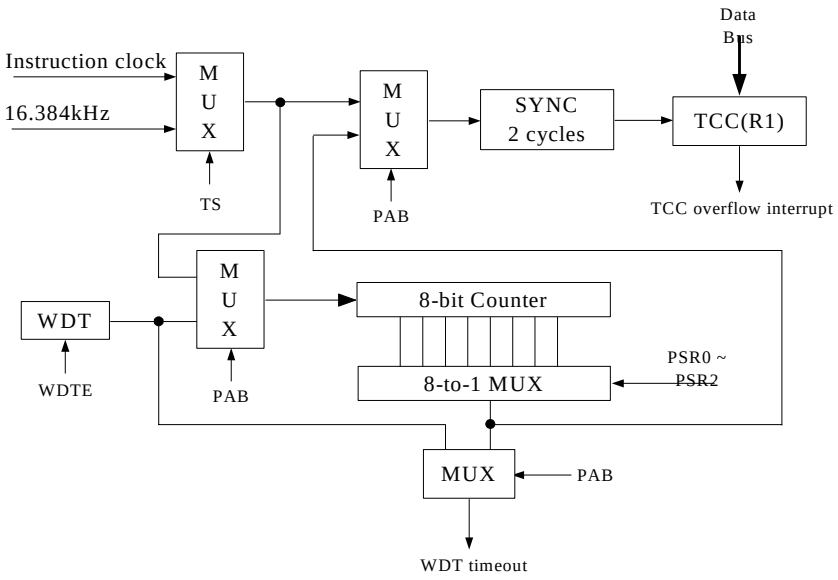


Fig. 25 Block Diagram of TCC and WDT

7.3.3 IOC5 Address Automatic Increase/Decrease Control, Data RAM Data Buffer 2

7.3.3.1 Page 0 Address Automatic Increase/Decrease control register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA2_ID	DA1_ID	DO_ID	–	DA2_IDEN	DA1_IDEN	DO_IDEN	–
R/W-1	R/W-1	R/W-1	×	R/W-0	R/W-0	R/W-0	×

Bit 0 : Undefined register, not for use

Bit 1 (DO_IDEN) : Enable Data ROM address flag Increase/Decrease Enable Function.

If this bit is set, the Data ROM address will increase or decrease after accessing (read or write) the Data ROM. ***When Expanded Data ROM is used, user can read or write into the external memory. By controlling RA Page 0 Bit 3, address auto increase/decrease function can be changed. Refer to RA Page 0 for detailed description.***

1/0 → Enable / Disable

Bit 2 (DA1_IDEN) : Enable Data RAM address Flag 1 (RD and RE register) Increase/Decrease Enable Function.

If this bit is set, the Data RAM address will increase or decrease after accessing (read or write) the Data RAM (RC register).

1/0 → Enable / Disable

Bit 3 (DA2_IDEN) : Enable Data RAM Address Flag 2 (IOC6 and IOC7) Increase/Decrease Enable Function.

If this bit is set, the Data RAM address will increase or decrease after accessing (read or write) the Data RAM (IOC5 register).

1/0 → Enable / Disable

Bit 4 : Undefined register, not for use.

Bit 5 (DO_ID) : Data ROM address automatic increase/decrease switch. Set to 1 means auto_increase, clear to 0 means auto_decrease.

1/0 → auto increase / auto decrease

Bit 6 (DA1_ID) : Data RAM address (RD and RE register) automatic increase/decrease switch. Set to 1 means auto_increase, clear to 0 means auto_decrease.

1/0 → auto increase / auto decrease

Bit 7 (DA2_ID) : Data RAM address (IOC6 and IOC7 register) automatic increase/decrease switch. Set to 1 means auto_increase, clear to 0 means auto_decrease.

1/0 → auto increase / auto decrease

7.3.3.2 Page 1 Data RAM Data Buffer 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM2D7	RAM2D6	RAM2D5	RAM2D4	RAM2D3	RAM2D2	RAM2D1	RAM2D0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0 ~ Bit 7 (RAM1D0 ~ RAM1D7) : Data RAM buffer for RAM reading or writing.

Location RC~RE Page 2, user can move a large number of continuous data from an address to another into the data RAM.

Example (move data from 0x0000 to 0x1000):

```
BC      R3,@5
MOV  A , @0xF0    ;Enable Data RAM Flag 1 and Flag 2
                  ;auto_increase function
IOW     0x05
BS      R3 , @5   :Set corresponding page
BS      R3 , @6
BC      R3 , @7
MOV  A , @0x00    ;Assign Data RAM Index 1
                  ;start address ”0x0000”
MOV     0x0D , A
MOV     0x0E , A
```

```
IOW  0x06          ; Assign DATA RAM Index 2 start
                   ; address ”0x1000”
MOV     A , @0x10
IOW     0x07
MOV     A , 0x0C  ;Read data from Index 1(address:0x0000)
IOW     0x05      ;Write data to Index 2(address:0x1000)
MOV     A , 0x0C  ;Read data from Index 1(address:0x0001)
IOW     0x05      ;Write data to Index 2(address:0x1001)
:
:
```

7.3.4 IOC6 Port 6 I/O Control, Data RAM Address (L)

7.3.4.1 Page 0 Port 6 I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOC60 ~ IOC67) : Port 6 (0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

7.3.4.2 Page 1 Data RAM Address 2 (L)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM2A7	RAM2A6	RAM2A5	RAM2A4	RAM2A3	RAM2A2	RAM2A1	RAM2A0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 7 (RAM2A0 ~ RAM2A7) : Data RAM address (Address 0 to Address 7) for RAM reading or writing

7.3.5 IOC7 PORT 7 I/O Control, Data RAM Address 2 (H)

7.3.5.1 Page 0 Port 7 I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOC70 ~ IOC77) : Port 7(0~7) I/O direction control register

0 → relative I/O pin as output

1 → relative I/O pin into high impedance

7.3.5.2 Page 1 Data RAM Address 2 (H)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	RAM2A11	RAM2A10	RAM2A9	RAM2A8
×	×	×	×	R/W-X	R/W-X	R/W-X	R/W-X

Bit 0~Bit 3 (RAM2A8 ~ RAM2A11) : Data RAM address (Address 8 to Address 11) for RAM reading or writing

Bit 4~Bit 7 : Undefined register, not for use.

7.3.6 IOC8 Port 8 I/O Control

7.3.6.1 Page 0 Port 8 I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC80 ~ IOC87) : Port 8 (0~7) I/O direction control register

0 → puts the relative I/O pin as output

1 → puts the relative I/O pin into high impedance

7.3.6.2 Page 1 Undefined register

This register is un*implemented, not for *use.

7.3.7 IOC9 Port 9 I/O Control

7.3.7.1 Page 0 Port 9 I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : Port 9 (0~7) I/O direction control register

0 → puts the relative I/O pin as output

1 → puts the relative I/O pin into high impedance

7.3.7.2 Page 1 Undefined register

This register is un*implemented, not for *use.

7.3.8 IOCA Undefined Register

IOCA Page 0 and Page 1 are un*implemented, not for *use.

7.3.9 IOCB Port B I/O Control, External LCD Driver Interface (for EMC 65x132)

7.3.9.1 Page 0 Port B I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOCB0~IOCB7) : Port B(0~7) I/O direction control register

0 → puts the relative I/O pin as output

1 → puts the relative I/O pin into high impedance

7.3.9.2 Page 1 External LCD Driver Controller

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA17	CWPWR	×	×	CSS	CSSON	DIS	EXLCD
R/W-0	R/W-0	×	×	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0(EXLCD) : External LCD driver enable/disable

0/1 → Port B, Port C normal IO/External LCD driver control (RE Page 2 LCD0, LCD1 = 1)

If EXLCD is equal to 0, Port B and Port C output are normal IO. When EXLCD is equal to 1, Port B and Port C are switch to external LCD driver control pin. At this time, when user executes a read or write Port B instruction, Port C timing characteristic is shown below:

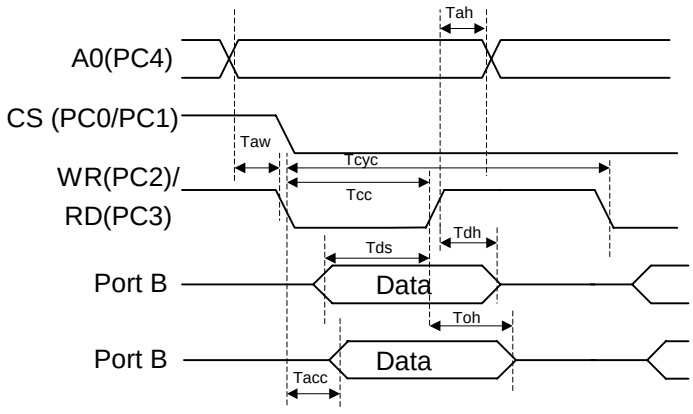


Fig. 26 Timing Characteristics of the External LCD Driver Data Read/Write

Symbol	Applicable Pins	Rated Value		Unit
		Min.	Max.	
Tah	A0	0	-	ns
Taw	A0	0	-	
Tcyc	A0	150	-	
Tcc	WR/RD	60	-	
Tds	D0 ~D7	20	-	
Tdh	D0 ~D7	10	-	
Tacc	D0 ~D7	-	60	
Toh	D0 ~D7	10	40	

Tah : Address hold time

Taw : Address set-up time

Tcyc : System cycle time

Tcc : Pulse width

Tds : Data set-up time

Tdh : Data hold time

Tacc : Read access time

Toh : Output disable time

User can operate in coordination with the on-chip Data ROM address automatic increase function to write a large number of data from the internal Data ROM to the external LCD RAM.

Example (To collocate EM9L8580 LCD driver):

START:

```
MOV   A , @0x0C;
IOW   IOC5_PAGE0     ;Set Data ROM address automatic increase
                     ;after read/write data
MOV   A , @0x09
IOW   IOCB_PAGE1     ;External LCD driver Chip 1 Instruction mode
                     ;select
MOV   A , @0xB0;
MOV   RB_PAGE0 , A   ;Set external LCD driver start address Page 0
MOV   A , @0x10
MOV   RB_PAGE0 , A
MOV   A , @0x00
MOV   RB_PAGE0 , A    ; Set external LCD driver start address Column 0
MOV   A , @0x00;
```

```
MOV  R7_PAGE1 , A;
MOV  R8_PAGE1 , A;
MOV  R9_PAGE1 , A  ;Start address: 0x00000
MOV  A , @0x0B
IOW  IOCB_PAGE1    ;select data mode
CN1:
MOV  A , R6_PAGE1  ;read data from Data ROM and address flag
                   ;increase
MOV  RB_RAGE0 , A  ;write data to external LCD driver
JMP   LOOP
```

Bit 1 (DIS) : External LCD driver Data/Instruction switch

0/1 → Instruction/Data

When EXLCD is equal to 1 and DIS bit equal to 0, the MCU will transmit/receive instruction. A0 (Port C7) will output a "0". If the DIS bit is set to 1, the MCU will transmit/receive data. A0 (Port C4) will output a "1".

Bit 2 (CSSON) : External LCD driver select enable

CSSON	CSS0	CS1..CS2	
		Low	High
0	×	–	CS1, CS2
1	0	CS1	CS2
1	1	CS2	CS1

Example for EMC 65x132 LCD driver :

```
MOV  A, @0x01
IOW  IOCB_PAGE1    ;Select external LCD driver & Instruction
                   ;mode
MOV  A,@0xB0
MOV  RB,A          ;Select external LCD driver COM0
MOV  A,@0x10
MOV  RB,A          ;Select external LCD driver SEG Upper 4 bit = 0
MOV  A,@0x00
MOV  RB,A          ;Select external LCD driver SEG Lower 4 bit = 0
MOV  A,@0x03
IOW  IOCB_PAGE1    ;Switch to DATA mode
MOV  A,@0xFF
MOV  RB,A          ;Write 0xFF to COM0 &SEG0
:
```

User must assign an external LCD address for the first time. After writing or reading the display data, the Segment address is automatically incremented. Hence, the MCU can continuously write or read data to the address.

Bit 3 (CSS) : External LCD driver chip select bit

0/1 → Chip 1 / Chip 2

Bit 4 ~ Bit 5 : Unused

Bit 6(CWPWR) : CAS Decoder Power Control

0/1 → Power off / Power on

Bit 7 (EXA17) : Expanded Data ROM start address MSB. This bit can be set only at the connected pin "EXSAL" to VDD.

7.3.10 IOCC Port C I/O Control, Port 6 Pull-high Register

7.3.10.1 Page 0 Port C I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 7 (IOCC0~IOCC7) : Port C (0~7) I/O direction control register

0 → puts the relative I/O pin as output

1 → puts the relative I/O pin into high impedance

7.3.10.2 Page 1 Port 6 Pull-high Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(PH60~PH67) : PORT6(0~7) pull high control register

0 → disable pull-high function

1 → enable pull-high function

7.3.11 IOCD Port D I/O Control, Port 7 Pull-high Register

7.3.11.1 Page 0 Port D I/O Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0~Bit 6 (IOCD0~IOCD6) : Port D (0~6) I/O direction control register

0 → puts the relative I/O pin as output

1 → puts the relative I/O pin into high impedance

7.3.11.2 Page 1 Port 7 Pull High Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7(PH70~PH77) : Port 7(0~7) pull high control register

0 → disable pull-high function

1 → enable pull-high function

7.3.12 IOCE Interrupt Mask, Differential Energy Detect

7.3.12.1 Page 0 Interrupt Mask Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 : Interrupt enable bits

0/1 → disable interrupt/enable interrupt

7.3.12.2 Page 1 Differential Energy Detect

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRSEL	DEDD	EDGE	WUEDD	CW_SMB	DEDCLK	DEDPWR	DEDTHD
R/W-0	R	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (DEDTHD) : Minimum detection threshold for Differential Energy Detector (DED)

0/1 → -45dBm/-30dBm

Bit 1 (DEDPWR) : Power control of Differential Energy Detector (DED)

0/1 → Power off / Power on

Bit 2 (DEDCLK) : Operating clock for Differential Energy Detector (DED)

0/1 → 32.768kHz/3.5826 MHz

This bit is used to select operating clock for the Differential Energy Detector (DED). When this bit is set to “1”, the PLL is also enabled regardless of RA Bit 6 (ENPLL). During this time, the Energy detector works at high frequency mode. When this bit is set to “0”, the Energy Detector works at a low frequency mode. The difference between high frequency and low frequency is as follows.

DEDPWR	DEDCLK	ENPLL	Energy Detector Clock	Main CLK
0	×	×	×	Determined by ENPLL
1	0	0	32.768 kHz	Disable
1	0	1	32.768 kHz	Enable
1	1	0	3.5826 MHz	Enable
1	1	1	3.5826 MHz	Enable

Note: ”×” means don’t care

Bit 3(CW_SMB) : Call Waiting / short message receiver switch

0 → Short message mode select ±5.5% CAS tone accepted frequency range deviation. (Protocol: ±5%)

1 → Call Waiting mode select ±2.0% CAS tone accepted frequency range deviation.

Bit 4 (WUEDD) : Wake-up control for the Energy Detector (DED) output data

1/0 → enable/disable

Bit 5 (EDGE) : Wake-up and interrupt trigging edge control of the Energy Detector (DED) output

1/0 → Rising edge and Falling edge trigger / Falling edge trigger

Bit 6(DEDD) : Output data for Differential Energy Detector (DED). If the input signal from TIP/EGIN1 and RING/EGIN2 pins to Differential Energy Detector is over the threshold level setting at IOCE Page 2 Bit 0 (DEDTHD), the DED will extract the zero-crossing pulse waveform corresponding to the input signal.

Bit 7 (VRSEL) : Reference voltage VR selection bit for Comparator

0 → VR = VDD

1 → VR = 2.0V

When this bit is set to "0", V2_0 reference circuit will be powered off. The 2.0V reference circuit is only powered on when this bit and RA Page 2 bit 7 (CMPEN) are all set to "1".

7.3.13 IOCF Interrupt Mask Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBF/STD	FSK/CW	–	UART	DED	CNT2	CNT1	TCC
R/W-0	R/W-0	×	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0~Bit 7 : Interrupt enable bits

0/1 → Disable interrupt/enable interrupt

7.4 I/O Port

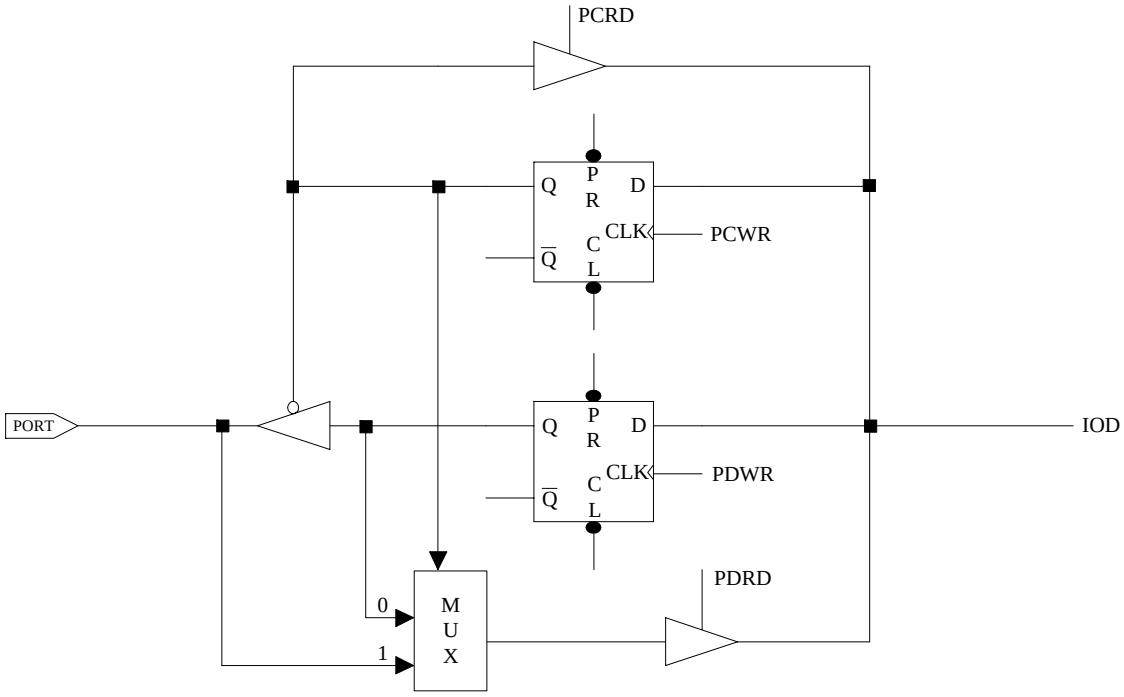


Fig. 27 I/O Port and I/O Control Register Circuit

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 27.

* ***The MCU will have a large current consumption when the IO is set to input and at floating state. Be careful to set unused IO to output or connect them to VDD or GND when they are set to input status.***

7.5 Reset

The Reset can be caused by:

(1) Power-on voltage detector reset (POVD) and power on reset

(2) WDT time-out (if enabled and in Green or Normal mode)

(3) /Reset pin pull low

NOTE

In Case (1), the POVD is controlled by Code Option. If you enable POVD, the CPU will reset at 2V and below, thus, the CPU will consume more current, which is 3μA. The power-on reset circuit is always enabled. It will reset the CPU at 1.4V and consume 0.5μA.

Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started
- The Program Counter (R2) is set to all "0"
- When powered on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared
- The Watchdog timer and prescaler counter are cleared
- The Watchdog timer is disabled
- The CONT register is set to all "1"
- The other register (Bit 7 ~ Bit 0)

Address	R Register Page 0	R Register Page 1	R Register Page 2	R Register Page 3	IOC Register Page 0	IOC Register Page 1
1	×××× ××××	0000 0000	0000 0000	×××× ××××	--	--
4	00×× ××××	×××× ××××	×××× ××××	×××× ××××	--	--
5	×000 0000	0000 0000	0000 0000	×××× 0000	1111 0000	×××× ××××
6	×××× ××××	×××× ××××	0000 0000	0000 0000	1111 1111	×××× ××××
7	×××× ××××	×××× ××××	0000 0000	0000 0000	1111 1111	×××× ××××
8	×××× ××××	×××× ××××	×××× 0000	×××× ××××	1111 1111	00000000
9	×××× ××××	×××× ××××	0000 0×××	×××× ×000	1111 1111	00000000
A	0000 0××0	×××× ××××	0000 0000	0000 0000	×××× ××××	×××× ××××
B	×××× ××××	×××× ××××	1111 1111	0000 0000	1111 1111	00×× 0000
C	×××× ××××	×××× ××××	1111 1111	×××× ××××	1111 1111	0000 0000
D	×××× ××××	×××× ××××	×××× ××××	×××× ××××	1111 1111	0000 0000
E	0000 0000	×××× ××××	××00 ××××	×××× ××××	0000 0000	0×00 0000
F	00×× 0000	0000 0000	0000 0000	×××× ××××	0000 0000	--

7.6 Wake-up

The controller provides a power saving mode:

(1) Sleep mode, RA (7) = 0 + "SLEP" instruction

The controller will turn off all the CPU and crystal. User has to turn off by software all the other circuits with power control like Keytone control or PLL control (which has an enable register).

Wake-up from Sleep mode:

(1) WDT time out

(2) External interrupt

(3) /Reset pull low

All these cases will reset the controller, and run the program at address zero. The status is the same as that of the power-on reset.

7.7 Interrupt

RE and RF are the interrupt status registers which record the interrupt request in flag bits. The IOCE and IOCF are the interrupt mask registers. The TCC timer, Counter 1 and Counter 2 are internal interrupt sources. P70 ~ P77 (INT0 ~ INT7) are external interrupt input with external interrupt sources. If the interrupts come from these interrupt sources, then the RE or RF register will generate a '1' flag to the corresponding register if the IOCE or IOCF registers are enabled. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RE and RF registers. The interrupt flag bit must be cleared by software before leaving the interrupt service routine and enabling interrupts, to avoid recursive interrupts.

7.8 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

Legend: **addr:** address **i:** Table pointer control **p:** special file register (0h~1Fh)
b: bit **k:** constant **r:** File Register

Binary Instruction	Hex	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2 + A → R2 bits 9, 10 do not clear	Z, C, DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1

Binary Instruction	Hex	Mnemonic	Operation	Status Affected	Instruction Cycle
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0 100b bbrr rrrr	0××××	BC R,b	0 → R(b)	None	1
0 101b bbrr rrrr	0××××	BS R,b	1 → R(b)	None	1
0 110b bbrr rrrr	0××××	JBC R,b	if R(b)=0, skip	None	2 if skip
0 111b bbrr rrrr	0××××	JBS R,b	if R(b)=1, skip	None	2 if skip
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 1kkk kkkk	1E8k	PAGE k	K→R5(4:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC	1

Note: One instruction cycle = 2 main clock

7.9 Code Option Register

The controller has one Code option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

7.9.1 Code Option Register 1 (Program ROM)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	/DED	/POVD

Bit 0 (/POVD) : Power-on Voltage Detector

0/1 → Enable / disable the Voltage Detector

/POVD	2.2V /POVD Reset Voltage	2.2V Power-on Reset Voltage	Sleep Mode Current (VDD=5V)
1	No	Yes (2.2V)	1μA
0	Yes (2.2V)	No	15μA

Bit 1(/DED) : Differential Energy Detect function enable bit

0/1 → Enable / disable DED function

7.10 Call Waiting Function Description

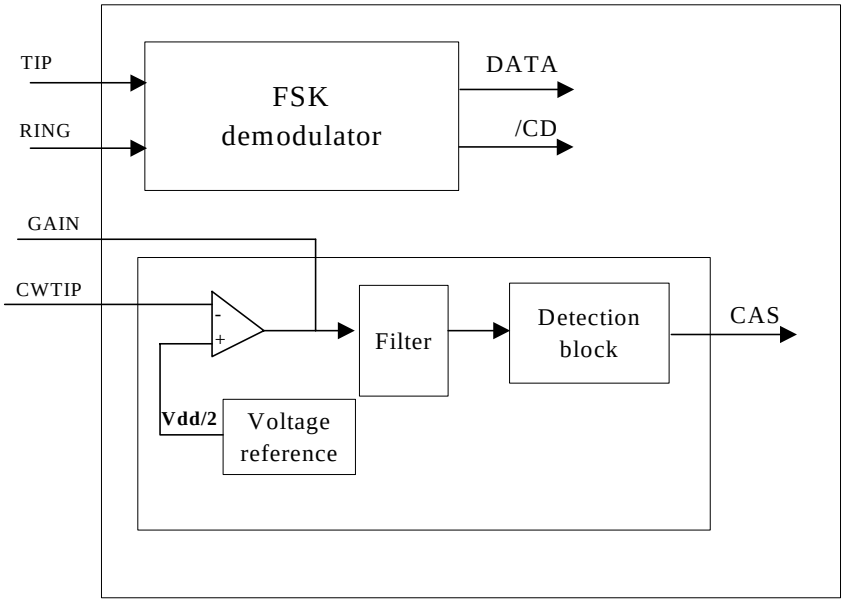


Fig.28 Call Waiting Block Diagram

Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. This way the customer can still receive important calls while engaged in a current call. The Call Waiting Decoder can detect CAS (Call-Waiting Alert Signal 2130Hz plus 2750Hz) and generate a valid signal on the data pins.

The call waiting decoder is designed to support the Caller Number Deliver feature, which is offered by regional Bell Operating Companies.

In a typical application, after enabling the CW circuit (by R5 Page 3 Bit 3 & Bit 4) this IC receives Tip and Ring signals from twisted pairs. The signals as inputs by the pre-amplifier, and the amplifier sends input signal to a band pass filter. Once the signal is filtered, the Detection block decodes the information and sends it to RE Page 2 Bit 7. The output data is made available at RE CAS bit.

The data is CAS signals. The CAS is normal high. When this IC detects a 2130Hz and a 2750Hz frequency, the CAS pin goes to low.

7.11 Differential Energy Detector (DED)

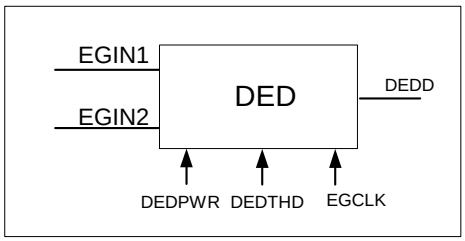


Fig.29 DED Block Diagram

The Differential Energy Detector is differential input level and zero crossing detector named as DED. It can detect any incoming AC signal above its threshold level and outputs a corresponding zero-crossing frequency pulse. For this energy detector, user can set its minimum detection threshold level at –35dBm or –45dBm through the DEDTHD bit. All the minimum detection value can be achieved under an input capacitor of more than 4700 pF and input resistor of 100 kΩ. The energy detector can be power-controlled by IOCE Page 1 Bit 1 (DEDPWR).

Register bits of the Energy Detector :

Register Bits	Descriptions
RF Page 0 Bit 3 (DED)	DED : Interrupt flag of DED output data
IOCE Page 1 Bit 7 (DEDD)	DEDD : Output data of DED
IOCE Page 1 Bit 5 (EDGE)	EDGE : edge control of DED output data **1/0** → Falling edge trig. / Rising edge and Falling edge trig.
IOCE Page 1 Bit 4 (WUEDD)	WUEDD : Wake-up control of DED output data **1/0** → enable/disable
IOCE Page 1 Bit 6 (DED)	DED : Interrupt mask of DED output data **1/0** → enable/disable interrupt of DED output data
IOCE Page 1 Bit 0 (DEDTHD)	DEDTHD : Minimum detection threshold of DED **0/1** → -45dBm/-30dBm
IOCE Page 1 Bit 1 (DEDPWR)	DEDPWR : Power control of DED **0/1** → power off/power on
IOCE Page 1 Bit 2 (DEDCLK)	DEDCLK : operating clock of DED **0** : low frequency clock **1** : high frequency clock

8 Absolute Maximum Ratings

Rating	Symbol	Min.	Typ.	Max.	Unit
DC Supply Voltage	VDD	-0.3		6	V
Input Voltage	Vin	VDD-0.5	VDD	VDD+0.5	V
Operating Temperature Range	Ta	0	25	70	°C

9 DC Electrical Characteristic

(Operation current consumption for Analog circuit)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation current for FSK	I_FSK	VDD=3V, CID power on	–	1.5	2.5	mA
Operation current for CW	I_CW	VDD=5V, CID power on	–	1.5	2.5	mA
Operation current for DTMF Receiver	I_DR	VDD=3V, DTMFr power on	–	1.5	2.5	mA
Operation current for Tone generator	I_DTMF	VDD=3V, DTMF power on	–	0.5	0.8	mA
Operation current for Current DA	I_DA	VDD=3V, CDA power on	–	1.5	4	mA
Operation current for Comparator	I_CMP	VDD=5V, PT power on	–	0.1	–	mA

(Ta=0°C ~ 70°C, VDD=3V ± 5%, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current for input pins	IIL1	VIN = VDD, VSS	–	–	±1	μA
Input Leakage Current for bidirectional pins	IIL2	VIN = VDD, VSS	–	–	±1	μA
Input High Voltage	VIH	–	2.0	–	–	V
Input Low Voltage	VIL	–	–	–	0.8	V
Input high threshold Voltage	VIHT	/RESET, TCC, RDET1	2.0	–	–	V
Input low threshold Voltage	VILT	/RESET, TCC, RDET1	–	–	0.8	V
Clock Input High Voltage	VIHX	OSCI	1.8	–	–	V
Clock Input Low Voltage	VILX	OSCI	–	–	1.2	V
Output High Voltage (Ports 8, 9, B, C, D)	VOH1	IOH = -6mA	2.0	2.4	–	V
Output High Voltage (Ports 6, 7)	–	IOH = -10.0mA	2.0	2.4	–	V
Output Low Voltage (Ports 8, 9, B, C, D)	VOL1	IOL = 6mA	–	–	0.4	V
Output Low Voltage (Port 6, 7)	–	IOL = 10.0mA	–	–	0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS	–	-10	-15	μA
Power-down current (Sleep mode)	ISB1	All input and I/O pins at VDD, output pin floating, WDT disabled	–	1	4	μA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low clock current (Green mode)	ISB2	All input and I/O pins at VDD, CLK=32.768kHz, WDT disabled, Output pin floating All analog circuit disabled	–	30	40	μA
Operating supply current (Normal mode)	ICC	/Reset=High, PLL enable CLK=3.579MHz, Output pin floating, All analog circuits disabled		2	3	mA
Tone generator reference voltage	Vref2	–	0.5		0.7	VDD

Differential Energy Detector (DED), (Ta=25°C, VDD=3.0V ± 5%, VSS=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EGIN1	Operating current for SED	SEDCLK bit = 0		20	25	μA
EGIN2	Operating current for SED	SEDCLK bit = 0		20	25	μA

10 AC Electrical Characteristic

CPU Instruction Timing (Ta=25°C, VDD=3V, VSS=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.579MHz		60 550		us ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note: N = selected prescaler ratio

FSK AC Characteristic (Vdd = 3V, Ta = +25°C)

Characteristic	Min.	Typ.	Max.	Unit
FSK Sensitivity				
Low Level Sensitivity Tip & Ring @SNR 20dB	-40	-48	–	dBm
High Level Sensitivity Tip & Ring @SNR 20dB	–	0	–	dBm
Signal Reject	–	-51	–	dBm
FSK Twist				
Positive Twist (High Level)	+10	–	–	dB
Positive Twist (Low Level)	+10	–	–	dB
Negative Twist (High Level)	-6	–	–	dB
Negative Twist (Low Level)	-6	–	–	dB

CW AC Characteristic (Vdd=3V,Ta=+25°C)

Characteristic	Min.	Typ.	Max.	Unit
CW Sensitivity				
Sensitivity @SNR 20dB	–	-38	–	dBm
USA & Europe Mode				
Low Tone Frequency 2130Hz	–	±1.2	–	%
High Tone Frequency 2750Hz	–	±1.2	–	%
Chinese Call Waiting Mode				
Low Tone Frequency 2130Hz	–	±2.0	–	%
High Tone Frequency 2750Hz	–	±2.0	–	%
Chinese SMS Mode				
Low Tone Frequency 2130Hz	–	±5.5	–	%
High Tone Frequency 2750Hz	–	±5.5	–	%
CW Twist				
Twist	±7	–	–	dB

DTMF (DTMF Receiver) AC Characteristic (Vdd = 3V, Ta = +25°C)

Characteristic	Min.	Typ.	Max.	Unit
DTMF Receiver				
Low Level Signal Sensitivity	–	-36	–	dBm
High Level Signal Sensitivity	–	0	–	dBm
Low Tone Frequency	–	±2	–	%
High Tone Frequency	–	±2	–	%
DTMF Receiver Noise Endurance				
Signal-to-noise Ratio	15	–	–	dB

Tone Generators for AC Characteristic (Vdd = 3V, Ta = +25°C)

Characteristic	Min.	Typ.	Max.	Unit
Tone 1/Tone 2 signal strength (root mean square voltage)				
Tone 1 signal strength V1rms *1	130	155	180	mV
Tone 2 signal strength V2rms *1		1.259V1rms		mV
Tone Twist				
(Tone 1 – Tone 2) twist	–	-2	–	dB
Tone frequency deviation				
Frequency deviation	–	–	±1	%

Note *1 : V1rms and V2rms has 2dB difference. It means 20log (V2rms/V1rms) = 20log1.259 = 2 (dB)

DED AC Characteristic (Vdd = +3.0V, Ta = + 25°C)

Characteristic	Min.	Typ.	Max.	Unit
Input sensitivity TIP and RING for DED, DEDTHD bit=0	–	-45	–	dBm
Input sensitivity TIP and RING for DED, DEDTHD bit=1	–	-35	–	dBm

Timing characteristic (Vdd = 3V, Ta=+25°C)

Description		Symbol	Min.	Typ.	Max.	Unit
Oscillator Timing Characteristic						
OSC start up	32.768kHz	Tosc	–	–	1500	ms
	3.579MHz PLL	–	–	–	10	us
Timing characteristic of reset						
Minimum width of reset low pulse		Trst	3	–	–	uS
Delay between reset and program start		Tdrs	–	18	–	mS
FSK Timing Characteristic						
Carrier detect low		Tcdl	–	10	14	ms
Carrier detect low to data valid		Tcdv	–	10	20	ns
Power up to FSK(setup time)		Tsup	–	15	20	ms
End of FSK to Carrier Detect high		Tcdh	–	–	4	ms
CW Timing Characteristic						
CAS input signal length (2130, 2750 Hz @ -20dBm)		Tcasi	–	80	–	ms
Call waiting data detect delay time		Tcwd	–	42	–	ms
Call waiting data release time		Tcwr	–	26	–	ms
DTMF Receiver Timing Characteristic						
Tone Present Detection Time		Tdp	–	*1	–	–
The guard-times for tone-present (C=0.1µF, R=300K)		Tgtp	–	30	–	ms
The guard-times for tone-absent (C=0.1µF, R=300K)		Tgta	–	30	–	mS
Propagation Delay (St to Q)		Tpq	–	8	–	us
Tone Absent Detection Time		Tda	–	*2	–	ms
SPI Timing Characteristic (CPU Clock 3.58MHz and Fsco = 3.58MHz /2)						
/SS set-up time		Tcss	560	–	–	ns
/SS hold time		Tcsh	250	–	–	–
SCLK high time		Thi	250	–	–	ns
SCLK low time		Tlo	250	–	–	ns
SCLK rising time		Tr	–	15	30	ns
SCLK falling time		Tf	–	15	30	ns

Description	Symbol	Min.	Typ.	Max.	Unit
SDI set-up time to the reading edge of SCLK	Tisu	25	–	–	ns
SDI hold time to the reading edge of SCLK	Tihd	25	–	–	ns
SDO disable time	Tdis	–	–	560	ns

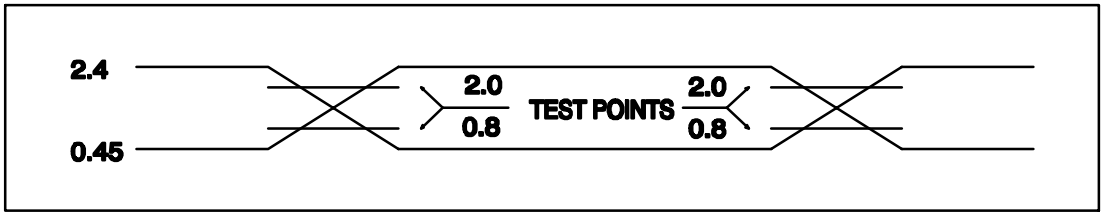
Note *1 : Controlled by software
*2 : Controlled by RC circuit

Data ROM access timing characteristic

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Tdiea	Delay from Phase 3 end to INSEND active	Cl=100pF			30	ns
Tdiei	Delay from Phase 4 end to INSEND inactive	Cl=100pF			30	ns
Tiew	INSEND pulse width		30			ns
Tdca	Delay from Phase 4 end to CA Bus valid	C1=100pF			30	ns
Tacc	ROM data access time		100			ns
Tcds	ROM data setup time		20			ns
Tcdh	ROM data hold time		20			ns
Tdca-1	Delay time of CA-1	C1=100pF			30	ns

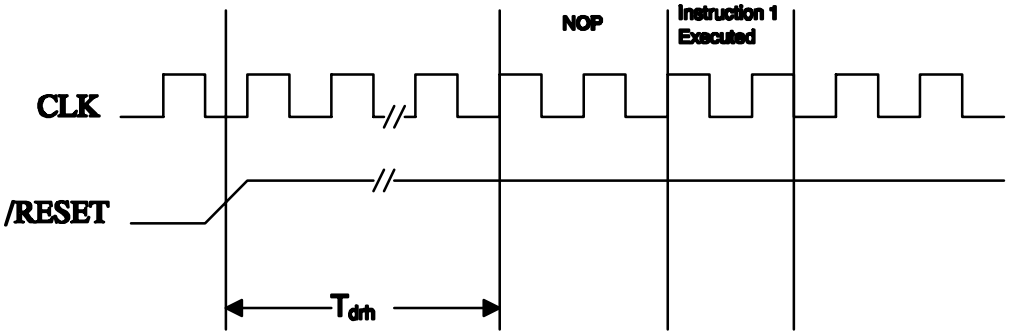
11 Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

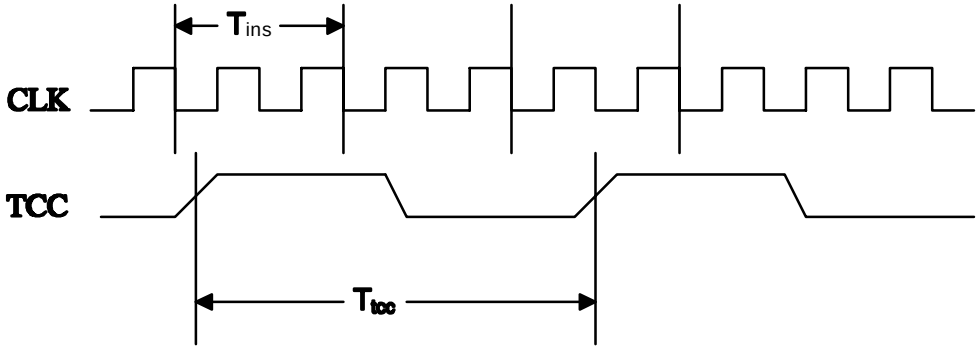


Fig. 30 AC Timing

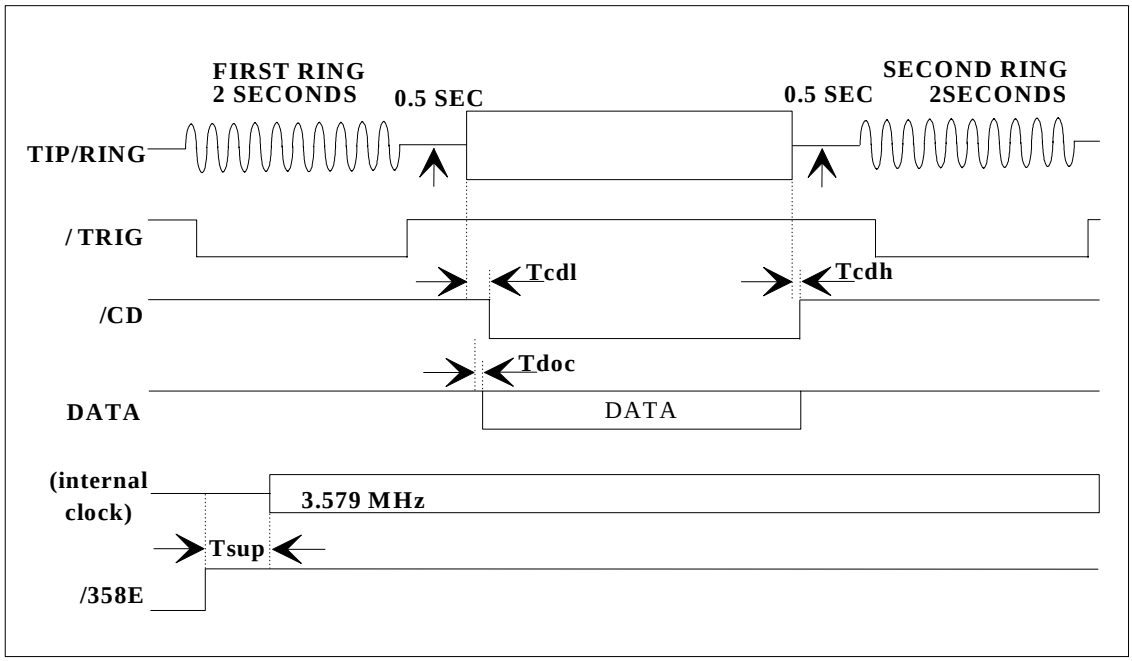


Fig. 31 FSK Timing Diagram

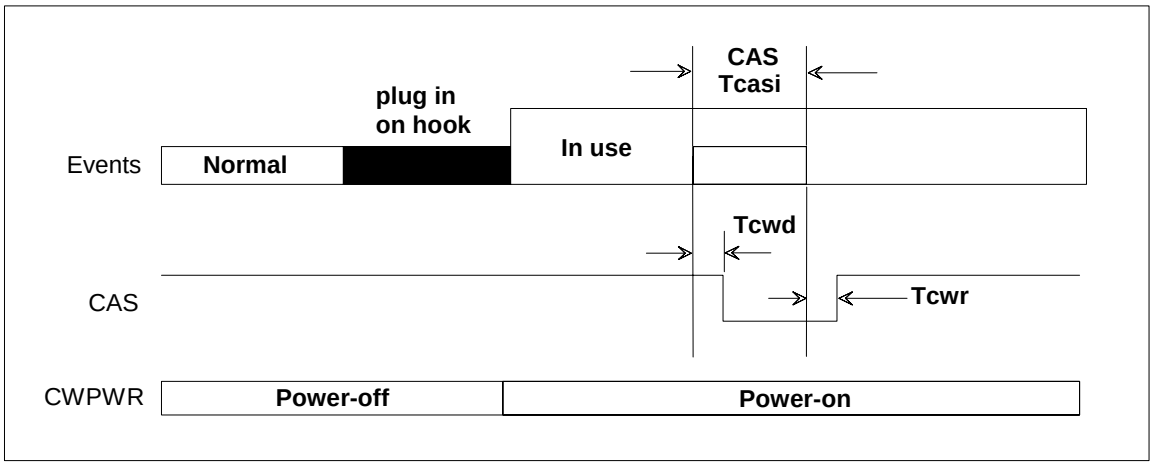


Fig. 32 Call Waiting Timing Diagram

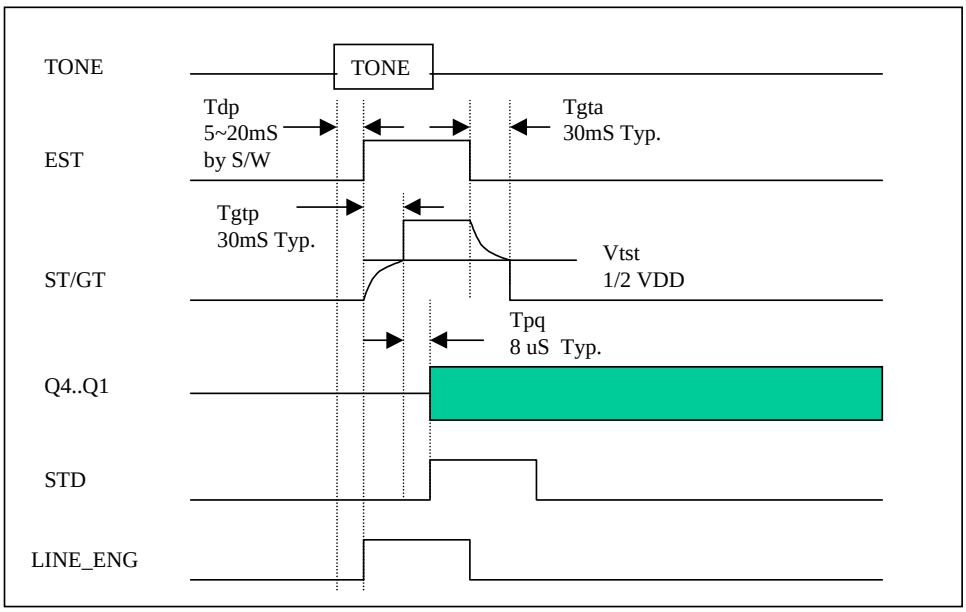


Fig. 33 DTMF Receiver Timing Diagram

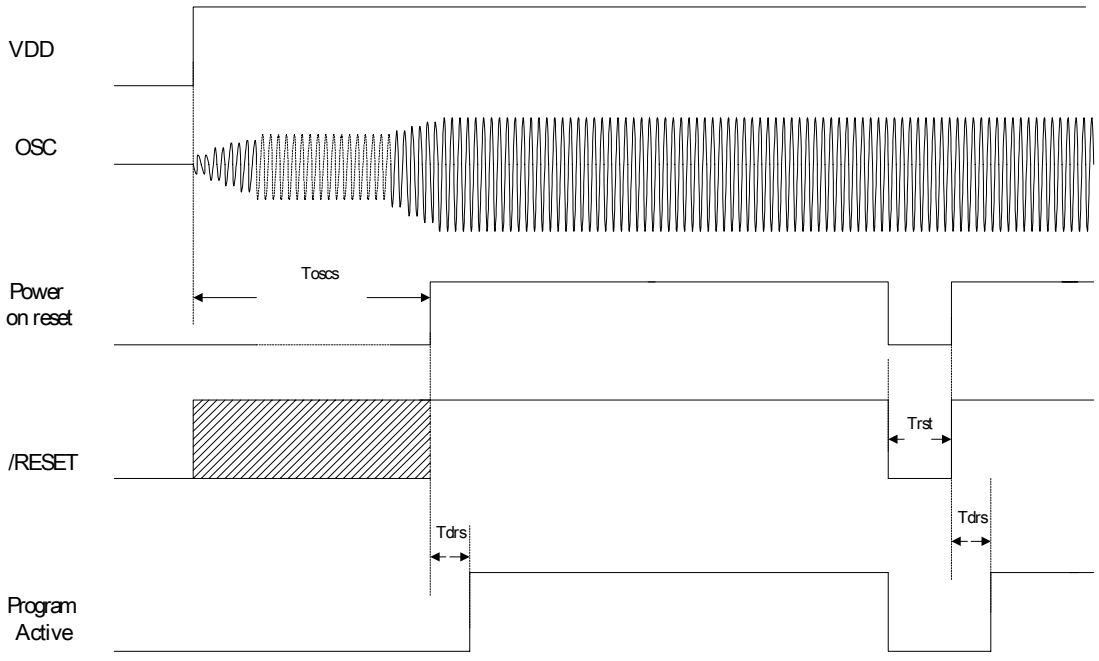


Fig. 34 Relationship between OSC Stable And Reset Time

12 Application Circuit

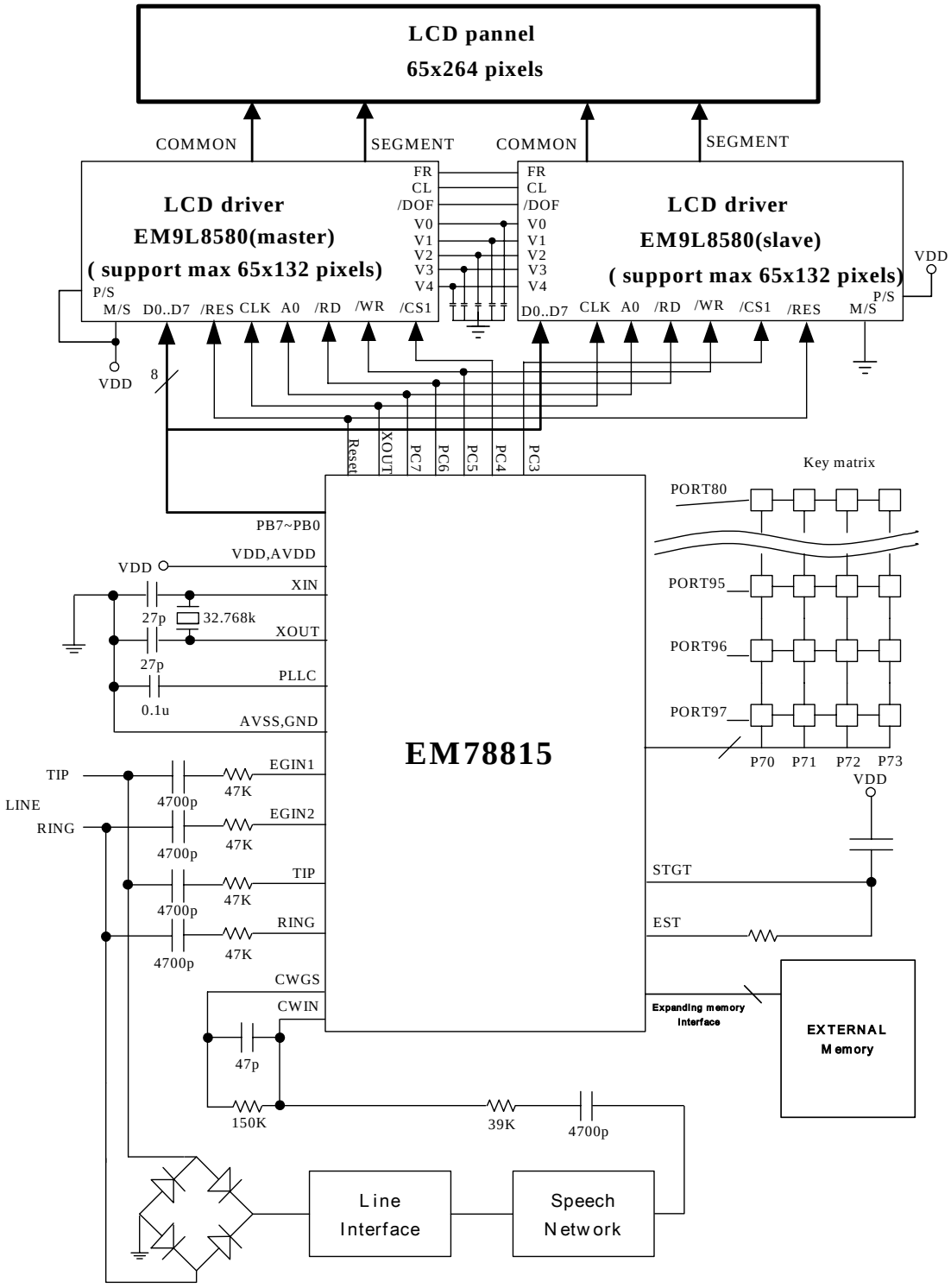


Fig. 35 External Multi-chip LCD Driver Application Circuit

APPENDIX

A Application Note

1. In targeting interrupt and program run to address 0x0008, ACC, R3 (Status), R5 (Program Page) and R4 (6, 7) will be automatically saved and R3 (6, 7) R register page will be set to Page 0, and reload after the instruction “RETI”.
2. 0V reference voltage will power down when both RD Page 2 Bit 7 (DAREF) and RA Page 2 Bit 7 (CMPEN) are cleared to 0.
3. Before using Keytone function, set Port 76 as output type.
4. For accessing data ROM, EM78P815 (OTP) can work at 10.74MHz, but note that only ROM type EM78815 can work at 5.3MHz.
5. While switching the main clock (regardless of high freq to low freq or vice versa), adding 6 instructions delay (NOP) is required.
6. Do not switch the MCU operation mode from normal mode to sleep mode directly. Before going into sleep mode, switch the MCU to green mode first.
7. ***Always keep RA Page 0 Bit 7 = 0, otherwise, unexpected error will occur.***