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CLARE
An IXYS Company

MXED401

200-Column Cholesteric LCD Driver

FEATURES:

- Drives Reflective-type Liquid Crystal Displays
- Black-White or Gray-Scale
- Cholesteric LCD (ChLCD) Compatible
- 200 Output Channels, Cascadeable
- 192-Channel Mode
- Token-Based Bi-directional Data Transfer
- 6-Bit Data to support 64-Level Gray-Scale
- ±2V to ±7V panel drive
- 4mA Minimum Source/Sink at ±7VOutput Levels
- 2.5V to 5V logic supply
- 26 MHz clock frequency
- 4mA Minimum Source/Sink at ±7V Output Levels
- Gold-Bumped Die @ 60 micron Output Pitch

OVERVIEW:

Clare introduces the MXED401, targeted for the emerging non-volatile reflective LCD market, specifically bi-stable and multi-stable Cholesteric LCD's. The MXED401 supports 200 phase-controlled voltage data outputs. This is the first standard product driver for ChLCD display panels.

FUNCTIONAL DESCRIPTION:

The MXED401 driver functions as a level shifter with a resting state at ground potential. Proper operation of the logic enables gray-scale capability. The output is a 128 Counter Clock (CCLK) event where each channel is a low resistive switch to external symmetric (with respect to ground) voltage supplies. Proper operation of the logic allows gray scale capability. The output is initially low (MV4) from one to sixty-four CCLK times, then continuously high (PV4) for sixty-four CCLK times, returning low for the balance of the 128 CCLK cycle (before returning to its quiescent value (VSS2)). The data driver chip is manufactured in a high voltage (30 V) CMOS process and is available in gold-bumped-die form.

The Token Bit Shift Register is used to control data latch timing for the Temporary Storage Register. A token bit (initialized by SRIN input) is transferred sequentially among the 200 possible (internal) outputs of the Shift register. This allows data to fill the Temporary Storage Register to in a Right to Left fashion. When the Temporary Register is filled its contents may be transferred to the Output Storage register via the LAT input. Output phase control is then accomplished by the Pulse Phase Shift Logic, data then passes to the High Voltage Translator unit to control the three output switches associated with each column output driver.

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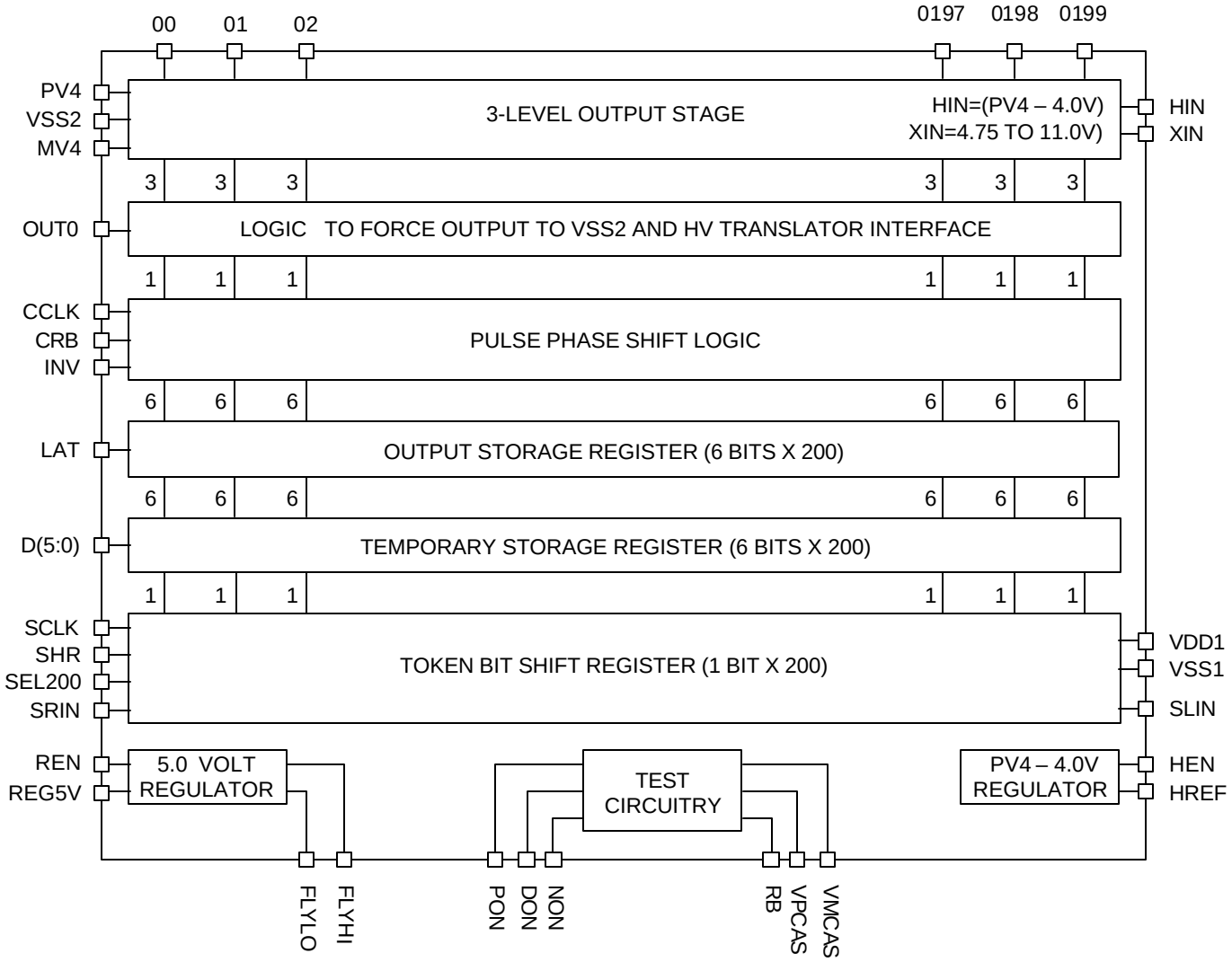
FIGURE 1 - MXED401 BLOCK DIAGRAM



MXED401 DATA SHEET

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ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Max.	Unit
Supply voltage VDD1	-0.3	7.0	V
Supply voltage PV4	-0.3	9.0	V
Supply voltage MV4	-9.0	+0.3	V
XIN input	-0.3	12.0	V
HIN input	PV4-6.0	PV4+0.3	V
Logic input levels	-0.3	VDD1 + 0.3	V
Storage temperature	-65	150	Celsius

OPERATING CONDITIONS

Parameter	Min.	Max.	Unit
Supply voltage VDD1	2.5	5.5	V
Supply Voltage PV4	2	7	V
Supply Voltage MV4	-7	-2	V
HIN	PV4-4.2	PV4-3.8	
XIN	4.75	11	V
Temperature Ambient	-20	80	Celsius

CIRCUIT DESCRIPTION

Voltage Regulator

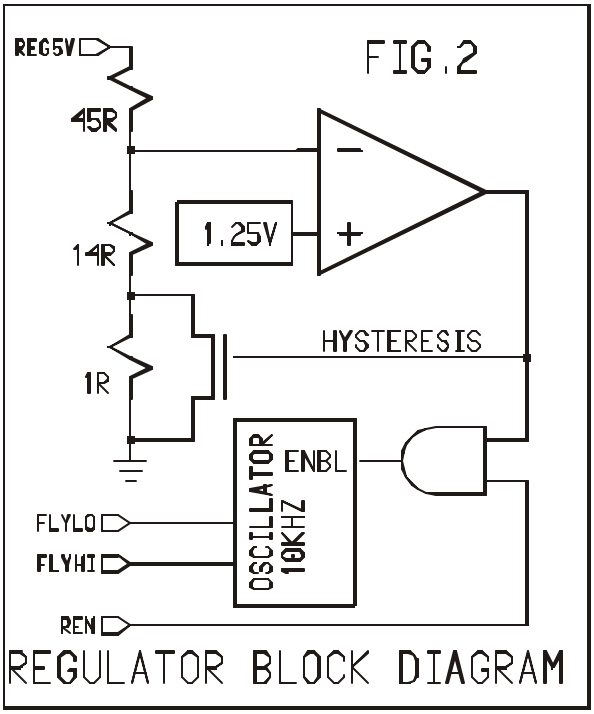
This product may be operated from supplies as low as 2.5 Volts. The output drive transistors require a voltage of 5.0 volts to 11.0 volts on the XIN pin to assure proper circuit operation. This bias voltage may be developed on the chip or provided by the system designer. When XIN is provided externally, the REN (Regulator ENable) pin is held low, and the FLYHI/FLYLO pins are left unconnected.

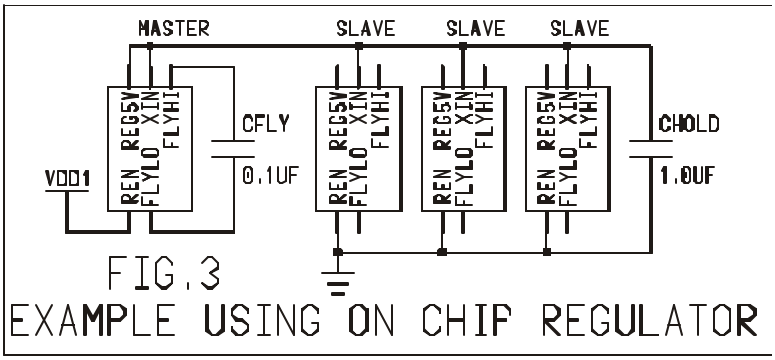
Systems lacking an available bias may use the on chip voltage regulator. The circuit is enabled by forcing REN high (to VDD1). This will cause an on-chip oscillator/charge pump circuit to operate continuously and output a somewhat regulated 5 volts at pin REG5V. A capacitor (CFLY=0.1uF) is connected between pins FLYHI and FLYLO. A storage capacitor (CHOLD=1.0uF) is required on REG5V. The XIN input is then connected to the REG5V output. The charge pump is capable of driving 18 XIN loads so generally only one or two circuits are used as regulator sources. In systems where more than one regulator circuit is enabled it is forbidden to short their respective HOLD capacitors. Enabling the regulator causes an additional DC current of 65uA (130 uA maximum) to flow from VDD1 to VSS1.

FIGURE 2 - REGULATOR BLOCK DIAGRAM

FIGURE 3 - EXAMPLE USING ON CHIP REGULATOR

FIGURE 4 - EXAMPLE USING EXTERNAL BIAS





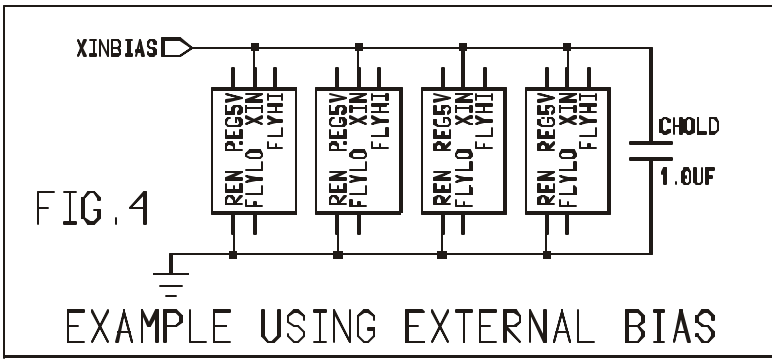


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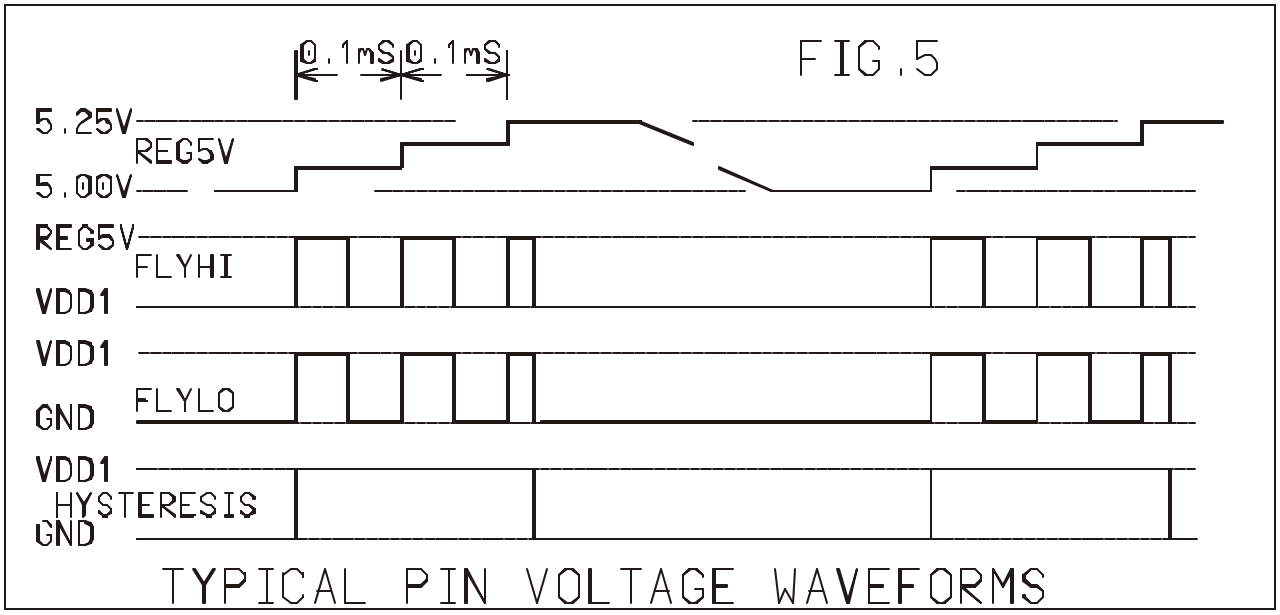
FIGURE 5 - TYPICAL PIN VOLTAGE WAVEFORMS



HREF Bias Generator

The output stage requires a reference supply 3.8 to 4.2 volts lower than PV4 into each HIN input. This may be provided by the system designer or generated on-chip. When HEN is held high, a bias voltage is generated at the HREF output which is (PV4-4.0v). This generated voltage may then be used to supply 6 HIN inputs. The HREF output must be stabilized by connecting a 0.1uF capacitor between HREF and PV4. A separate stabilizing capacitor is required for each HREF used. It is forbidden to connect any HREF pin to another HREF pin. Each enabled HREF output causes an additional DC current of 60uA (130 uA maximum) to flow from PV4 to MV4.

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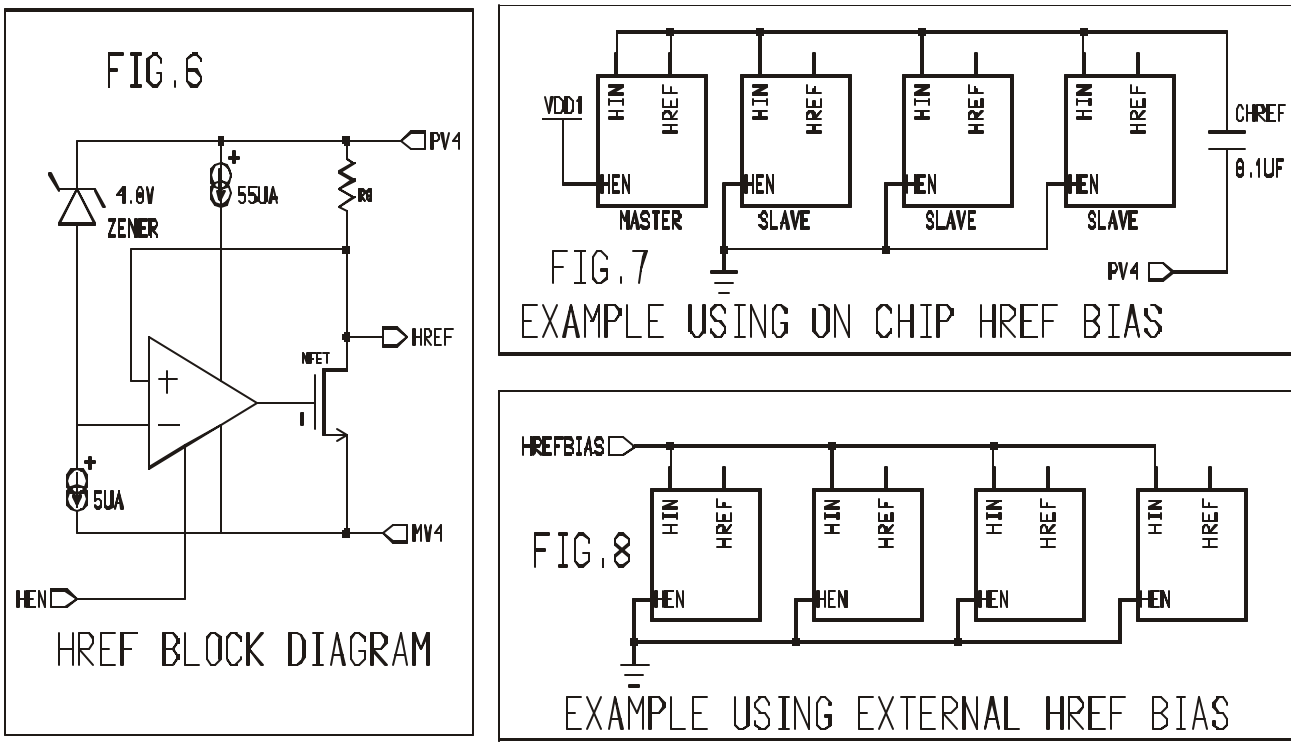
FIGURE 6 - HREF BLOCK DIAGRAM

FIGURE 7 - EXAMPLE USING ON CHIP HREF BIAS

FIGURE 8 - EXAMPLE USING EXTERNAL HREF BIAS



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Data Input Procedure

A data synchronization bit is entered into the TOKEN bit shift register via the SRIN (or SLIN) on a rising edge of SCLK. The token bit travels along the complete shift register path in order to control data latching. The internal logic is shown below. Notice the use of the SCLK divider. SCLK frequency is halved inside the IC to keep the current consumption to a minimum. The shift logic modifies the input signals in a manner that requires input data (DAT5:0) to follow the SRIN synchronization bit by 2 SCLK rising edges. Initialization of the system is accomplished via the RB input pin. The 6-bit data word is passed through the output register when pin LAT is LOW. When pin LAT is HIGH data is latched in the output storage register.

The inputs SHR and SEL200 are set by the user to control SHift-Right (versus shift left) operation and SELect 200 output configuration (versus 192 output configuration.). When SEL200 is LOW the user ignores the output pads near the edge of the die. That is, ignore outputs O0-O3 and O196-O199, use only outputs O4-O195. When SHR is HIGH data is loaded first into the lower number outputs first and completes the load at the higher numbered outputs. For example, with SHR high and SEL200 low the input data will load into register O4 first and complete the cycle by loading O195 on the last clock edge.

FIGURE 9 - INTERNAL LOGIC DETAILS FOR DATA PATH

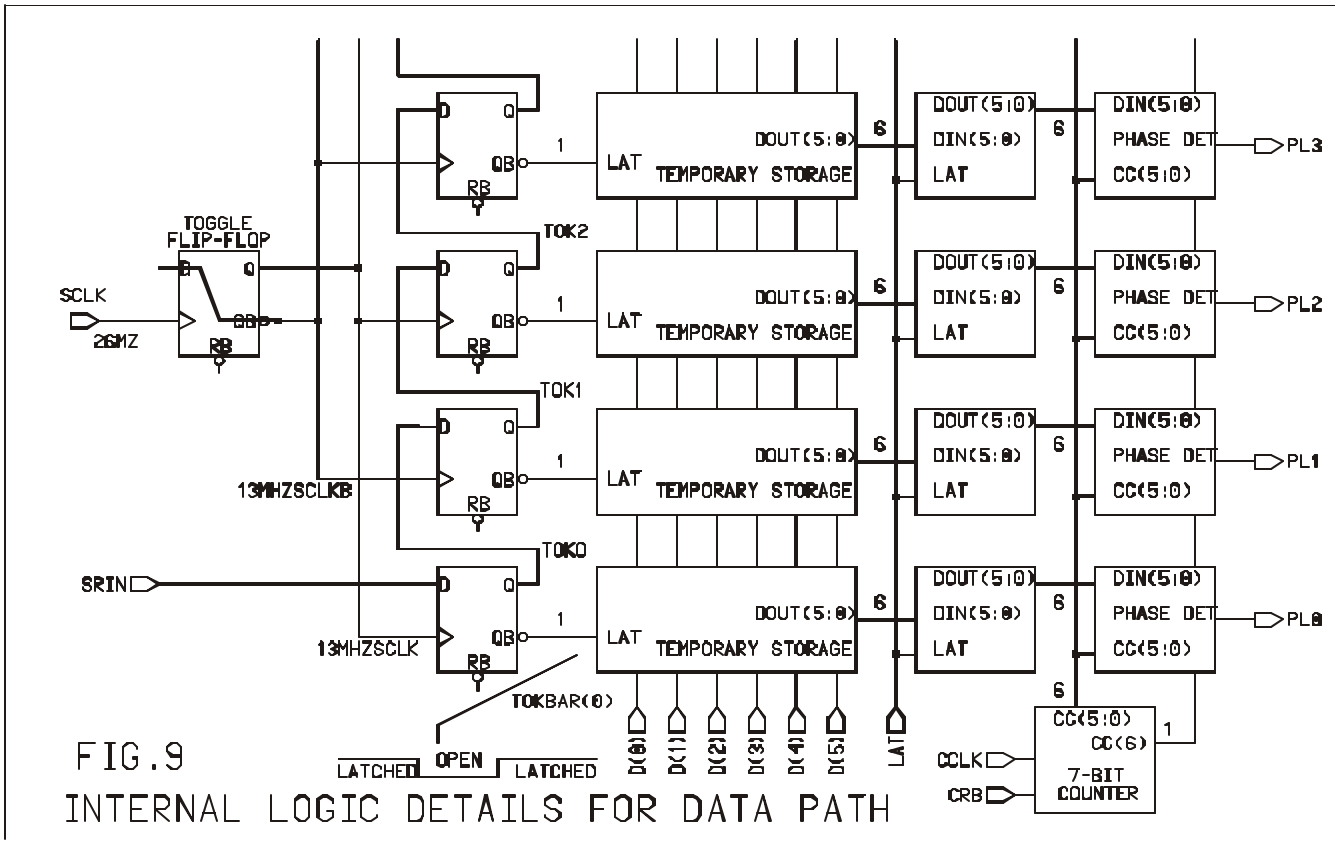
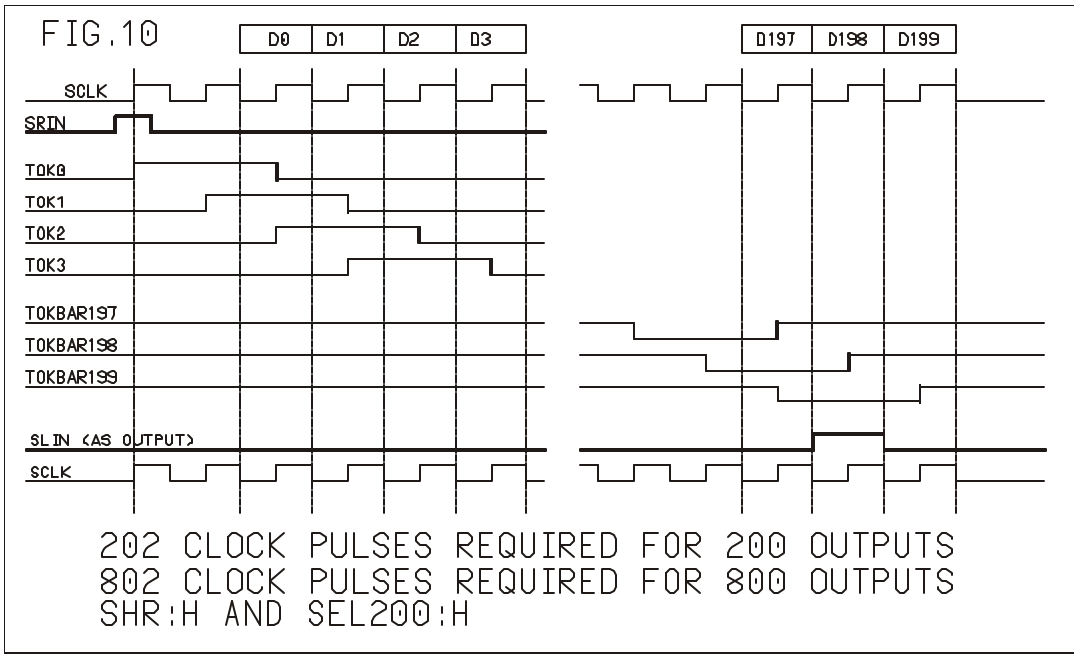
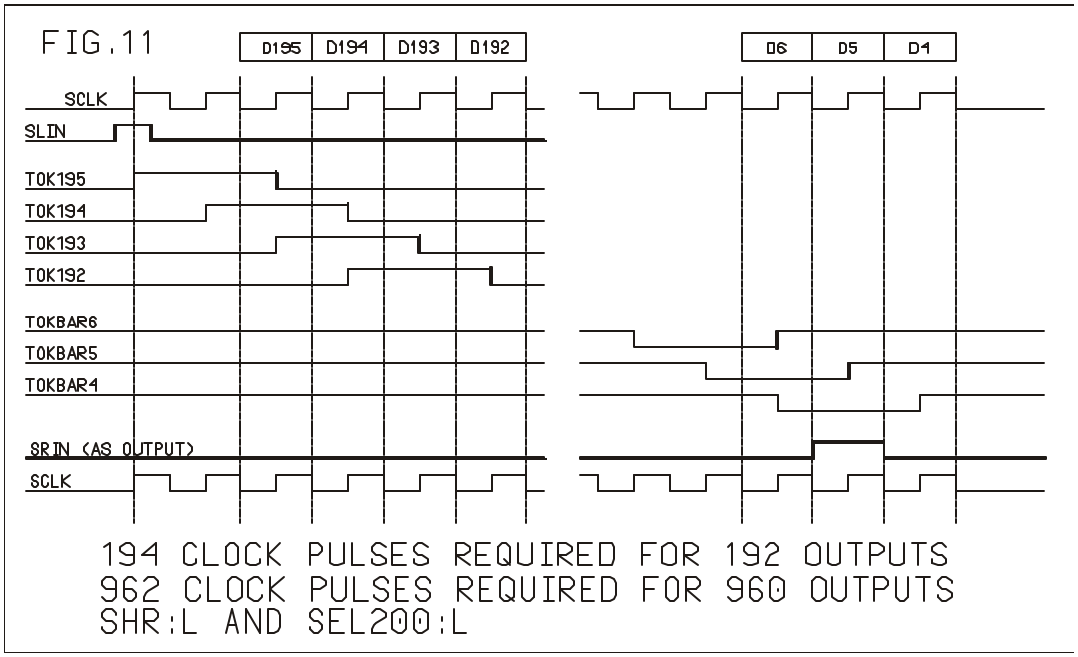


FIG.9
INTERNAL LOGIC DETAILS FOR DATA PATH

FIGURE 10 -

FIGURE 11 -





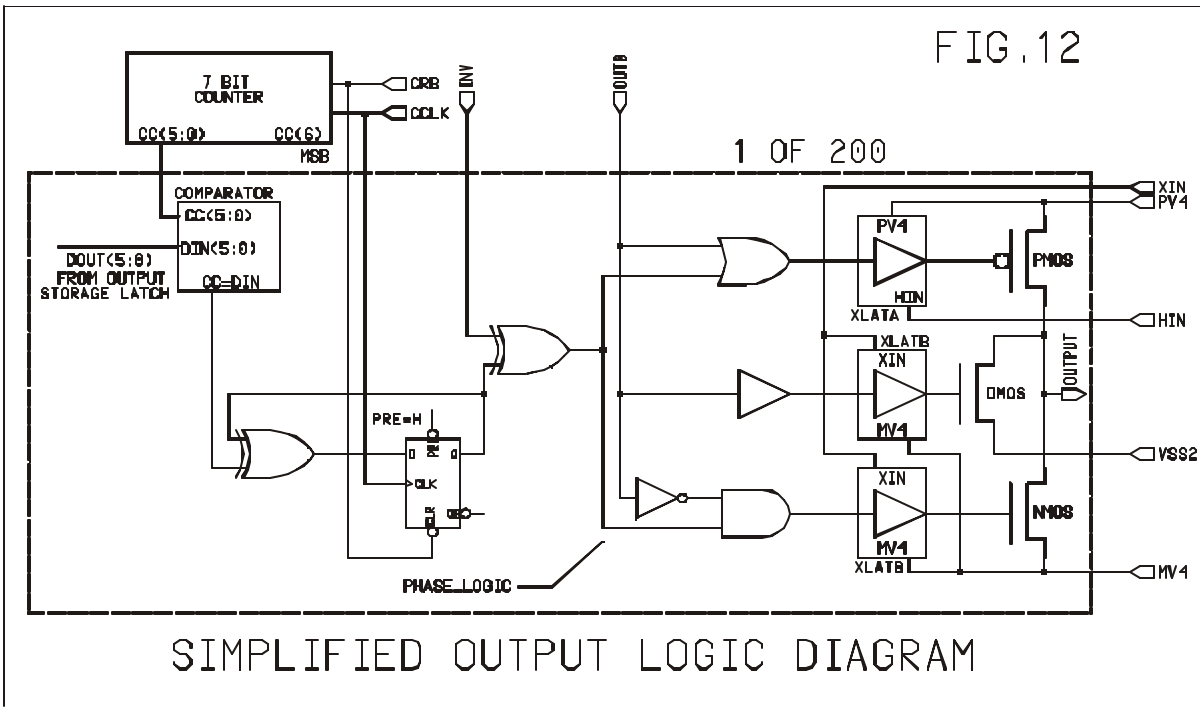
Phase Logic and Out0

The circuit has a 7-bit counter that is reset in a synchronous manner via the CRB (Counter-Reset-Bar) and CCLK (Counter CLK) pins. The counter is “preset” to zero if the CRB pin is low when the CCLK pin rises.

Each phase detector output is a 128 CCLK event. The INV pin will be assumed low for the purpose of this discussion. Upon reset (via CRB) the output will be low. The output is always guaranteed to be high continuously for 64 units of the 128 CCLK event. The output is also guaranteed to be low for 64 units of the 128 CCLK events, however, not usually continuously. The input data indicates which event should be completed in order to allow the data to go high. For example, an input data word of zero will cause the output to be low until the first rising edge of CCLK, then high for the subsequent 64 rising edges, then low again for the final 63 clocks. Notice that the output is always initially low for at least one CCLK period. A fifty percent (50%) duty cycle is attained when 63 (2F-HEX) is the input data; resulting in 64 units of low followed by 64 units of high.

The INV pin may invert the output from the above discussion. Pin INV must be high in order to produce a 64 unit high followed by a 64 unit low pulse train. The OUT0 (OUTput ZERO) pin will always command all outputs to zero volts potential (via the VSS2 input) irrespective of the individual states of CCLK, CRB or data stored in the output storage register.

FIGURE 12 - SIMPLIFIED OUTPUT LOGIC DIAGRAM



FIGURES 13 - 15 - PHASE DETECTOR WAVEFORM EXAMPLES

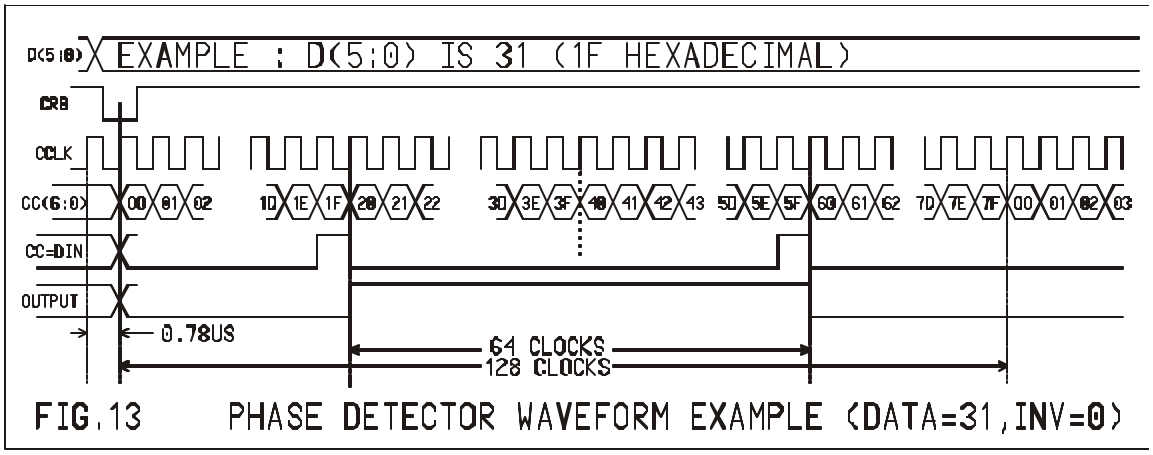


FIG.13 PHASE DETECTOR WAVEFORM EXAMPLE (DATA=31,INV=0)

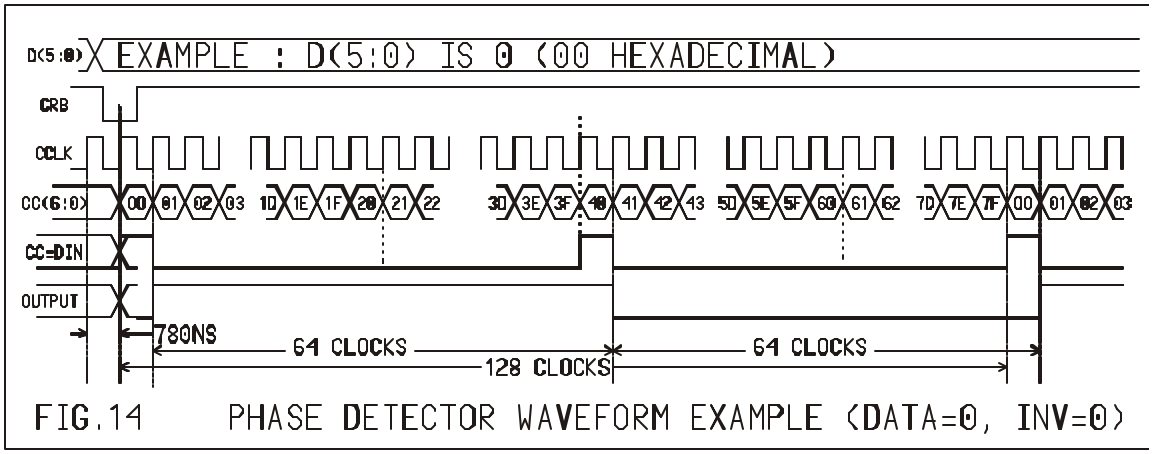


FIG.14 PHASE DETECTOR WAVEFORM EXAMPLE (DATA=0, INV=0)

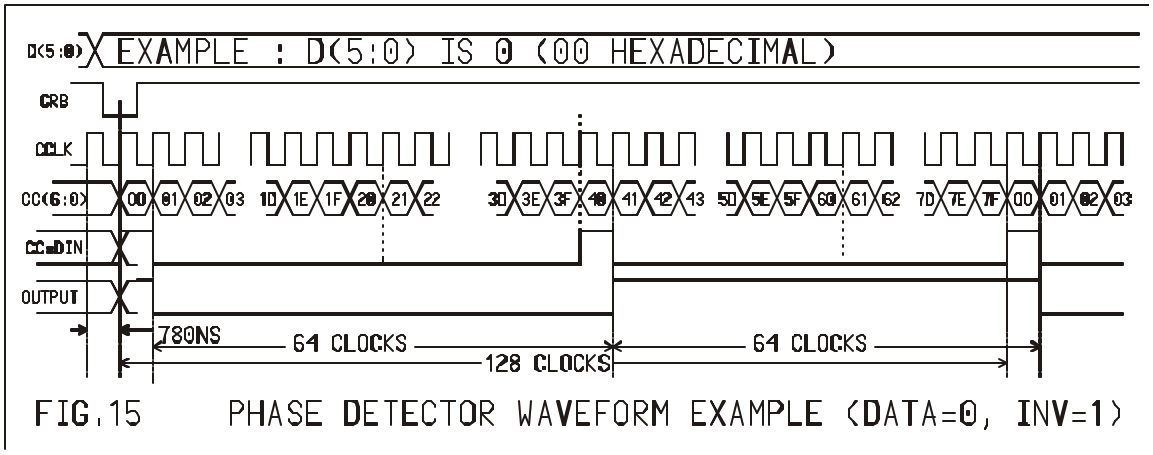


FIG.15 PHASE DETECTOR WAVEFORM EXAMPLE (DATA=0, INV=1)

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max.	Unit	Condition
Logic supply current	IVDD1		0.01 2.6 6.6 10.0	mA	Vdd=2.5V Sclk=0MHz Vdd=2.5V Sclk=26MHz Vdd=3.3V Sclk=50MHz Vdd=5.0V Sclk=50MHz
IDD1 due to REG5V ckt	IDDREG		130	uA	REN=H (no XIN load)
PV4 supply current (DC)	IPV4DC1		60	uA	HEN:L
PV4 supply current (DC)	IMV4DC2		150	uA	HEN:H
XIN supply current (DC)	IXINDC		20	uA	
MV4 supply current (DC)	IPV4DC1	-60		uA	HEN:L
MV4 supply current(DC)	IPV4DC2	-170		uA	HEN:H
PV4 supply current(AC)	IPV4AC		300	uA	CCLK=2.5MHz
XIN current(AC)	IXINAC		300	uA	CCLK=2.5MHz
MV4 supply current(AC)	IMV4AC	-450		uA	CCLK=2.5MHz
Logic input high voltage	VIH	VDD1-0.3		V	
Logic input low voltage	VIL		0.3	V	
Logic output high voltage	VOH	VDD1-0.5		V	IOH=1mA
Logic output low voltage	VOL		0.5	V	IOL=-1mA
Logic input current high level	IIH	3	3	uA	Vinput=VDD1
Logic input current low level	IIL	-3	-3	uA	Vinput=0V
Output voltage high	VOH	+V4-0.02V			Iload=0
Output voltage zero	VOO	-0.020V	0.020V		Iload=0
Output voltage low	VOL		PV4+- 0.02V		Iload=0

DC ELECTRICAL CHARACTERISTICS (CONT.)

Parameter	Symbol	Min	Max.	Unit	Condition
REG5V fanout	RFO		18		XIN loads
HREF fanout	HFO		8		HIN loads
Output switch impedance high	ZOH (1)	PV4-0.2V			Iload=-0.2mA (1)
Output switch impedance zero	ZOO (1)	-0.20V	0.20V		-0.2mA>Iload>0.2mA (1)
Output switch impedance low	ZOL (1)		MV4+-0.2V		Iload=0.2mA (1)
Output switch current high	IOH	4		mA	PV4=7,Vout=-7V
Output switch current sink	IOOL4		-4	mA	Vout=4.0V, OUT0=H
Output switch current source	IOOH4	4		mA	Vout=-4.0V,OUT0=H
Output switch current sink	IOOL2		-2	mA	Vout=2.0V, OUT0=H
Output switch current source	IOOH4	2		mA	Vout=-2.0V,OUT0=H
Output switch current low	IOL		-4	mA	MV4=-7,Vout=+7V

(1) PV4 = 2V, MV4 = -2V

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	VDD1=>2.5V	VDD1>3.2V	Unit
SCLK min pulse width high	TSPWH	15	8	nS
SCLK min pulse width low	TSPWL	15	8	nS
SCLK data setup time	TSS	15	8	nS
SCLK data hold time	TSH	15	8	nS
CCLK min pulse width high	TCPWH	50	25	nS
CCLK min pulse width low	TCPWL	50	25	nS
CCLK -CRB setup time	TCS	25	12	nS
CCLK -CRB hold time	TCH	25	12	nS
LAT min pulse width high	TLPWH	50	25	nS
LAT min pulse width low	TLPWL	50	25	nS
LAT fall after SCLK rise time	TSS	50	25	nS
LAT rise before SCLK rise time	TSH	50	25	nS

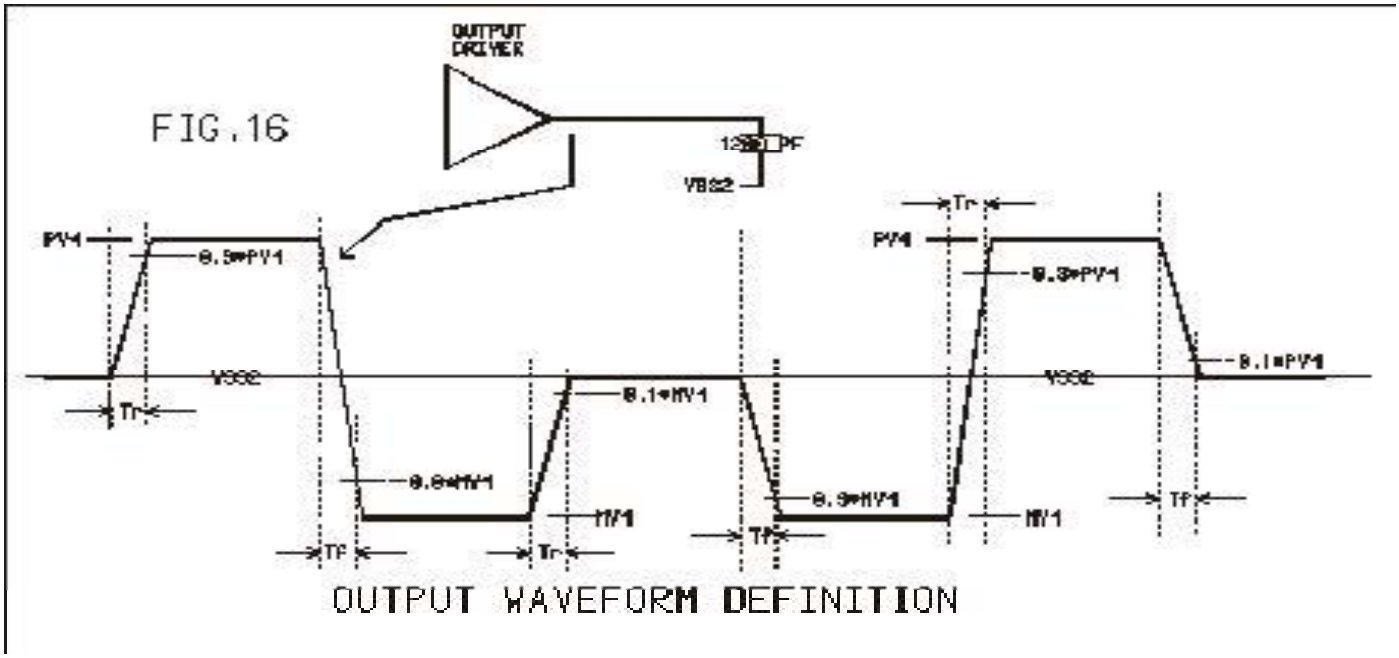
COLUMN DRIVER IC DESIGNATION TABLE

Symbol Name	I/O	Designation	Function
O0 to O199	O	Column Drive Output	-
OUT0	I	Output Gate (Asynchronous)	H:Vss2 , L:PV4,MV4
CRB	I	Counter Clear Signal(synchronous)	L & CCLK Rising Edge: Counter Clear H: Counter Enable L: disable
CCLK	I	Pulse Phase Shifter Counter Clock	Rising Edge : Count, Max 4MHz
INV	I	Phase Shift Data Invert Signal	L: Normal ,H: Invert (see Fig 14&15)
LAT	I	Phase Shift Data Latch Strobe	H : Latched, L: Transparent
D[5:0]	I	Phase Shift Data	D(5) : MSB, D(0):LSB
SCLK	I	Token Shift Clock	Data entered on Rising Edges
SHR	I	Data Shift Direction	H: Shift Right, Input is SRIN L: Shift Left, Input is SLIN
SEL200	I	Data Output Select 200 or 192	H: SRIN to O000, (SHR:H) L: SRIN to O004, (SHR:H)
VDD1	-	Power Supply For Logic System	2.5 To 5.5V
VSS1	-	Logic Ground	0V
PV4	-	Power Supply For LC Drive	7 to 2V
MV4	-	Power Supply For LC Drive	-7 to -2V
SRIN	I/O	Data Synchronization bit	Input for SHR:H, Output for SHR:L
SLIN	I/O	Data synchronization bit	Input for SHR:L, Output for SHR:H
HIN	I	High Reference input	(PV4-4.0V) (see HREF/HIN also)
HEN	I	HREF source enable signal	L: HREF not used , H: Enable HREF
HREF	O	High Reference Output	(PV4-4.0V)Reference output
REN	I	Regulator Enable Input	Enable:H, Disable:L
FLYHI	-	Voltage Regulator flying capacitor.	0.1uF cap to FLYLO when REN:H No connect when REN:L
FLYLO	-	Voltage Regulator flying capacitor.	0.1uF cap to FLYHI when REN:H No connect when REN:L
REG5V	O	Regulated 5 volt output	1.0uF cap to VSS1 When REN:H
XIN	I	Translator input bias reference	Bias between +5.0V to +11.0V
VSS2	-	Output Driver Ground	0V
RB	I	Master Reset	Reset :L , Normal:H

TABLE 6 - AC CHARACTERISTICS (See Fig. 16)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Shift Clk Frequency				26	MHz	VDD1 = 2.5V
Count Clk Frequency				4	MHz	VDD1=2.5V
Rising Time	Tr		-	5	us	SEE FIG. 16
Falling Time	Tf		-	5	us	SEE FIG. 16
PV4 Driver Equivalent output resistance	PV4Ron			1.0	Kohm	Iout=200uA
MV4 Driver Equivalent output resistance	MV4Ron			1.0	Kohm	Iout=200uA
PV4,MV4 Pulse Width	TPV4,TMV4	25			us	See Section 8
Output Delay Time		-	-	1	us	TBD

FIGURE 16 - OUTPUT WAVEFORM DEFINITION



MECHANICAL SPECIFICATIONS

DIE SPECIFICATIONS

Die Dimensions:		
"X" Dimension	12830 µm	Measured from center of scribe to center of scribe
"Y" Dimension	1760 µm	Measured from center of scribe to center of scribe
Thickness	635 µm (nominal)	Unthinned (non-back lapped wafer)
Gold Bump Height	15±3 µm	

Die Materials:	
Passivation	Silicon Nitride (SiN)
Gold Bump Hardness	45-75 HV
Wafer	Silicon (Si)

Note: The active surface is sensitive to light. Cover with an opaque material after assembly.

COORDINATES RELATIVE TO ORIGIN (0, 0) AT MINIMUM PAD CENTER LOCATION

Corners of Scribe Centers

Lower Left: X = -115µm, Y = -205µm

Upper Right: X = 12715µm, Y = 1555µm

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FIGURE 17 - DIE DIMENSIONAL DRAWING

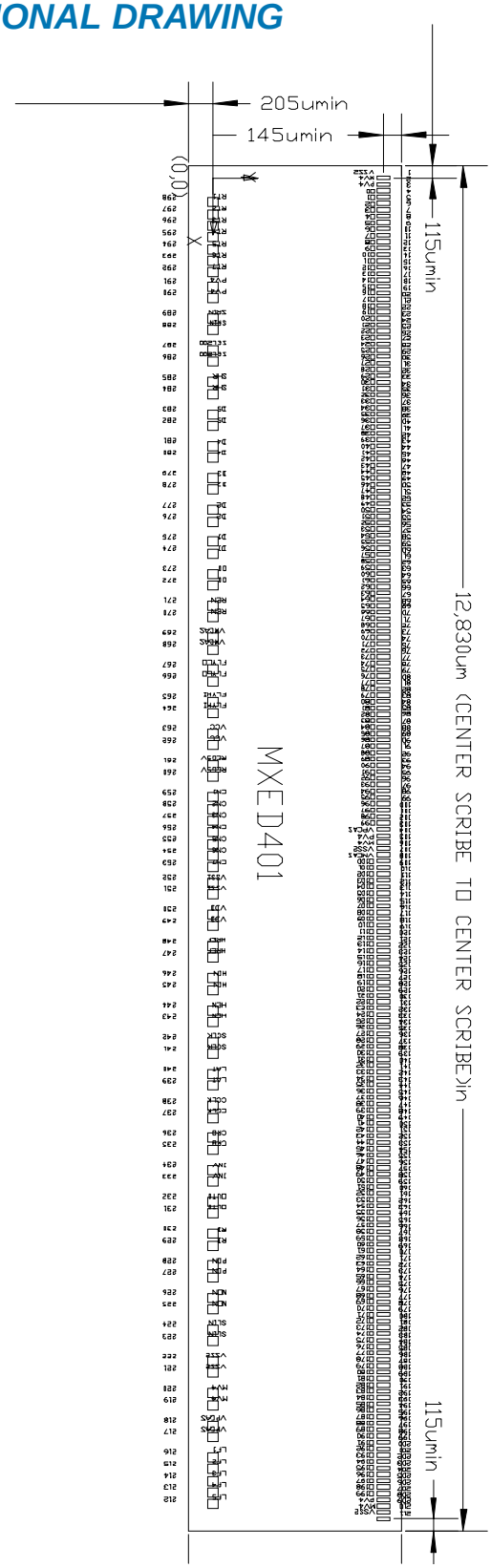

TABLE 4 - TRUTH TABLE (TOKEN BIT SHIFT REGISTER)

INPUT			Input-Output		Data to clock synchronization
SHR	SCLK	SEL200	SRIN	SLIN	
H	Rising Edge	H	Input	Output	D(5:0) sequence O0,O1…O198,O199
H	Rising Edge	L	Input	Output	D(5:0) sequence O4,O5…O194,O195
L	Rising Edge	H	Output	Input	D(5:0) sequence O199,O198…O1,O0
L	Rising Edge	L	Output	Input	D(5:0) sequence O195,O194…O5,O4

TABLE 5 - TRUTH TABLE (DATA LATCH)

LAT	CONDITION
H	Latched
L	Open (Transparent)

ORDERING INFORMATION

MXED401

Ordering Part Number	Package
14501-00	Gold Bumped Die in Waffle Trays
14526-00	Gold Bumped Die in Wafer Form
14535-00	TCP (Tape Carrier Package) please consult factory
14539-00	BGA (typically for prototyping only)

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