application INFO available

High Speed Power Driver

FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both Vs and Vc can independently range from 5V to 40V. For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

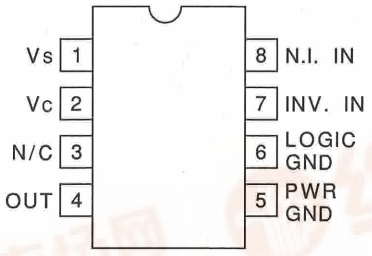
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

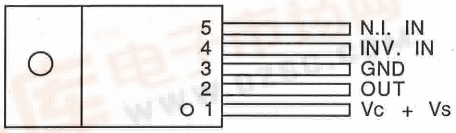
$\overline{OUT} = \overline{INV}$ and N.I.
$\overline{OUT}$ = INV or N.I.

CONNECTION DIAGRAMS

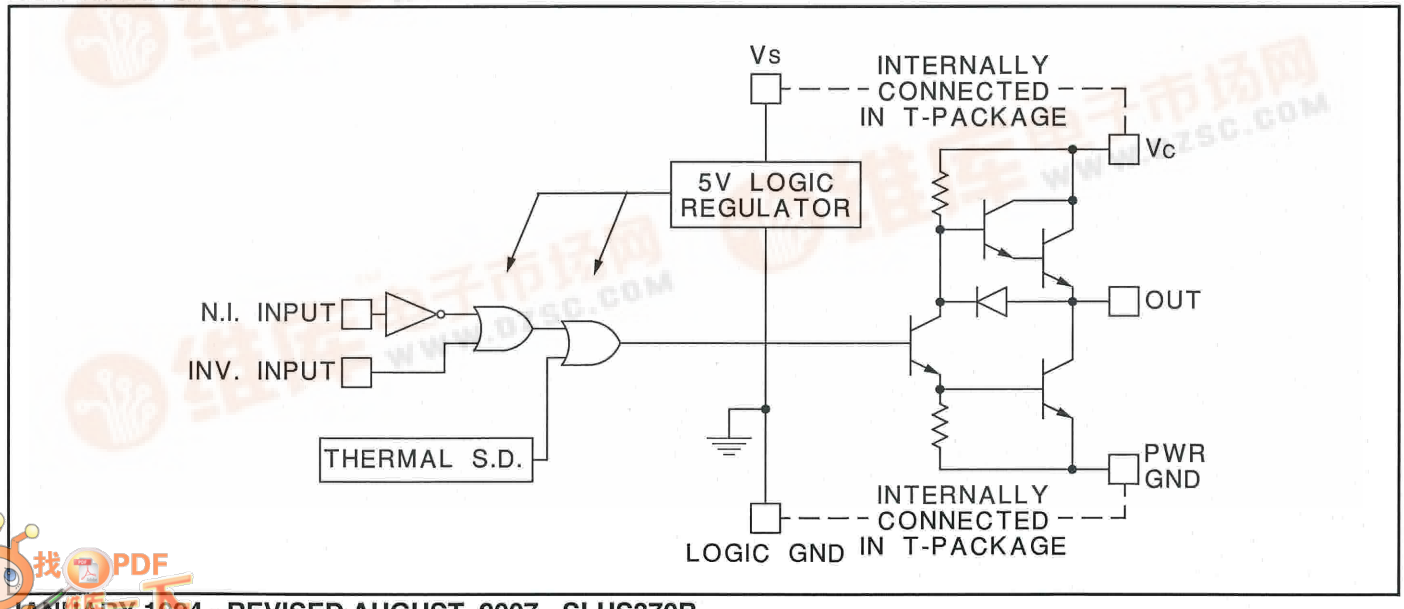
DIL-8 MINIDIP, SOIC-8
(TOP VIEW)
N or JG Package, D Package



5-PIN TO-220
(TOP VIEW)
T Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	N-Pkg	JG-Pkg	T-Pkg
Supply Voltage, V_{IN}	40V	40V	40V
Collector Supply Voltage, V_C	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1.0A
Peak Transient	±1.5A	±1.0A	±2.0A
Capacitive Discharge Energy	20µJ	15µJ	50µJ
Digital Inputs (See Note)	5.5V	5.5V	5.5V
Power Dissipation at T_A = 25°C (See Note)	1W	1W	3W
Power Dissipation at T_A (Leads/Case) = 25°C (See Note)	3W	2W	25W
Operating Temperature Range	0°C to +70°C	-55°C to +125°C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Note: All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1705, -25°C to +85°C for the UC2705, and 0°C to +70°C for the UC3705; $V_S = V_C$ = 20V, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Vs Supply Current	Vs = 40V, (Outputs High, T Pkg)		6	8	mA
	Vs = 40V, (Outputs Low, T Pkg)		8	12	mA
Vc Supply Current (N, JG Only)	Vc = 40V, Outputs Low		2	4	mA
Vc Leakage Current (N, JG Only)	Vs = 0, Vc = 30V		0.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.05	0.1	mA
Output High Sat., Vc-Vo	Io = -50mA			2.0	V
	Io = -500mA			2.5	V
Output Low Sat., Vo	Io = 50mA			0.4	V
	Io = 500mA			2.5	V
Thermal Shutdown			155		°C

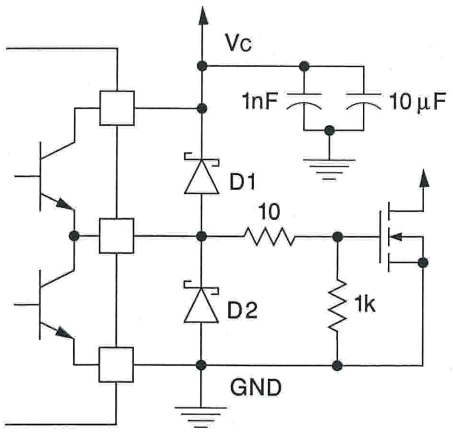
TYPICAL SWITCHING CHARACTERISTICS:

$V_S = V_C$ = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
Vc Cross-Conduction Current Spike Duration	Ouput Rise	25			ns
	Output Fall	0			ns

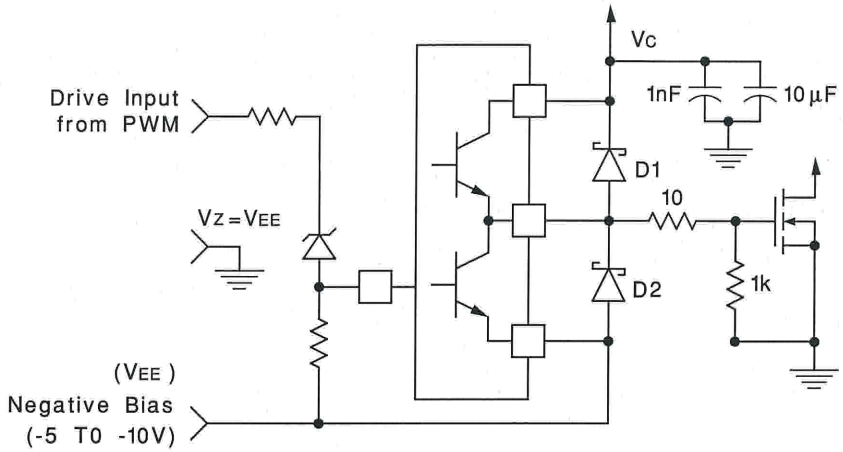
APPLICATIONS

Power MOSFET Drive Circuit



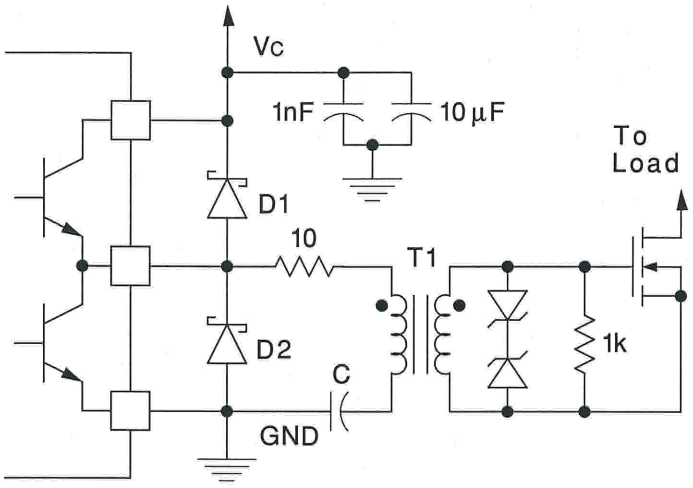
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.



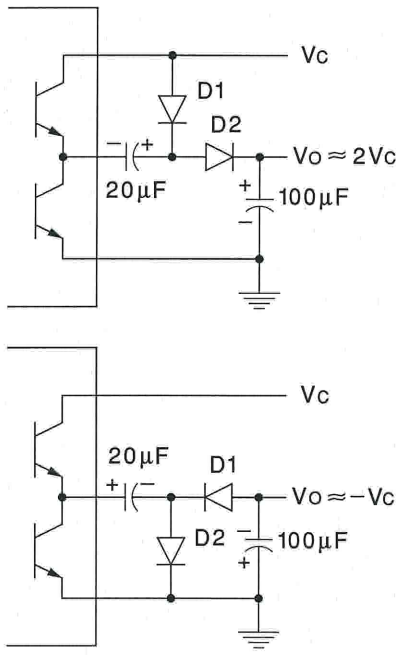
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9579801M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9579801MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-9579801VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1705J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1705J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1705L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2705NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC3705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3705NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3705T	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type
UC3705TG3	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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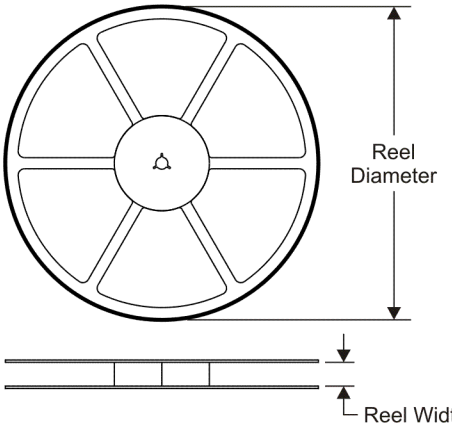
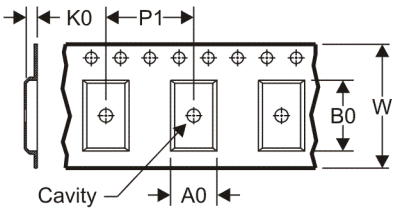
TAPE AND REEL INFORMATION

REEL DIMENSIONS

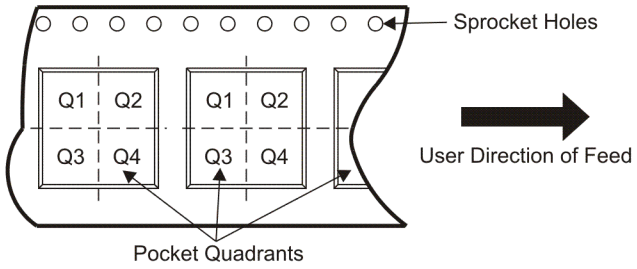


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

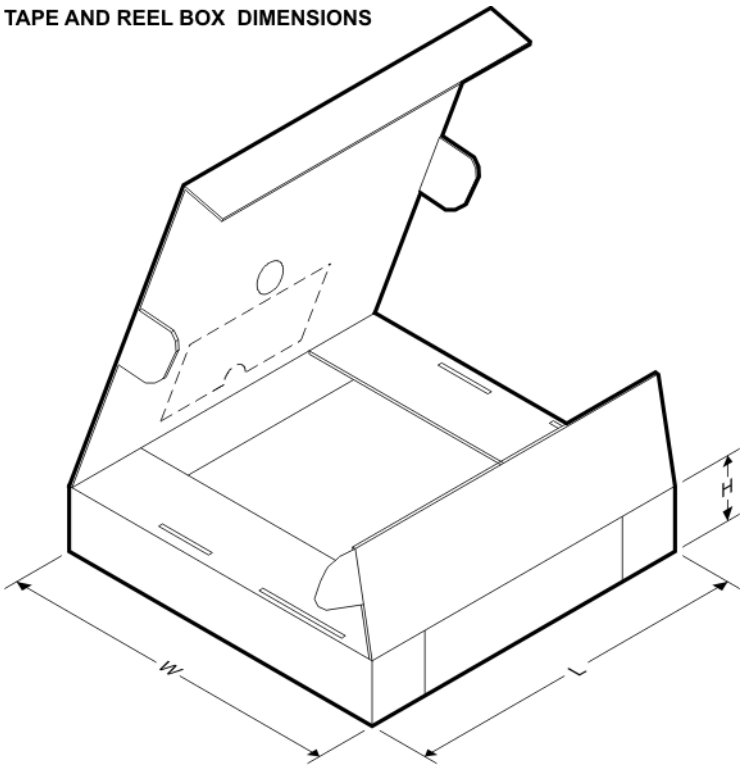


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

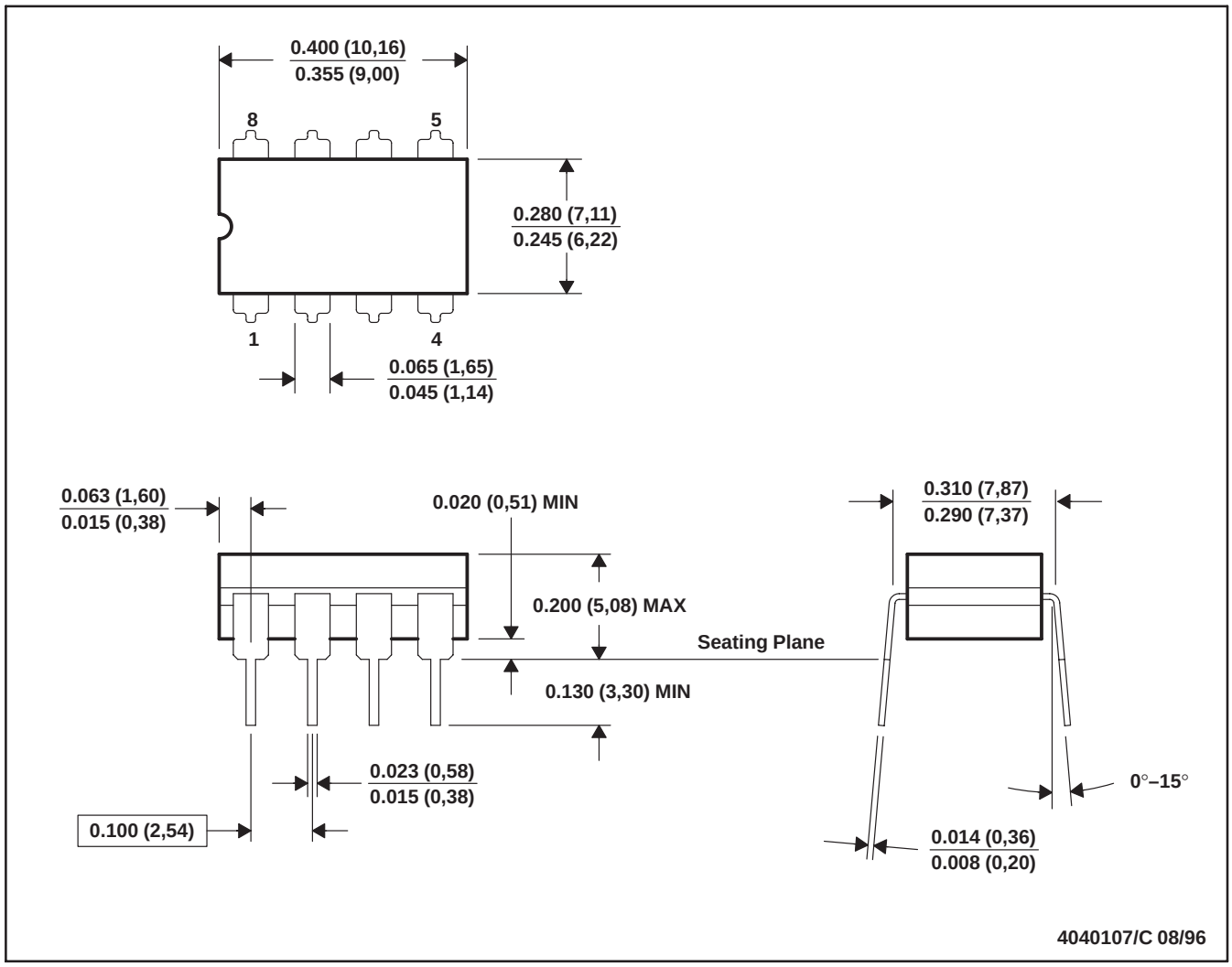
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3705DTR	SOIC	D	8	2500	346.0	346.0	29.0

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

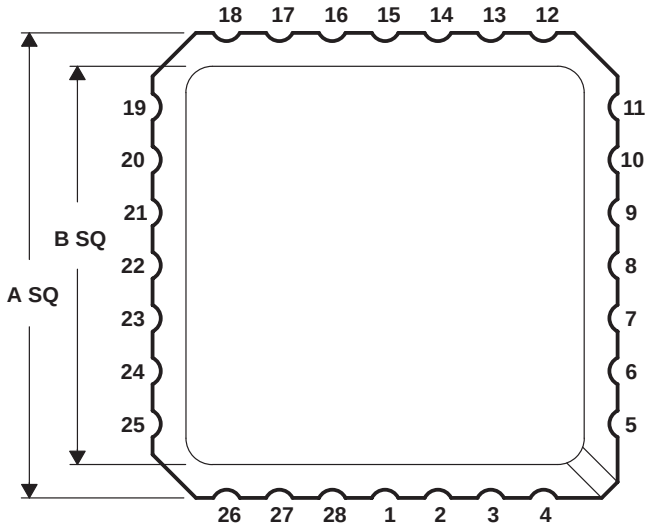


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

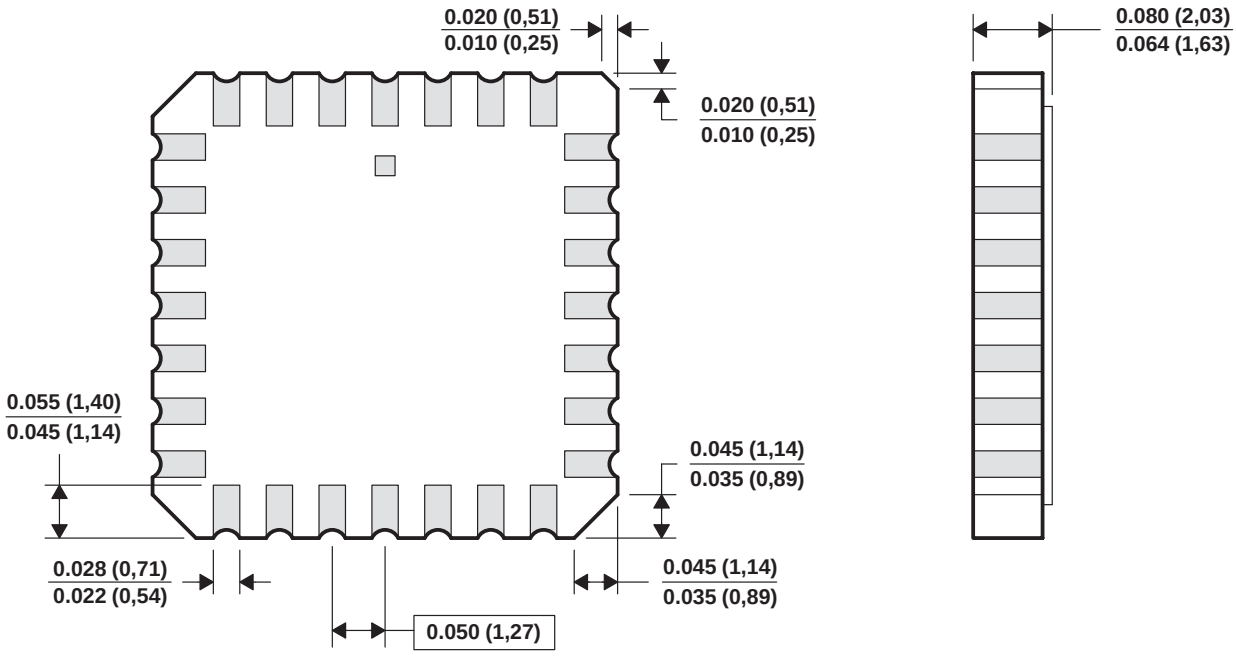
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



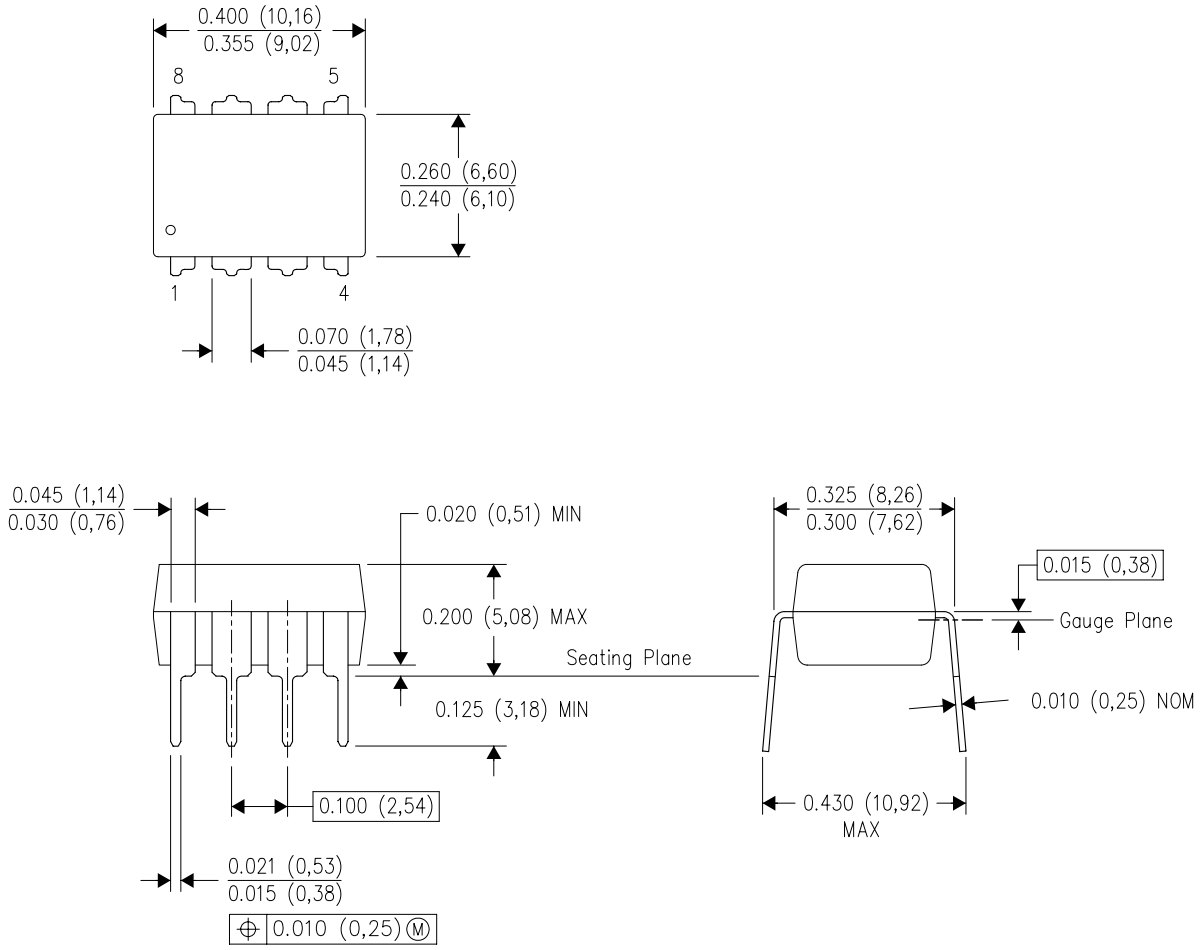
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

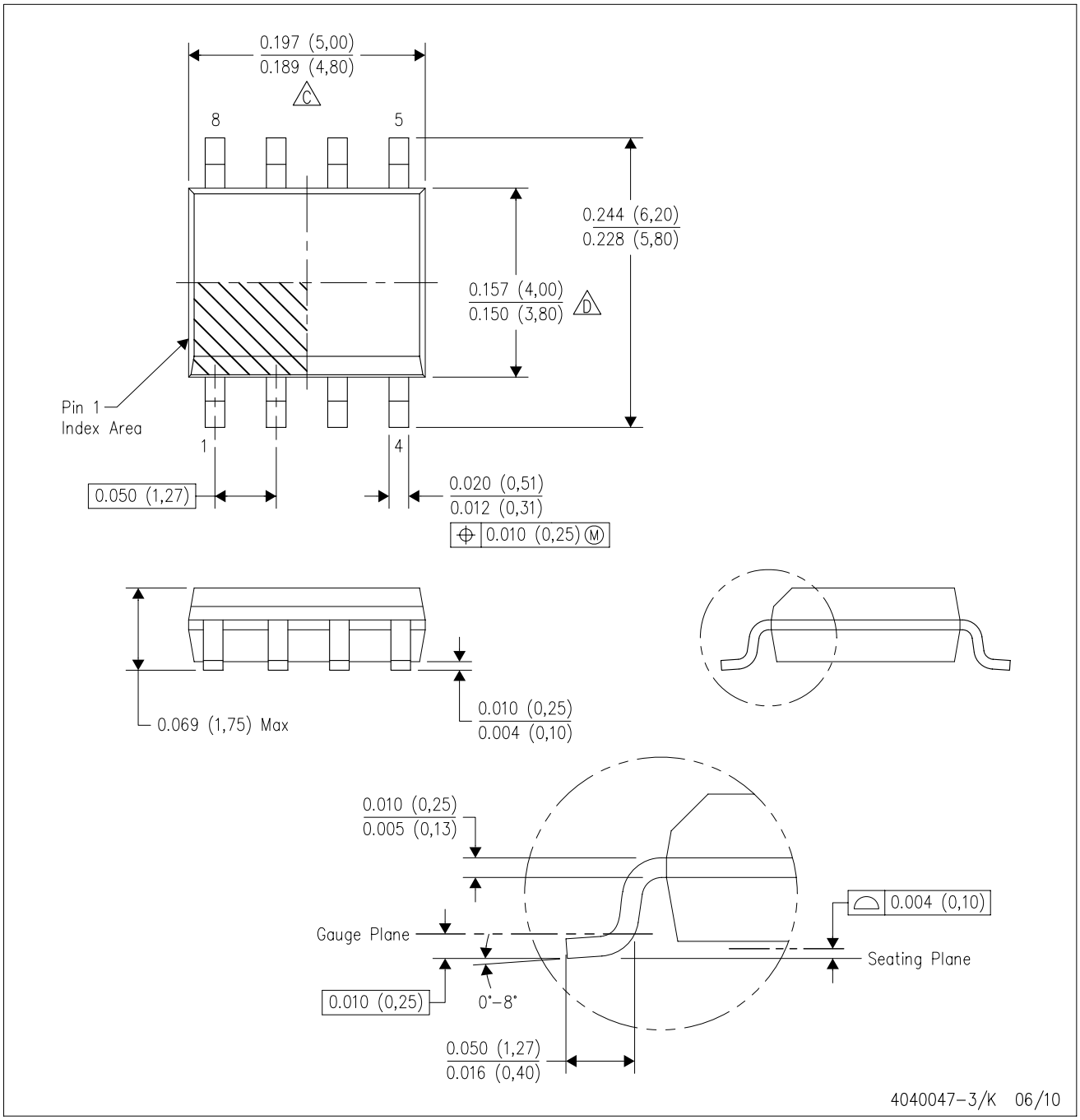
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



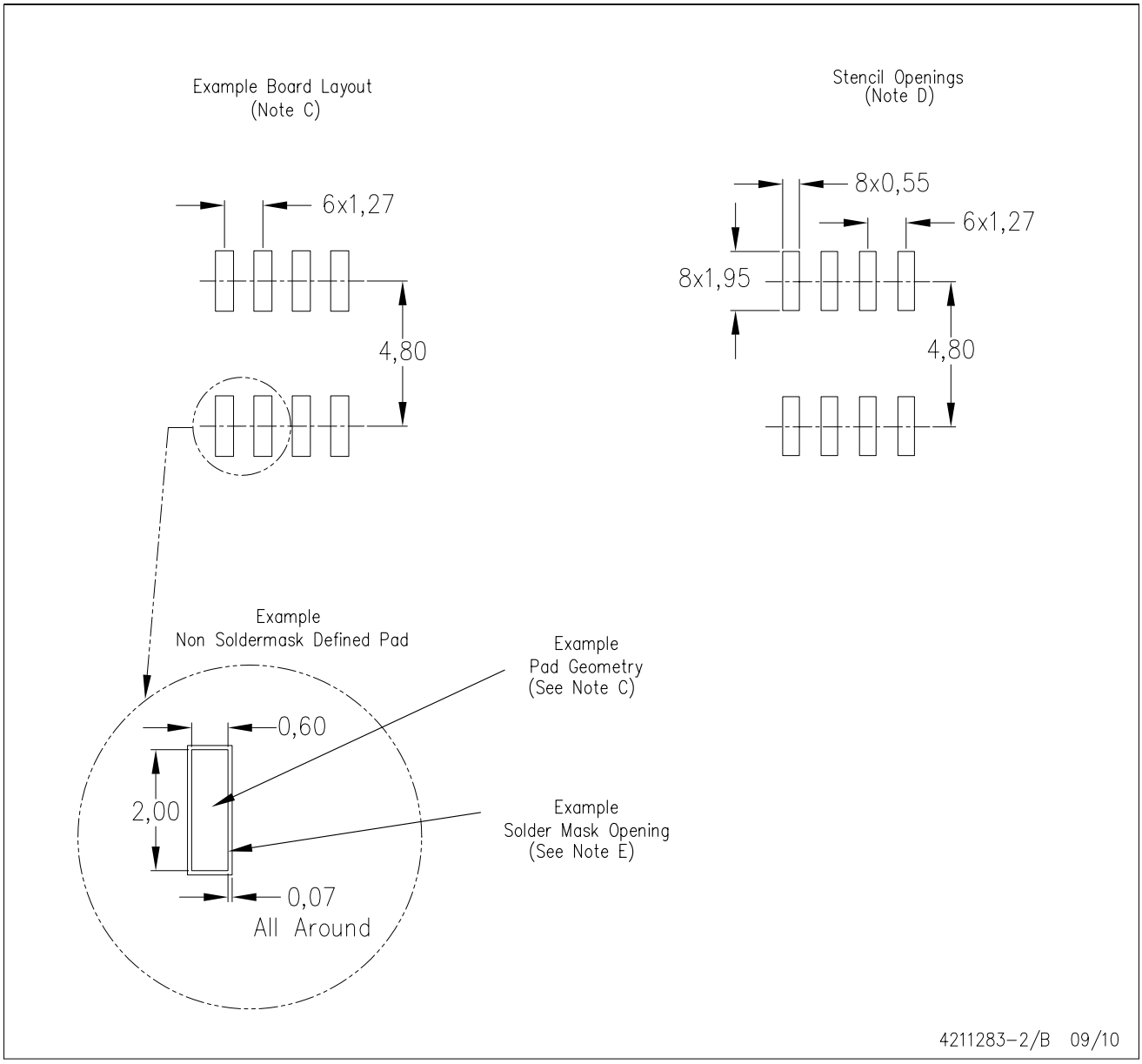
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



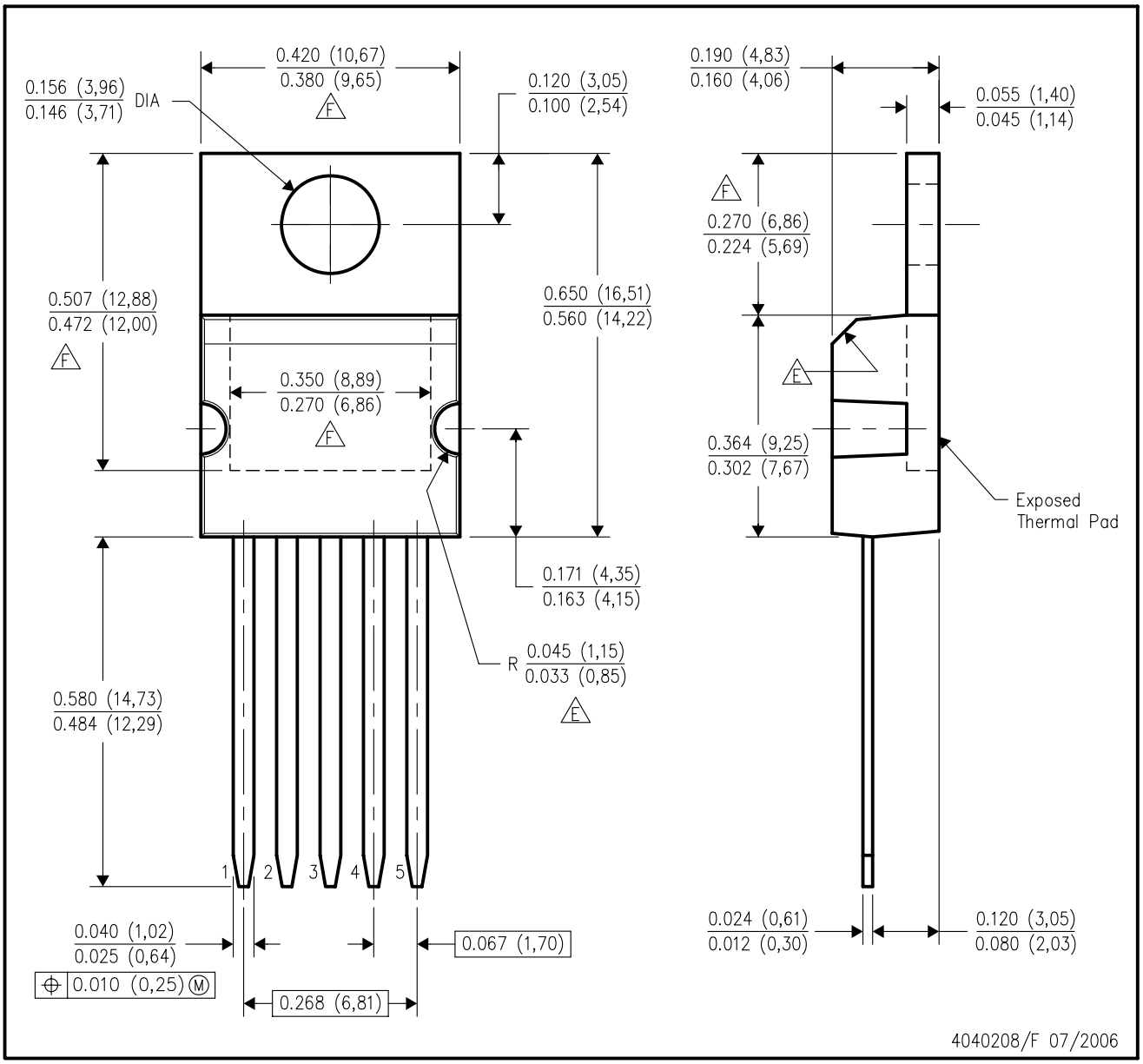
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

KC (R–PSFM–T5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. All lead dimensions apply before solder dip.
D. The center lead is in electrical contact with the mounting tab.
E. These features are optional.
F. Thermal pad contour optional within these dimensions.

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