

FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
 - **Extended Temperature Performance of –40°C to 85°C**
 - **Enhanced Diminishing Manufacturing Sources (DMS) Support**
 - **Enhanced Product Change Notification**
 - **Qualification Pedigree ⁽¹⁾**
 - **Member of the Texas Instruments Widebus+™ Family**
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated DIMM Load**
 - **Supports SSTL_2 Data Inputs**
 - **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
 - **Supports LVCMOS Switching Levels on the RESET Input**
 - **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
 - **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
 - **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTV32867-EP operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	CSSTV32867SGKEREP	S867EP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ is a trademark of Texas Instruments.

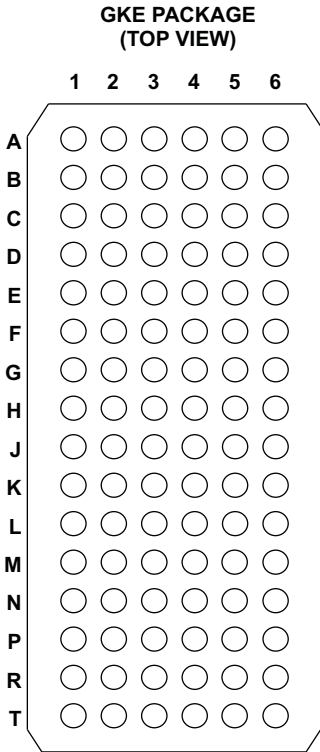
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006, Texas Instruments Incorporated



SN74SSTV32867-EP
26-BIT REGISTERED BUFFER
WITH SSTL_2 INPUTS AND LVCMOS OUTPUTS

SGS6641-SEPTEMBER 2008 查询"SN74SSTV32867-EP"供应商



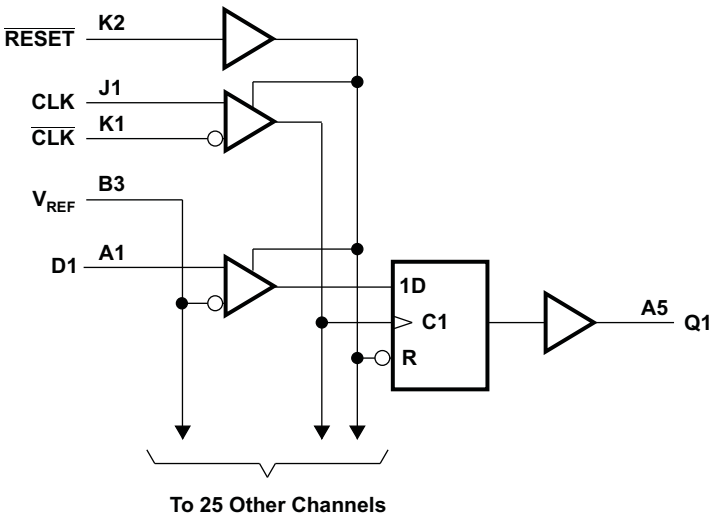
TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	D1	V _{CC}	GND	V _{DDQ}	Q1	Q2
B	D3	D2	V _{REF}	GND	Q3	Q4
C	D5	D4	NC	GND	Q5	Q6
D	D7	D6	GND	V _{DDQ}	Q7	Q8
E	D9	D8	V _{CC}	GND	Q9	V _{DDQ}
F	D11	D10	GND	V _{DDQ}	Q10	GND
G	D13	D12	V _{CC}	V _{DDQ}	Q12	Q11
H	D15	D14	GND	GND	GND	Q13
J	CLK	NC	GND	GND	GND	Q14
K	CLK	RESET	V _{CC}	V _{DDQ}	Q15	Q16
L	D16	D17	GND	V _{DDQ}	Q17	GND
M	D18	D19	V _{CC}	GND	Q18	V _{DDQ}
N	D20	D21	GND	V _{DDQ}	Q20	Q19
P	D22	D23	NC	GND	Q22	Q21
R	D24	D25	NC	GND	Q24	Q23
T	D26	V _{CC}	GND	V _{DDQ}	Q26	Q25

FUNCTION TABLE

INPUTS				OUTPUT Q
RESET	CLK	CLK	D	
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q ₀
L	X or floating	X or floating	X or floating	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} or V_{DDQ}	Supply voltage range	–0.5	3.6	V
V_I	Input voltage range ⁽²⁾	–0.5	$V_{CC} + 0.5$	V
V_O	Output voltage range ⁽²⁾⁽³⁾	–0.5	$V_{DDQ} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DDQ}$		±50 mA
I_O	Continuous output current	$V_O = 0$ to V_{DDQ}		±50 mA
	Continuous current through each V_{CC} , V_{DDQ} , or GND			±100 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			40 °C/W
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 3.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	2.3		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)	1.15	1.25	1.35	V
V_{TT}	Termination voltage	$V_{REF} - 40$ mV	V_{REF}	$V_{REF} + 40$ mV	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data input		$V_{REF} + 310$ mV	V
V_{IL}	AC low-level input voltage	Data input		$V_{REF} - 310$ mV	V
V_{IH}	DC high-level input voltage	Data input		$V_{REF} + 150$ mV	V
V_{IL}	DC low-level input voltage	Data input		$V_{REF} - 150$ mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$		1.7	V
V_{IL}	Low-level input voltage	$\overline{RESET}$		0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$		0.97	1.53 V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$		360	mV
I_{OH}	High-level output current			–8	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	–40		85	°C

- (1) The $\overline{RESET}$ input of the device must be held at V_{CC} or GND to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74SSTV32867-EP

26-BIT REGISTERED BUFFER

WITH SSTL_2 INPUTS AND LVCMOS OUTPUTS

SCS5684-SSTV32867-EP 2008 查询"SN74SSTV32867-EP"供应商

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}		I _I = -18 mA		2.3 V			-1.5	V
V _{OH}		I _{OH} = -100 µA		2.3 V to 2.7 V	V _{DDQ} - 0.2			V
		I _{OH} = -8 mA		2.3 V	1.7			
V _{OL}		I _{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I _{OL} = 8 mA		2.3 V			0.45	
I _I	All inputs	V _I = V _{CC} or GND		2.7 V			±5	µA
I _{CC}	Static standby	RESET = GND	I _O = 0	2.7 V			40	µA
	Static operating	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)}					95	mA
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching, 50% duty cycle	I _O = 0	2.5 V		44		µA/MHz
	Dynamic operating – per each data input	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK switching, 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				5		µA/clock MHz/ D input
C _I ⁽²⁾	Data inputs	V _I = V _{REF} ± 310 mV		2.5 V		3.5		pF
	CLK, CLK	V _{ICR} = 1.25 V, V _{I(PP)} = 360 mV				4.5		
	RESET	V _I = V _{CC} or GND				5		

(1) All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

(2) Measured with 50-MHz input frequency

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

				V _{CC} = 2.5 ± 0.2 V			UNIT
				MIN	TYP	MAX	
f _{clock}	Clock frequency					200	MHz
t _w	Pulse duration	CLK, CLK high or low		2.5			ns
t _{act}	Differential inputs active time ⁽¹⁾				22		ns
t _{inact}	Differential inputs inactive time ⁽²⁾				22		ns
t _{su}	Setup time	Fast slew rate ⁽³⁾⁽⁴⁾	Data before CLK↑, CLK↓	1.0			ns
		Slow slew rate ⁽⁴⁾⁽⁵⁾		1.5			
t _h	Hold time	Fast slew rate ⁽³⁾⁽⁴⁾	Data after CLK↑, CLK↓	1.0			ns
		Slow slew rate ⁽⁴⁾⁽⁵⁾		1.5			

(1) Data inputs must be low a minimum time of t_{act} min, after RESET is taken high.

(2) Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} min, after RESET is taken low.

(3) Data signal input slew rate ≥ 1 V/ns

(4) CLK, CLK input slew rates are ≥ 1 V/ns.

(5) Data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns

Switching Characteristics

over recommended operating free-air temperature range, $V_{REF} = V_{DDQ}/2$ and $C_L = 30$ pF (unless otherwise noted)
(see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CLK and $\overline{\text{CLK}}$	Q		5.5	ns
t_{PHL}	$\overline{\text{RESET}}$	Q		5.2	ns

PARAMETER MEASUREMENT INFORMATION

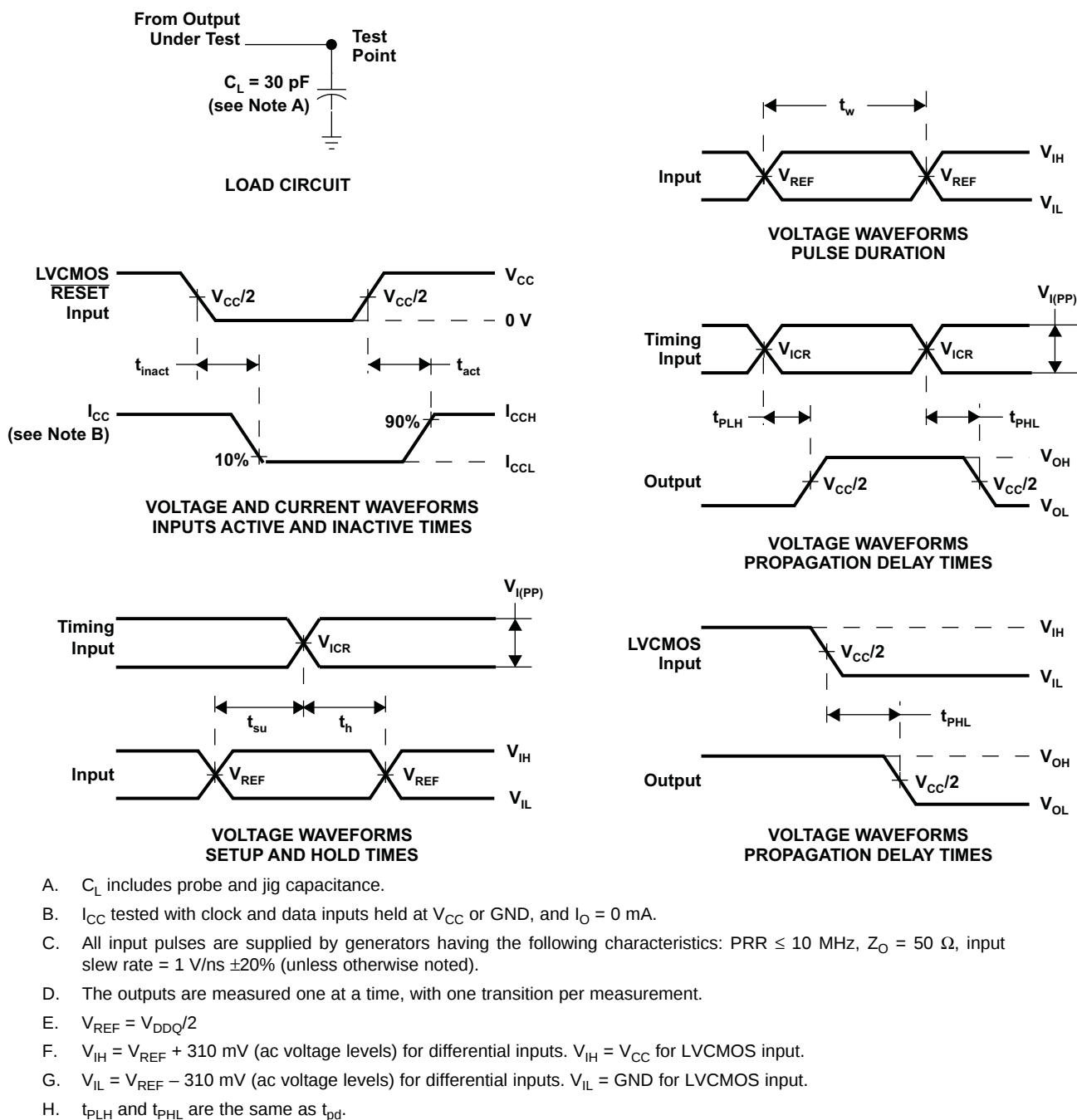


Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSSTV32867SGKEREP	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	N / A for Pkg Type
V62/06676-01XE	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

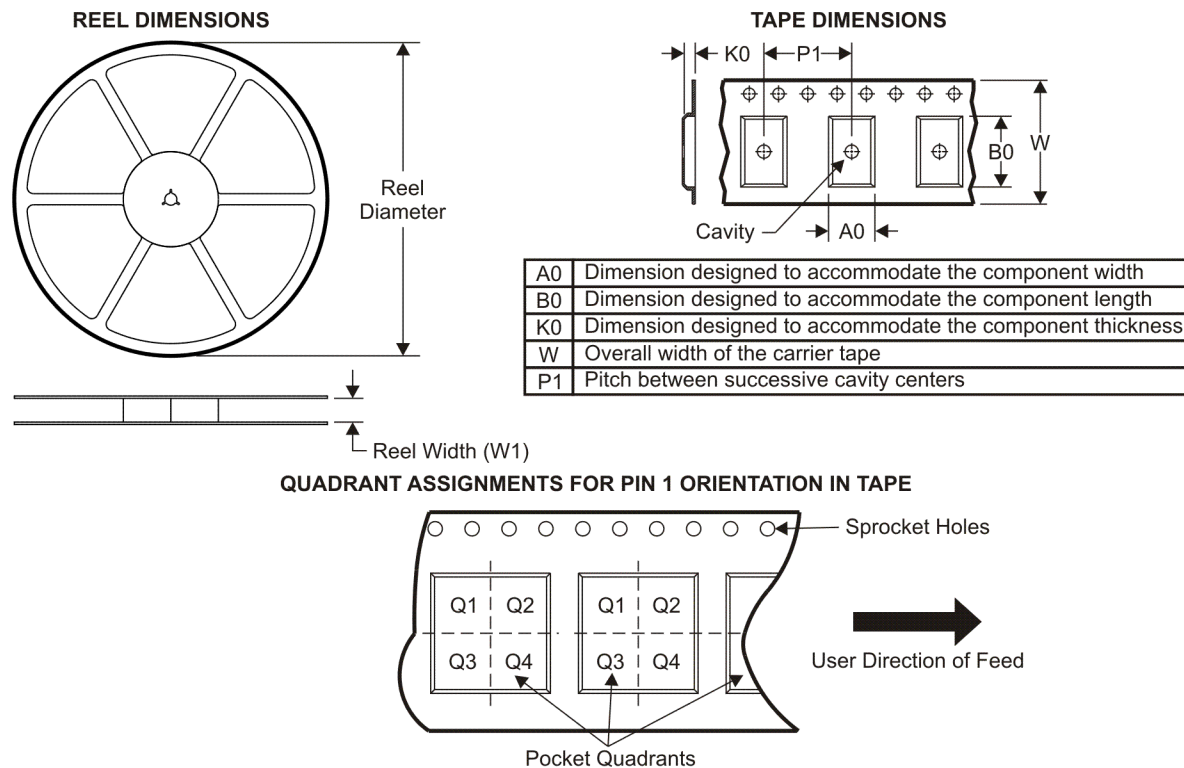
OTHER QUALIFIED VERSIONS OF SN74SSTV32867-EP :

- Catalog: [SN74SSTV32867](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSSTV32867SGKEREP	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

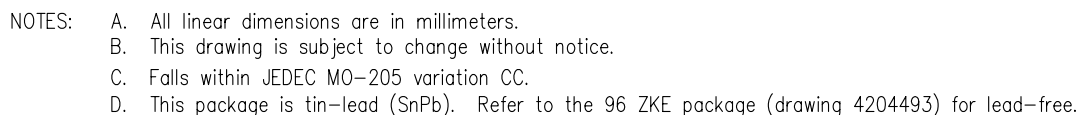
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSSTV32867SGKERE	LFBGA	GKE	96	1000	346.0	346.0	41.0

PLASTIC BALL GRID ARRAY



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless