

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance:
80 Ω (typ.) at $V_{CC} = 4.5$ V
70 Ω (typ.) at $V_{CC} = 6.0$ V
60 Ω (typ.) at $V_{CC} = 9.0$ V
typical "break before make" built-in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4067 are high-speed Si-gate CMOS devices and are pin compatible with the "4067" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4067 are 16-channel analog multiplexers/demultiplexers with four address inputs (S_0 to S_3), an active LOW enable input (\bar{E}), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The "4067" contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to a common input/output (Z).

With \bar{E} LOW, one of the sixteen switches is selected (low impedance ON-state) by S_0 to S_3 . All unselected switches are in the high impedance OFF-state. With \bar{E} HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_3 .

The analog inputs/outputs (Y_0 to Y_{15} , and Z) can swing between V_{CC} as a positive limit and GND as a negative limit. V_{CC} to GND may not exceed 10 V.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/t_{PZH}	turn-on time \bar{E} to V_{OS} S_n to V_{OS}	$C_L = 15$ pF $R_L = 1$ k Ω $V_{CC} = 5$ V	26 29	32 33	ns ns
t_{PLZ}/t_{PHZ}	turn-off time \bar{E} to V_{OS} S_n to V_{OS}		27 29	26 30	ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	29	29	pF
C_S	max. switch capacitance independent (Y) common (Z)		5 45	5 45	pF pF

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6$ ns

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \} \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs

C_L = output load capacitance in pF

C_S = max. switch capacitance in pF

V_{CC} = supply voltage in V

- For HC the condition is $V_i = \text{GND to } V_{CC}$

For HCT the condition is $V_i = \text{GND to } V_{CC} - 1.5$ V

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).

24-lead mini-pack; plastic (SO24; SOT137A).

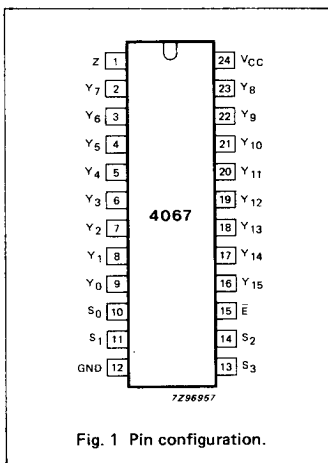


Fig. 1 Pin configuration.

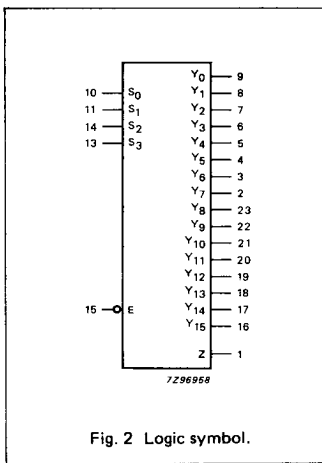


Fig. 2 Logic symbol.

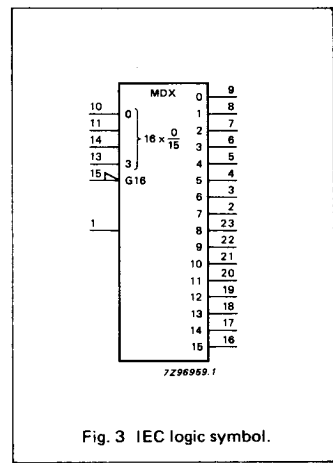


Fig. 3 IEC logic symbol.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Z	common input/output
9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	Y ₀ to Y ₁₅	independent inputs/outputs
10, 11, 14, 13	S ₀ to S ₃	address inputs
12	GND	ground (0 V)
15	E	enable input (active LOW)
24	V _{CC}	positive supply voltage

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS					CHANNEL ON
E	S ₃	S ₂	S ₁	S ₀	
L	L	L	L	L	Y ₀ - Z
L	L	L	L	H	Y ₁ - Z
L	L	L	H	L	Y ₂ - Z
L	L	L	H	H	Y ₃ - Z
L	L	H	L	L	Y ₄ - Z
L	L	H	L	H	Y ₅ - Z
L	L	H	H	L	Y ₆ - Z
L	L	H	H	H	Y ₇ - Z
L	H	L	L	L	Y ₈ - Z
L	H	L	L	H	Y ₉ - Z
L	H	L	H	L	Y ₁₀ - Z
L	H	L	H	H	Y ₁₁ - Z
L	H	H	L	L	Y ₁₂ - Z
L	H	H	L	H	Y ₁₃ - Z
L	H	H	H	L	Y ₁₄ - Z
L	H	H	H	H	Y ₁₅ - Z
H	X	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

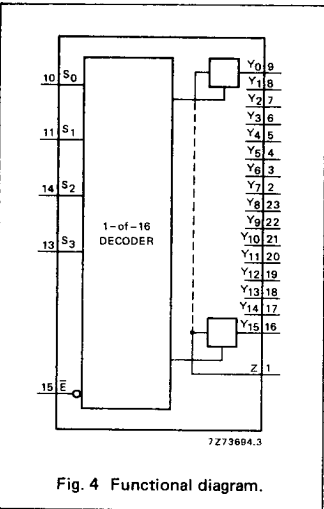


Fig. 4 Functional diagram.

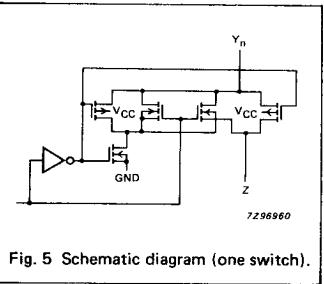


Fig. 5 Schematic diagram (one switch).

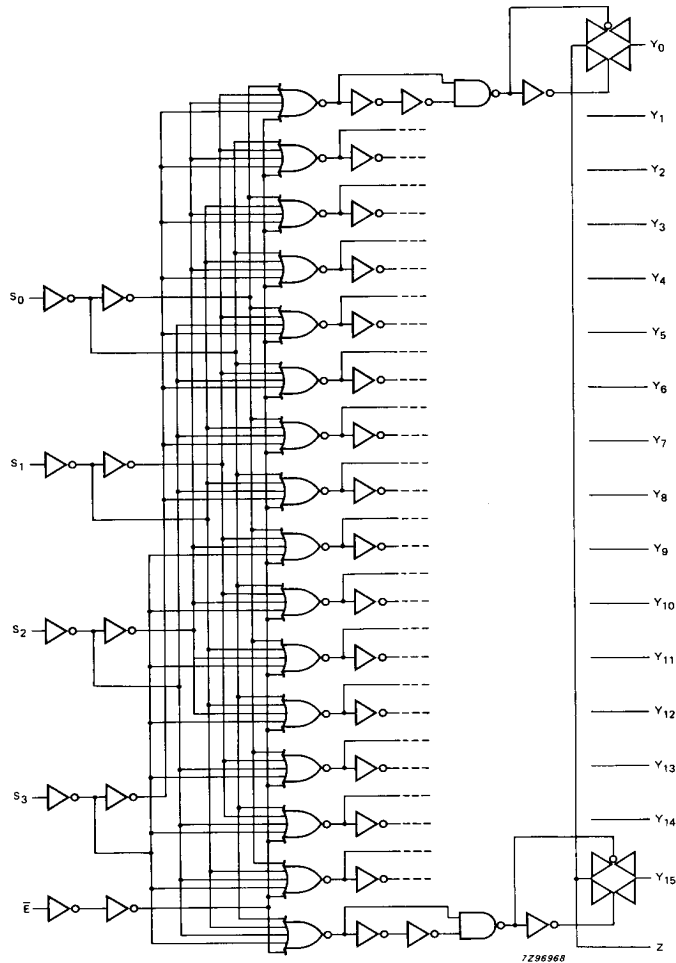
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Fig. 6 Logic diagram.

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Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V _{CC}	DC supply voltage	-0.5	+11.0	V	
±I _{IK}	DC digital input diode current		20	mA	for V _I < -0.5 V or V _I > V _{CC} + 0.5 V
±I _{SK}	DC switch diode current		20	mA	for V _S < -0.5 V or V _S > V _{CC} + 0.5 V
±I _S	DC switch current		25	mA	for -0.5 V < V _S < V _{CC} + 0.5 V
±I _{CC} ; ±I _{GND}	DC V _{CC} or GND current		50	mA	
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P _S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V _{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V _I	DC input voltage range	GND		V _{CC}	GND		V _{CC}	V	
V _S	DC switch voltage range	GND		V _{CC}	GND		V _{CC}	V	
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t _r , t _f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V V _{CC} = 10.0 V

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DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} - GND = 4.5$ V

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS			
		74HC/HCT									V _{CC} V	I _S μA	V _{is}	V _I
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
R _{ON}	ON-resistance (peak)		110	180		225		270	Ω	2.0	100	V _{CC} to GND	V _{IH} or V _{IL}	
			95	160		200		240	Ω	4.5	1000			
									Ω	6.0	1000			
			75	130		165		195	Ω	9.0	1000			
R _{ON}	ON-resistance (rail)		150	—		—		—	Ω	2.0	100	GND or V _{CC}	V _{IH} or V _{IL}	
			90	160		200		240	Ω	4.5	1000			
			80	140		175		210	Ω	6.0	1000			
			70	120		150		180	Ω	9.0	1000			
ΔR _{ON}	maximum variation of ON-resistance between any two channels		—						Ω	2.0		V _{CC} to GND	V _{IH} or V _{IL}	
			9						Ω	4.5				
			8						Ω	6.0				
			6						Ω	9.0				

Notes to DC characteristics

- At supply voltages ($V_{CC} - GND$) approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig. 7.

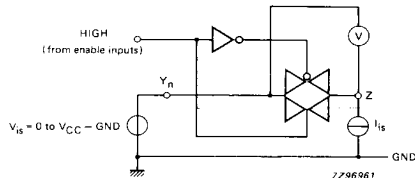


Fig. 7 Test circuit for measuring ON-resistance (R_{ON}).

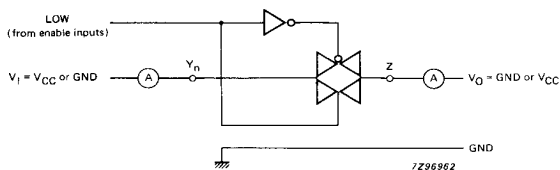


Fig. 8 Test circuit for measuring OFF-state current.

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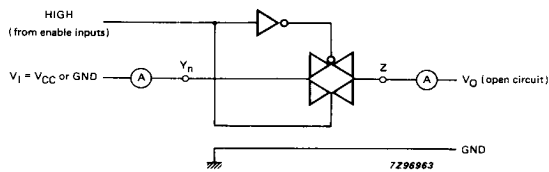


Fig. 9 Test circuit for measuring ON-state current.

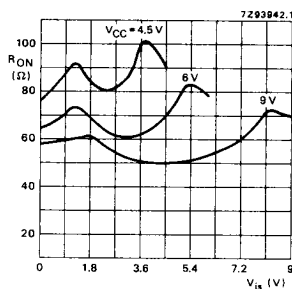


Fig. 10 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{IS}) for $V_{IS} = 0$ to $V_{CC} - GND$.

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Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS		
		74HC									V _{CC} V	V _I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V _{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0			
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V _{CC} or GND		
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} − GND (see Fig. 8)	
±I _S	analog switch OFF-state current all channels			0.8		8.0		8.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} − GND (see Fig. 9)	
±I _S	analog switch ON-state current			0.8		8.0		8.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} − GND (see Fig. 9)	
I _{CC}	quiescent supply current			8.0 16.0		80.0 160		160 320	μA	6.0 10.0	V _{CC} or GND	V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND	

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	OTHER	
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Y _n to Z		25 9 7 5	75 15 13 9		95 19 16 11		110 22 19 14	ns	2.0 4.5 6.0 9.0	R _L = ∞; C _L = 50 pF (see Fig. 16)
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Z to Y _n		18 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	
t _{PHZ} / t _{PLZ}	turn-off time E to Y _n		74 27 22 20	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 9.0	R _L = 1 kΩ; C _L = 50 pF (see Fig. 17)
t _{PHZ} / t _{PLZ}	turn-off time S _n to Y _n		83 30 24 21	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 9.0	
t _{PHZ} / t _{PLZ}	turn-off time E to Z		85 31 25 24	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	
t _{PHZ} / t _{PLZ}	turn-off time S _n to Z		94 34 27 25	290 58 47 45		365 73 62 56		435 87 74 68	ns	2.0 4.5 6.0 9.0	
t _{PZH} / t _{PZL}	turn-on time E to Y _n		80 29 23 17	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	
t _{PZH} / t _{PZL}	turn-on time S _n to Y _n		88 32 26 18	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0	
t _{PZH} / t _{PZL}	turn-on time E to Z		85 31 25 18	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0	
t _{PZH} / t _{PZL}	turn-on time S _n to Z		94 34 27 19	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0	

Note to AC characteristics for 74HC

Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

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DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS		
		74HCT									V _{CC} V	V _I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I _I	input leakage current			0.1		1.0		1.0	μA	5.5	V _{CC} or GND		
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} − GND (see Fig. 8)	
±I _S	analog switch OFF-state current all channels			0.8		8.0		8.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} − GND (see Fig. 9)	
±I _S	analog switch ON-state current			0.8		8.0		8.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} − GND (see Fig. 9)	
I _{CC}	quiescent supply current			8.0		80.0		160	μA	4.5 to 5.5	V _{CC} or GND	V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND	
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V _{CC} −2.1 V	other inputs at V _{CC} or GND	

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E	0.6
S _n	0.5

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AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	OTHER	
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Y _n to Z		9	15		19		22	ns	4.5	R _L = ∞; C _L = 50 pF (see Fig. 16)
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Z to Y _n		6	12		15		18	ns	4.5	
t _{PHZ} / t _{PLZ}	turn-off time E̅ to Y _n		26	55		69		83	ns	4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 17)
t _{PHZ} / t _{PLZ}	turn-off time S _n to Y _n		31	55		69		83	ns	4.5	
t _{PHZ} / t _{PLZ}	turn-off time E̅ to Z		30	60		75		90	ns	4.5	
t _{PHZ} / t _{PLZ}	turn-off time S _n to Z		35	60		75		90	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time E̅ to Y _n		32	60		75		90	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time S _n to Y _n		35	60		75		90	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time E̅ to Z		38	65		81		98	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time S _n to Z		38	65		81		98	ns	4.5	

Note to the AC characteristics

Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

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Recommended conditions and typical values

GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V _{CC} V	V _{is(p-p)} V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	4.5 9.0	4.0 8.0	R _L = 10 k Ω ; C _L = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	4.5 9.0	4.0 8.0	R _L = 10 k Ω ; C _L = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	4.5 9.0	note 1	R _L = 600 Ω ; C _L = 50 pF f = 1 MHz (see Figs 11 and 15)
f _{max}	minimum frequency response (-3 dB)	90 100	MHz MHz	4.5 9.0	note 2	R _L = 50 Ω ; C _L = 10 pF (see Figs 12 and 13)
C _S	maximum switch capacitance independent (Y) common (Z)	5 45	pF pF			

Notes to the AC characteristics*General note*V_{is} is the input voltage at Y_n or Z terminal, whichever is assigned as an input.V_{os} is the output voltage at Y_n or Z terminal, whichever is assigned as an output.*Notes*

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

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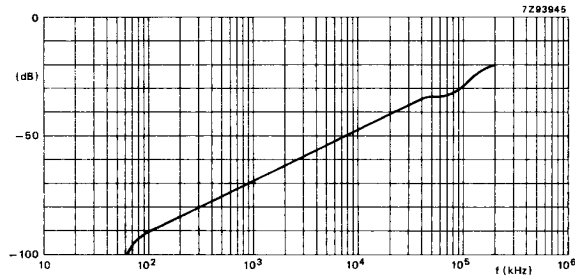


Fig. 11 Typical switch "OFF" signal feed-through as a function of frequency.

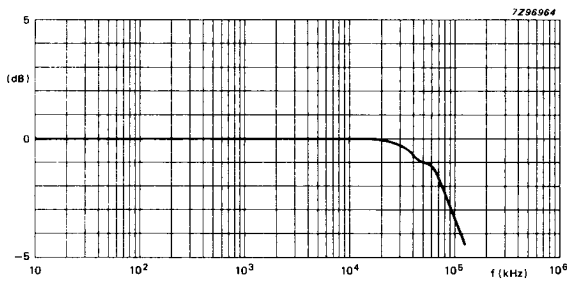


Fig. 12 Typical frequency response.

Note to Figs 11 and 12

Test conditions:
 $V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$;
 $R_L = 50 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

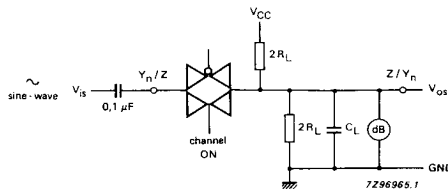
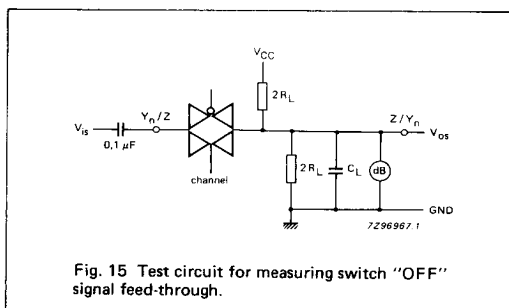
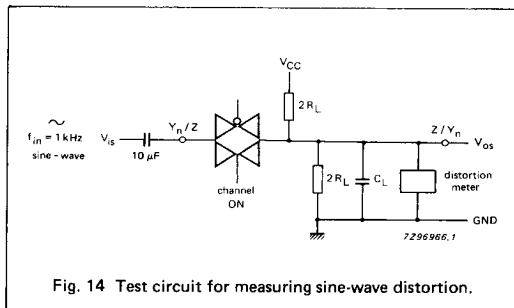


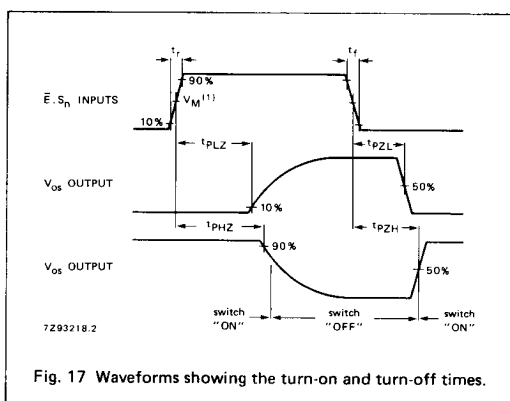
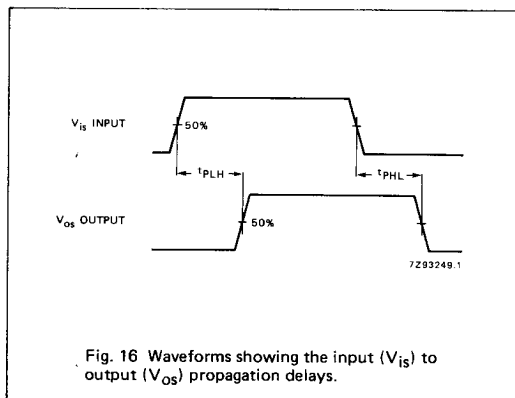
Fig. 13 Test circuit for measuring minimum frequency response.

Note to Fig. 13

Adjust input voltage to obtain
0 dBm at V_{0s} when $f_{in} = 1 \text{ MHz}$.
After set-up frequency of f_{in} is
increased to obtain a reading of
-3 dB at V_{0s} .

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AC WAVEFORMS

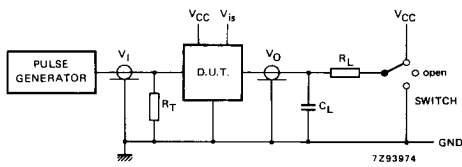


Note to Fig. 17

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

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TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	V_{is}
tpZH	GND	V_{CC}
tpZL	V_{CC}	GND
tpHZ	GND	V_{CC}
tPLZ	V_{CC}	GND
others	open	pulse

Fig. 18 Test circuit for measuring AC performance.

Definitions for Figs 18 and 19:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

$t_r = t_f = 6$ ns, when measuring f_{max} , there is no constraint on t_r, t_f with 50% duty factor.

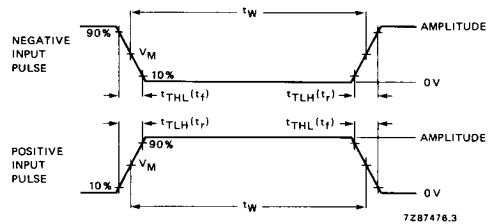


Fig. 19 Input pulse definitions.

FAMILY	AMPLITUDE	V_M	t_r, t_f	
			f_{max} , PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns