

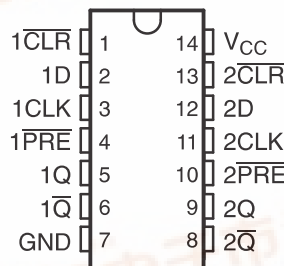
FEATURES

- Controlled Baseline
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree ⁽¹⁾

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to 10 LSTTL Loads
- Low Power Consumption, 80 μA Max I_{CC}
- Typical $t_{\text{pd}} = 15 \text{ ns}$
- $\pm 4 \text{ mA}$ Output Drive at 5 V
- Low Input Current of 1 mA Max

D OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74HC74 device contains two independent D-type positive edge triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|------------------------|--------------|-----------------------|------------------|
| -55°C to 125°C | SOIC – D | Reel of 2500 | SN74HC74MDREP | HC74MEP |
| | TSSOP – PW | Reel of 2000 | SN74HC74MPWREP | HC74MEP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|-------------------------|-------------------------|------------|---|------------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H ⁽¹⁾ | H ⁽¹⁾ |
| H | H | \uparrow | H | H | L |
| H | H | \uparrow | L | L | H |
| H | H | L | X | Q_0 | $\overline{\text{Q}}_0$ |

(1) This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



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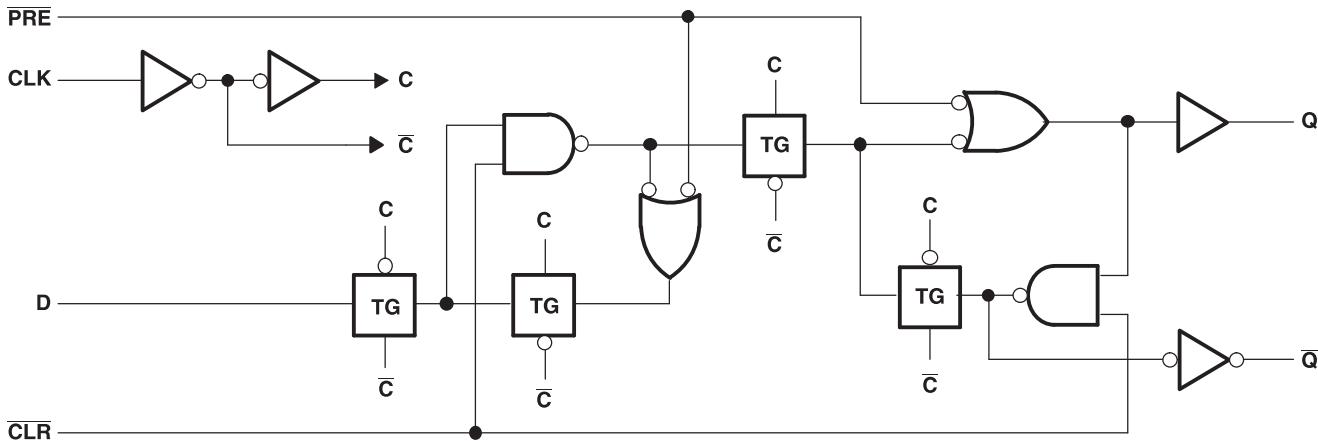
SN74HC74-EP

DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET

SC15749 MARCH 2008

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LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|------------------|---|--|------|-----|------|
| V _{CC} | Supply voltage range | | −0.5 | 7 | V |
| I _{IK} | Input clamp current | V _I < 0 or V _I = 0 to V _{CC} ⁽¹⁾ | | ±20 | mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O = 0 to V _{CC} ⁽¹⁾ | | ±20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±25 | mA |
| | Continuous current through V _{CC} or GND | | | ±50 | mA |
| θ _{JA} | Package thermal impedance ⁽²⁾ | PW package | | 113 | °C/W |
| T _{stg} | Storage temperature range | | −60 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|-----------------|---------------------------------|-------------------------|------|-----------------|------|
| V _{CC} | Supply voltage | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | V |
| | | V _{CC} = 4.5 V | 3.15 | | |
| | | V _{CC} = 6 V | 4.2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | V |
| | | V _{CC} = 4.5 V | | 1.35 | |
| | | V _{CC} = 6 V | | 1.8 | |
| V _I | Input voltage | 0 | | V _{CC} | V |
| V _O | Output voltage | 0 | | V _{CC} | V |
| ΔtΔv | Input transition rise/fall time | V _{CC} = 2 V | | 1000 | ns |
| | | V _{CC} = 4.5 V | | 500 | |
| | | V _{CC} = 6 V | | 400 | |
| T _A | Operating free-air temperature | -55 | | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----|-------|------|
| | | | | MIN | TYP | MAX | | | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = –20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | |
| | | I _{OH} = –4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | |
| | | I _{OH} = –5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 µA | 2 V | | 0.002 | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 4 | | 80 | µA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | pF |

TIMING REQUIREMENTS

| | | | V _{CC} | T _A = 25°C | | MIN | MAX | UNIT |
|--------------------|---|--|-----------------|-----------------------|-----|-----|-----|------|
| | | | | MIN | MAX | | | |
| f _{clock} | Clock frequency | | 2 V | 6 | | 4.2 | | MHz |
| | | | 4.5 V | 31 | | 21 | | |
| | | | 6 V | 0 | 36 | 0 | 25 | |
| t _w | Pulse duration | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low | 2 V | 100 | | 150 | | ns |
| | | | 4.5 V | 20 | | 30 | | |
| | | | 6 V | 17 | | 25 | | |
| | CLK high or low | 2 V | 80 | | 120 | | | |
| | | 4.5 V | 16 | | 24 | | | |
| | | 6 V | 14 | | 20 | | | |
| t _{su} | Setup time before CLK↑ | Data | 2 V | 100 | | 150 | | ns |
| | | | 4.5 V | 20 | | 30 | | |
| | | | 6 V | 17 | | 25 | | |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 2 V | 25 | | 40 | | | |
| | | 4.5 V | 5 | | 8 | | | |
| | | 6 V | 4 | | 7 | | | |
| t _h | Hold time, data after CLK↑ | | 2 V | 0 | | 0 | | ns |
| | | | 4.5 V | 0 | | 0 | | |
| | | | 6 V | 0 | | 0 | | |

SN74HC74-EP

DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET

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SWITCHING CHARACTERISTICS

over operating free-air temperature range $C_L = 50$ pF, (unless otherwise noted)

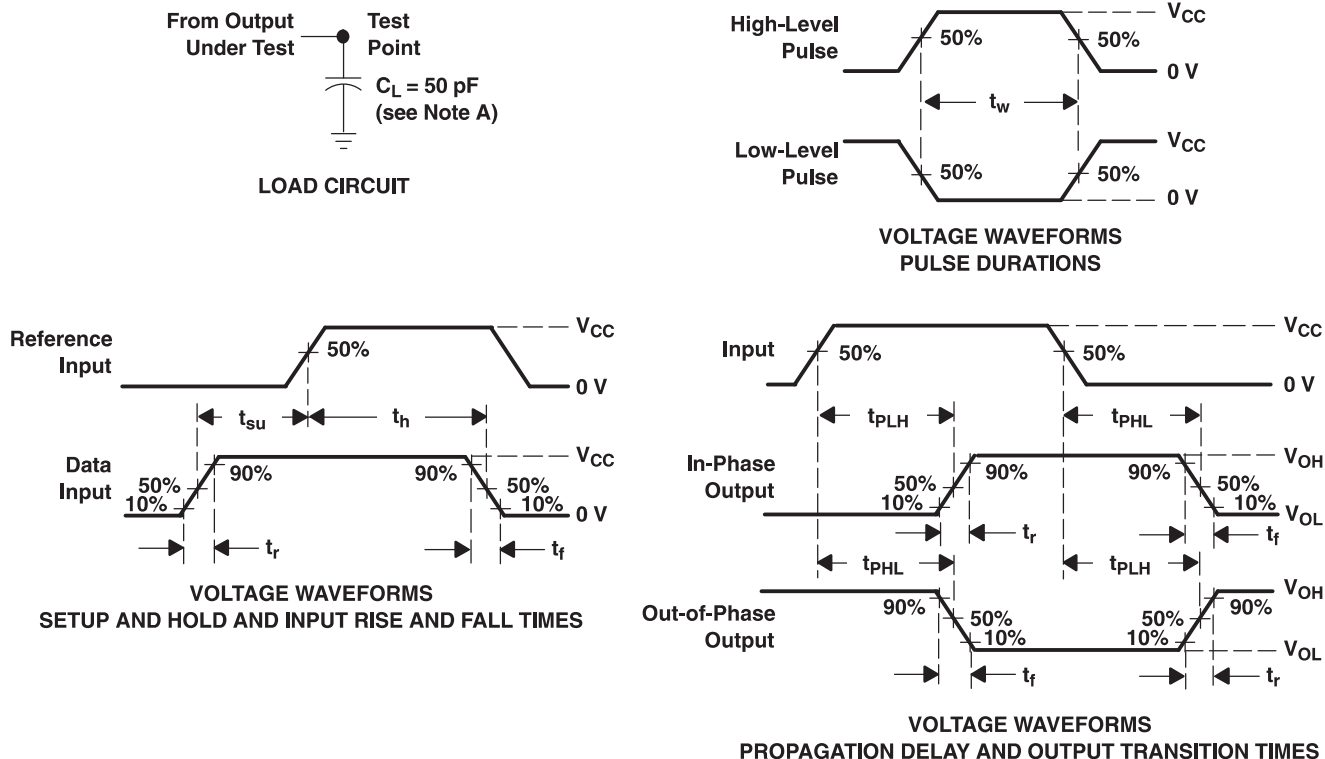
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-----------|--------------------------------------|---------------------|----------|--------------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| f_{max} | | | 2 V | 6 | 10 | | 4.2 | | MHz |
| | | | 4.5 V | 31 | 50 | | 21 | | |
| | | | 6 V | 36 | 60 | | 25 | | |
| t_{pd} | \overline{PRE} or \overline{CLR} | Q or \overline{Q} | 2 V | | 70 | 230 | | 345 | ns |
| | | | 4.5 V | | 20 | 46 | | 69 | |
| | | | 6 V | | 15 | 39 | | 59 | |
| | CLK | Q or \overline{Q} | 2 V | | 70 | 175 | | 250 | |
| | | | 4.5 V | | 20 | 35 | | 50 | |
| | | | 6 V | | 15 | 30 | | 42 | |
| t_t | | Q or \overline{Q} | 2 V | | 28 | 75 | | 110 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | |
| | | | 6 V | | 6 | 13 | | 19 | |

Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----------------|-----|------|
| C_{pd} | Power dissipation capacitance | No load | 35 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74HC74MPWREP | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/08613-01XE | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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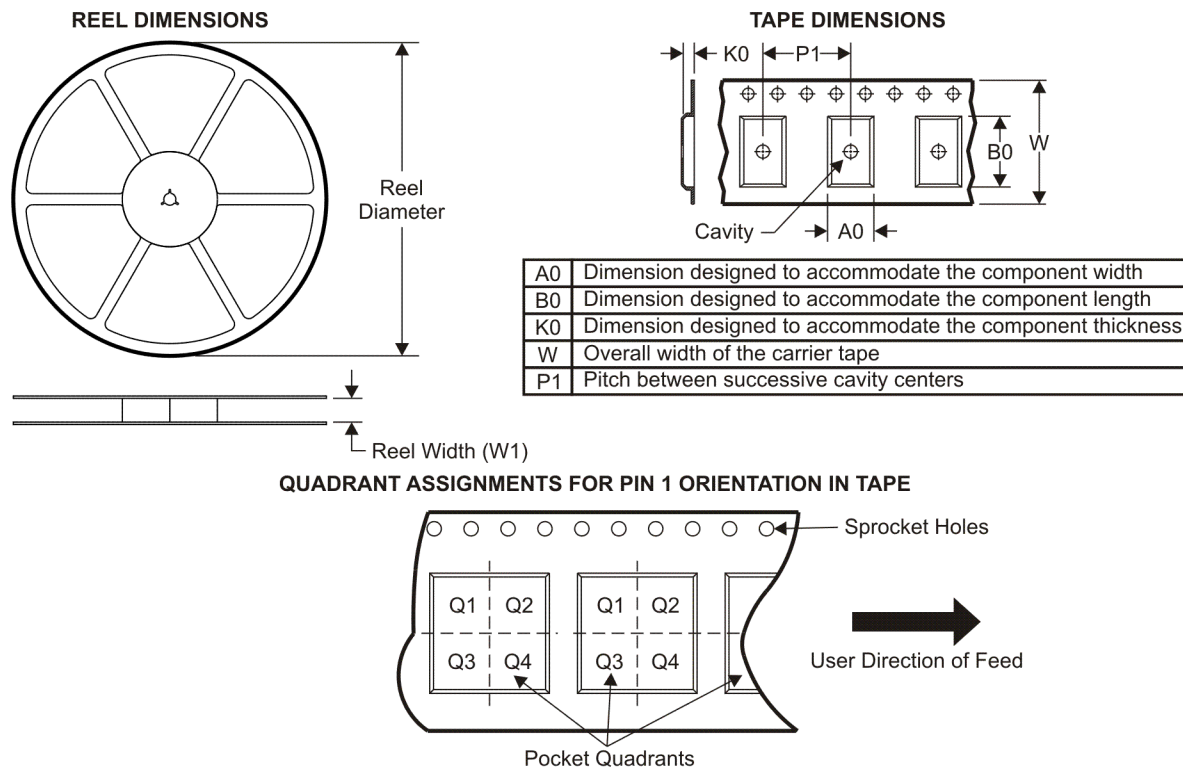
OTHER QUALIFIED VERSIONS OF SN74HC74-EP :

- Catalog: [SN74HC74](#)
- Automotive: [SN74HC74-Q1](#)
- Military: [SN54HC74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

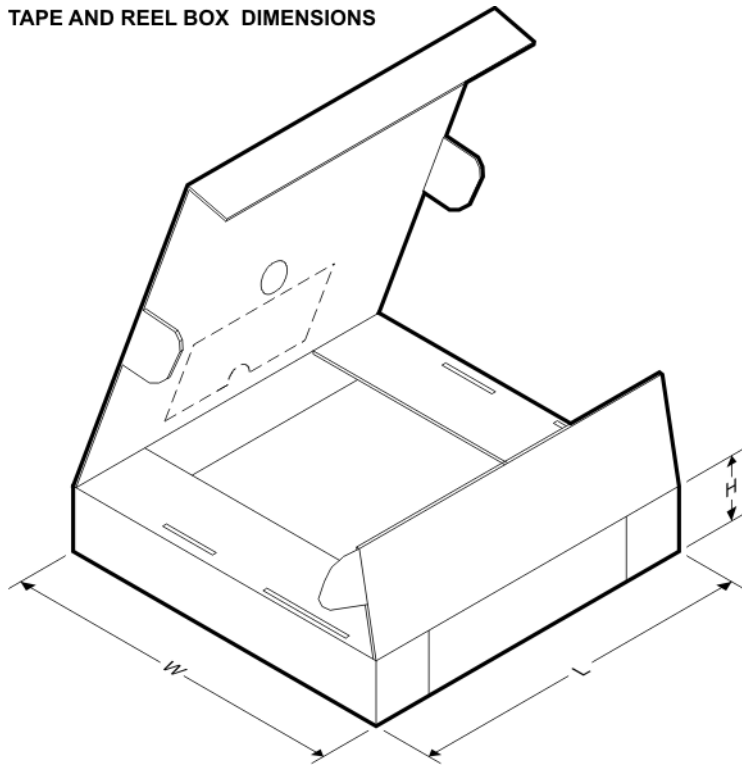
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC74MPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



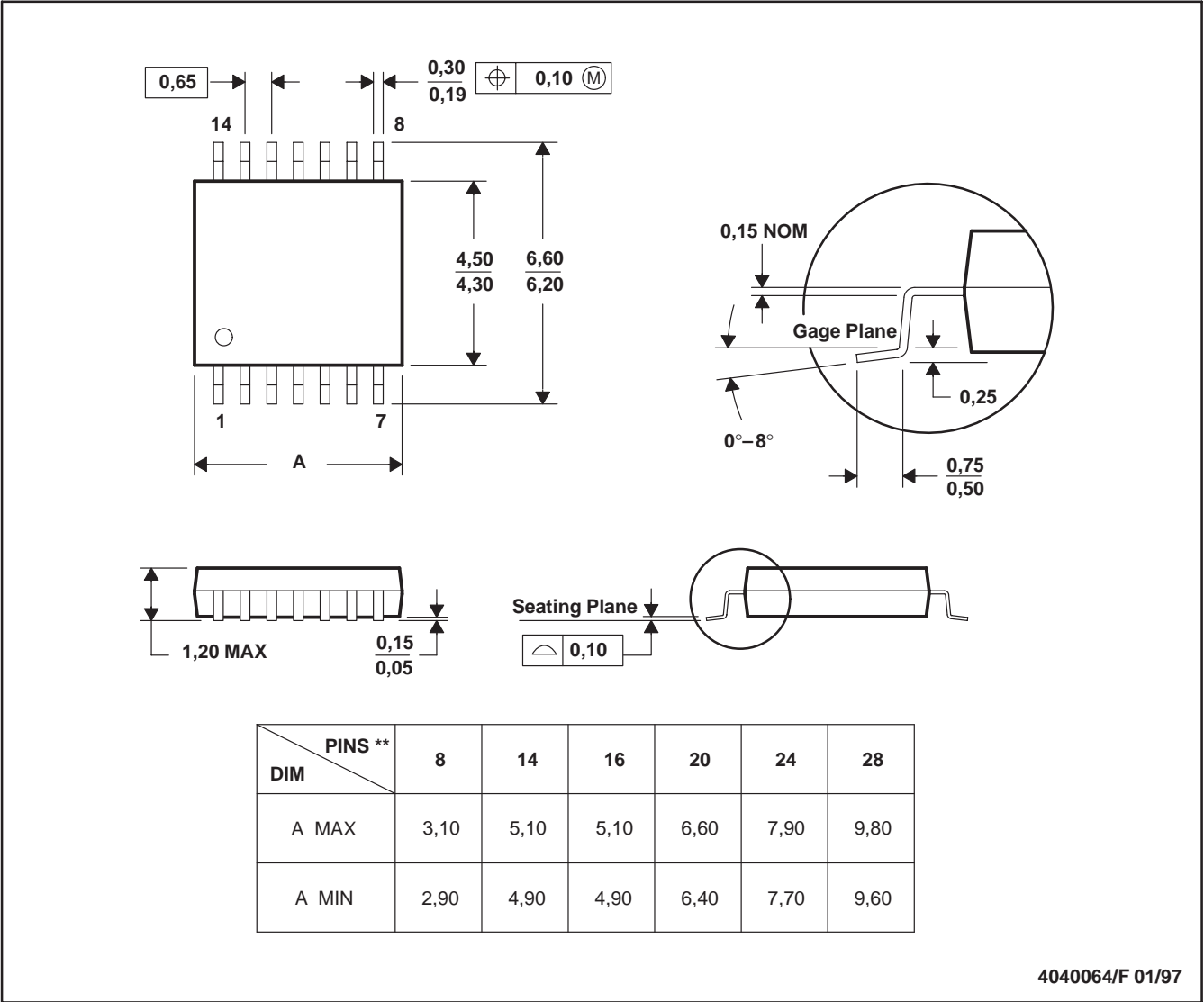
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC74MPWREP | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

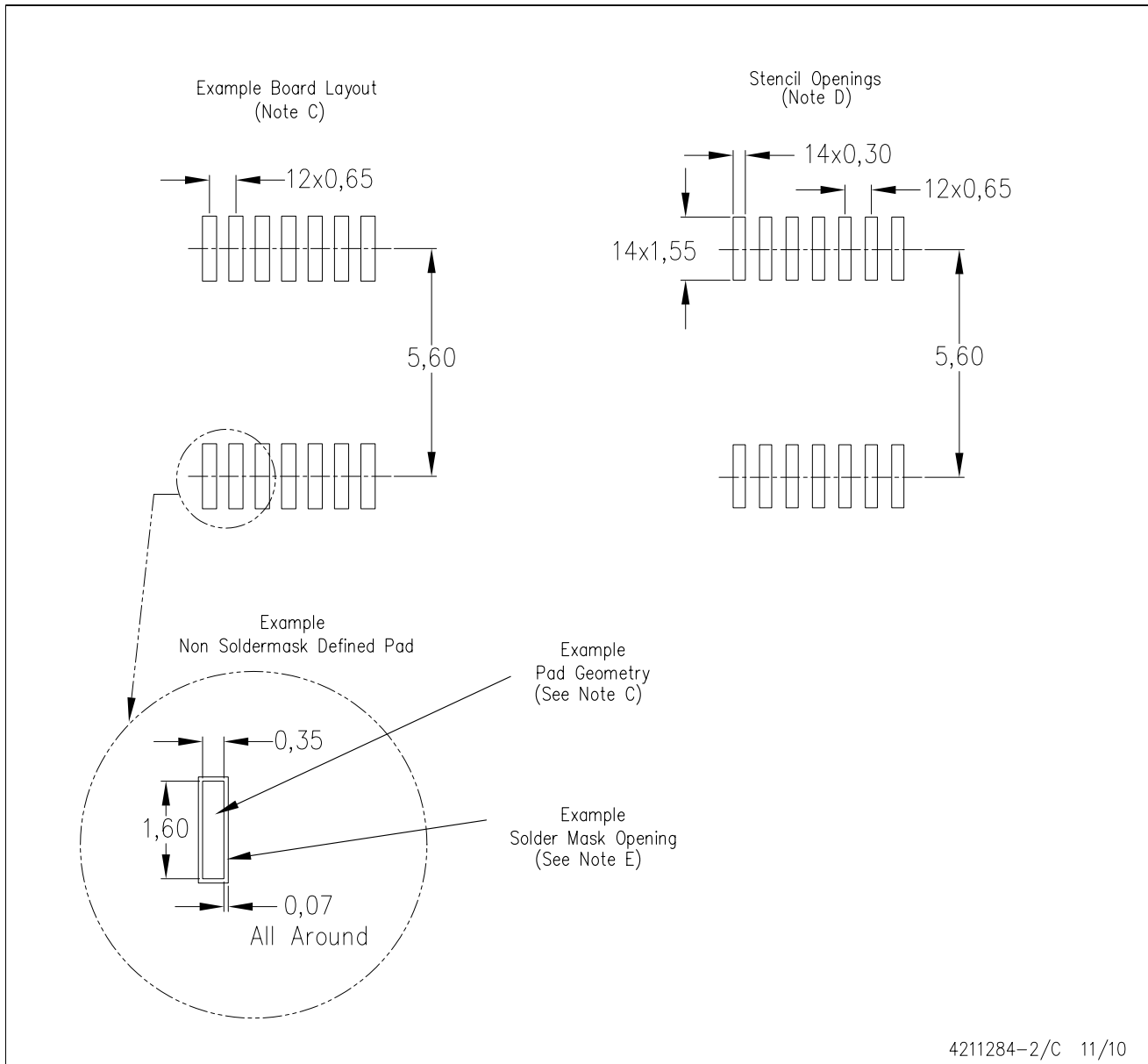
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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