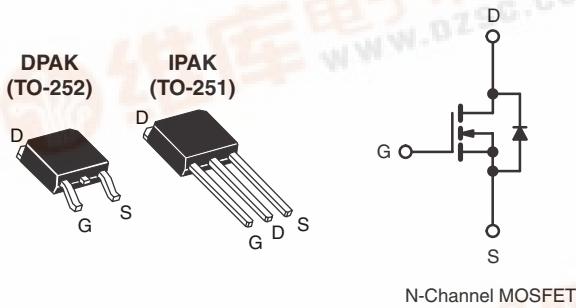


## Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
R <sub>DS(on)</sub> ( $\Omega$ )	V <sub>GS</sub> = 10 V      0.10
Q <sub>g</sub> (Max.) (nC)	25
Q <sub>gs</sub> (nC)	5.8
Q <sub>gd</sub> (nC)	11
Configuration	Single



### FEATURES

- Dynamic dV/dt Rating
- Surface Mount (IRFR024, SiHFR024)
- Straight Lead (IRFU024, SiHFU024)
- Available in Tape and Reel
- Fast Switching
- Ease of Parallelizing
- Simple Drive Requirements
- Lead (Pb)-free Available



### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

### ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR024PbF	IRFR024TRPbF <sup>a</sup>	-	IRFU024PbF
	SiHFR024-E3	SiHFR024T-E3 <sup>a</sup>	-	SiHFU024-E3
SnPb	IRFR024	IRFR024TR <sup>a</sup>	IRFR024TRL <sup>a</sup>	IRFU024
	SiHFR024	SiHFR024T <sup>a</sup>	SiHFU024TL <sup>a</sup>	SiHFU024

#### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS T<sub>C</sub> = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	$\pm 20$	
Continuous Drain Current	I <sub>D</sub>	14	A
		9.0	
T <sub>C</sub> = 25 °C			
T <sub>C</sub> = 100 °C			
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	56	
Linear Derating Factor		0.33	W/°C
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.020	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	91	mJ
Maximum Power Dissipation	P <sub>D</sub>	42	W
T <sub>C</sub> = 25 °C		2.5	
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	T <sub>A</sub> = 25 °C		
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	260 <sup>d</sup>	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V<sub>DD</sub> = 25 V, starting T<sub>J</sub> = 25 °C, L = 541  $\mu$ H, R<sub>G</sub> = 25  $\Omega$ , I<sub>AS</sub> = 14 A (see fig. 12).
- c. I<sub>SD</sub> ≤ 17 A, dI/dt ≤ 110 A/ $\mu$ s, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0	

**Note**

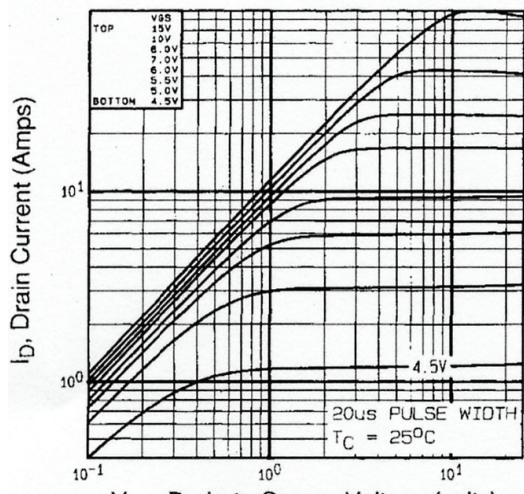
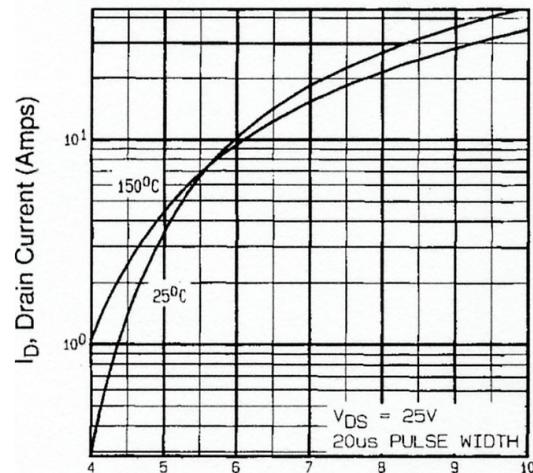
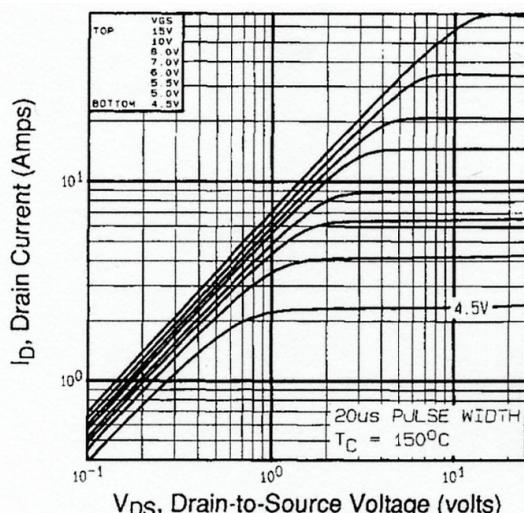
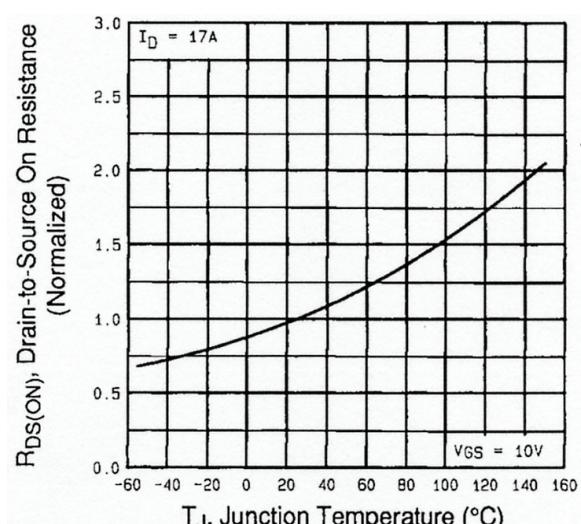
- a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		60	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1 \text{ mA}$		-	0.073	-	$^\circ\text{C}/\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	25	$\mu\text{A}$	
		$V_{DS} = 48 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^\circ\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 8.4 \text{ A}^b$	-	-	0.10	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 25 \text{ V}$ , $I_D = 8.4 \text{ A}^b$		6.2	-	-	S	
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	640	-	pF	
Output Capacitance	$C_{oss}$			-	360	-		
Reverse Transfer Capacitance	$C_{rss}$			-	79	-		
Total Gate Charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 17 \text{ A}$ , $V_{DS} = 48 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	25	nC	
Gate-Source Charge	$Q_{gs}$			-	-	5.8		
Gate-Drain Charge	$Q_{gd}$			-	-	11		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}$ , $I_D = 17 \text{ A}$ , $R_G = 18 \Omega$ , $R_D = 1.7 \Omega$ , see fig. 10 <sup>b</sup>		-	13	-	ns	
Rise Time	$t_r$			-	58	-		
Turn-Off Delay Time	$t_{d(off)}$			-	25	-		
Fall Time	$t_f$			-	42	-		
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	$L_S$			-	7.5	-		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	14	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	56		
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 14 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	1.5	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = 17 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	88	180	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.29	0.64	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )						

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^{\circ}\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^{\circ}\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

# IRFR024, IRFU024, SiHFR024, SiHFU024

Vishay Silicon IRFU024, IRFR024, SiHFR024, SiHFU024"供应商

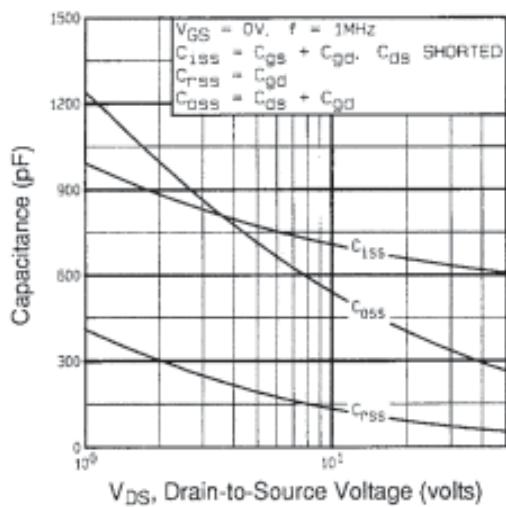


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

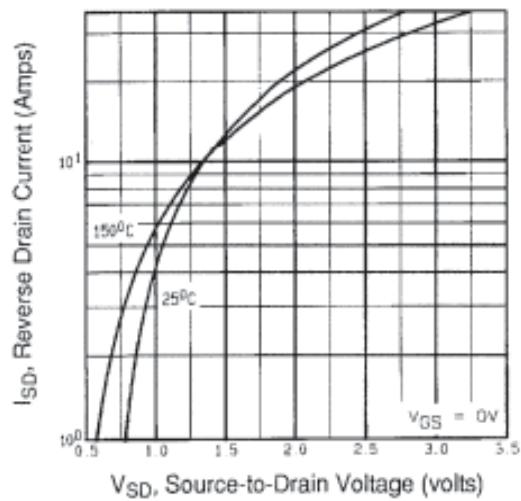


Fig. 7 - Typical Source-Drain Diode Forward Voltage

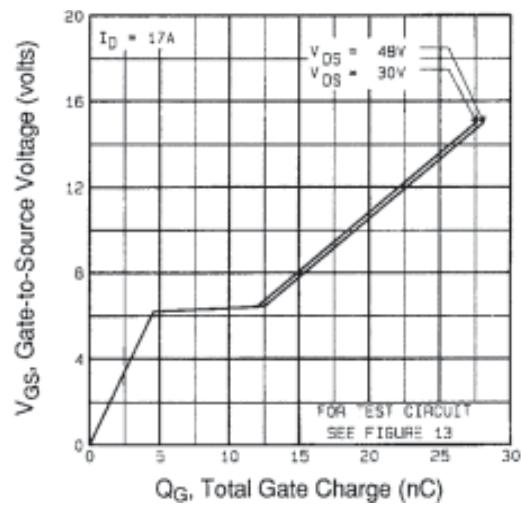


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

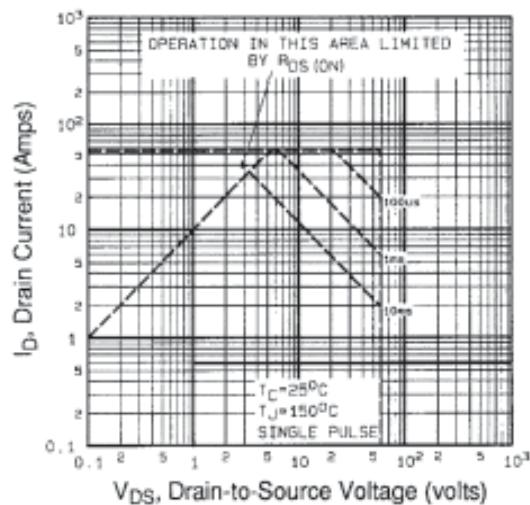


Fig. 8 - Maximum Safe Operating Area

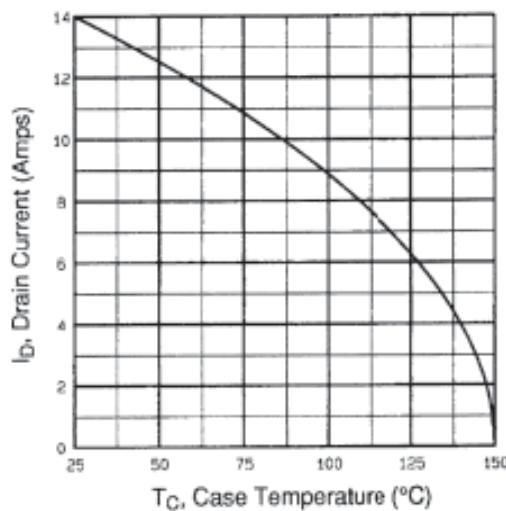


Fig. 9 - Maximum Drain Current vs. Case Temperature

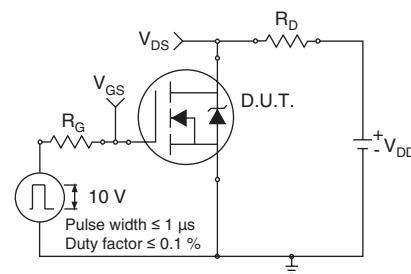


Fig. 10a - Switching Time Test Circuit

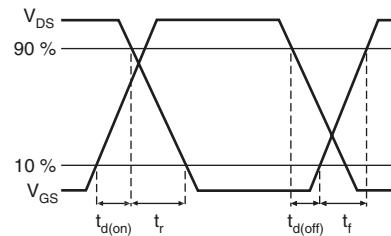


Fig. 10b - Switching Time Waveforms

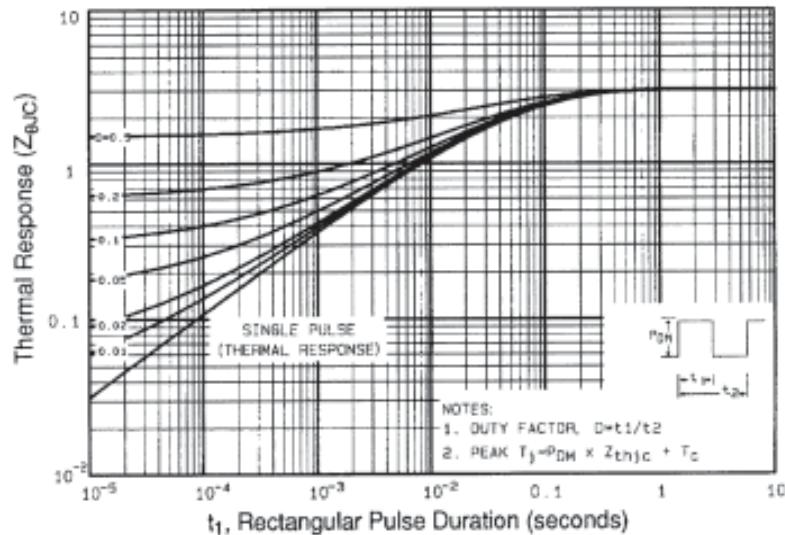


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

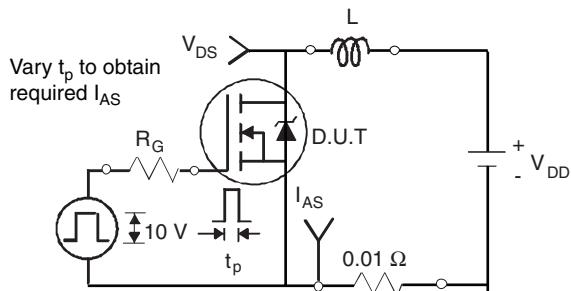


Fig. 12a - Unclamped Inductive Test Circuit

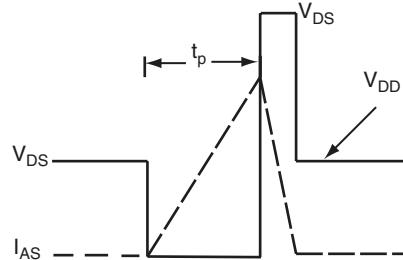


Fig. 12b - Unclamped Inductive Waveforms

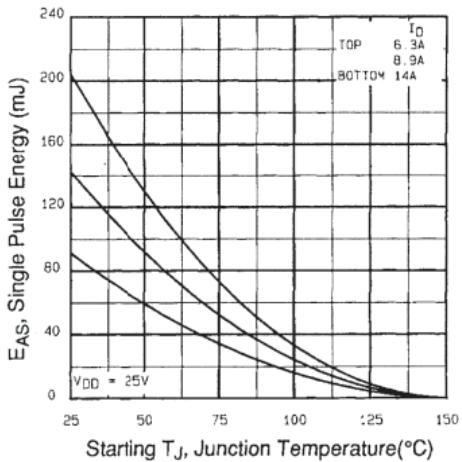


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

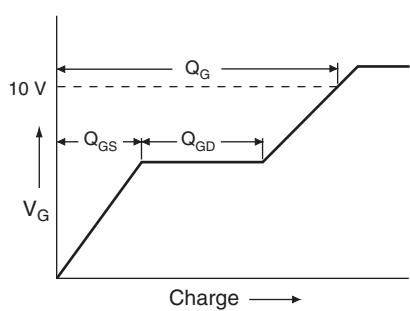


Fig. 13a - Basic Gate Charge Waveform

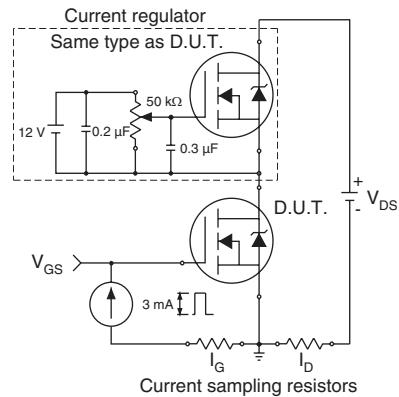
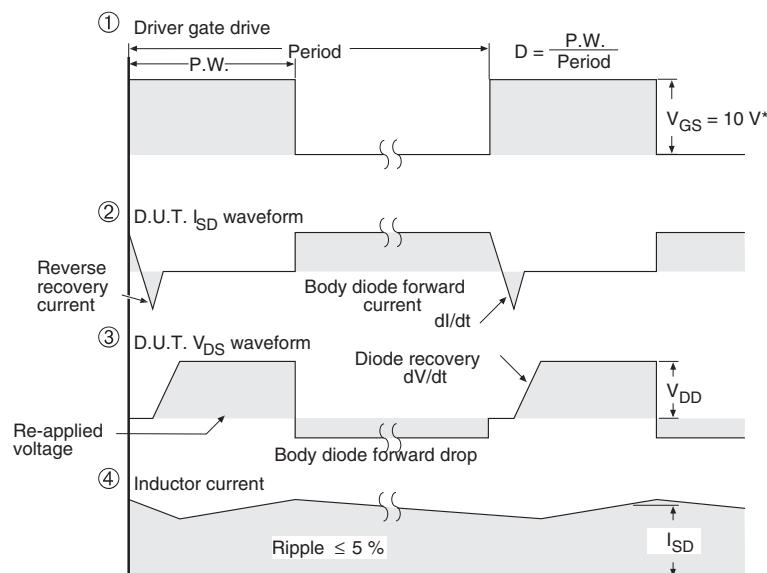
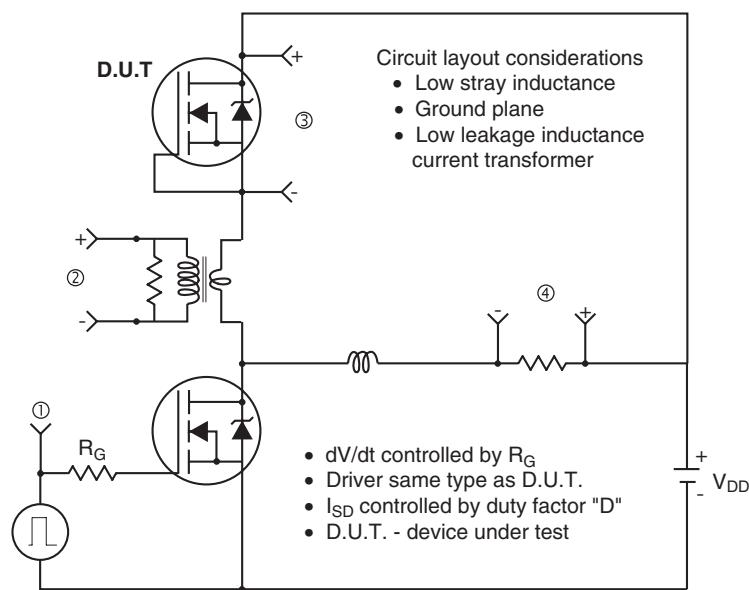


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5$  V for logic level devices

**Fig. 14 - For N-Channel**

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