



AOU405

P-Channel Enhancement Mode Field Effect Transistor



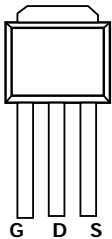
General Description

The AOU405 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the TO-251 package, this device is well suited for high current load applications. *Standard Product AOU405 is Pb-free (meets ROHS & Sony 259 specifications). AOU405L is a Green Product ordering option. AOU405 and AOU405L are electrically identical.*

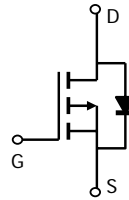
Features

V_{DS} (V) = -30V
 I_D = -18A (V_{GS} = -10V)
 $R_{DS(ON)} < 34m\Omega$ (V_{GS} = -10V)
 $R_{DS(ON)} < 60m\Omega$ (V_{GS} = -4.5V)

TO-251



Top View
 Drain Connected to Tab



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{B,G}	I_D	$T_A=25^\circ\text{C}$ ^G	-18
		$T_A=100^\circ\text{C}$ ^G	-18
Pulsed Drain Current	I_{DM}	-40	A
Avalanche Current ^C	I_{AR}	-18	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	40	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	60
		$T_C=100^\circ\text{C}$	30
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	16.7	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	40	$^\circ\text{C/W}$
Maximum Junction-to-Case ^C	$R_{\theta JC}$	1.8	2.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C		-0.003	-1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.2	-2	-2.4	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-40			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-18A T _J =125°C		28	34	mΩ
				40	47	
		V _{GS} =-4.5V, I _D =-10A		48	60	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-18A		17		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				-18	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		920	1100	pF
C _{oss}	Output Capacitance			190		pF
C _{rss}	Reverse Transfer Capacitance			122		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.6	4.5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-15V, I _D =-18A		18.7	23	nC
Q _g (4.5V)	Total Gate Charge (4.5V)			9.7	11.7	nC
Q _{gs}	Gate Source Charge			2.54		nC
Q _{gd}	Gate Drain Charge			5.4		nC
t _{D(on)}	Turn-On DelayTime			9	13	ns
t _r	Turn-On Rise Time	V _{GS} =-10V, V _{DS} =-15V, R _L =0.82Ω, R _{GEN} =3Ω		25	35	ns
t _{D(off)}	Turn-Off DelayTime			20	30	ns
t _f	Turn-Off Fall Time			12	18	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-18A, di/dt=100A/μs		21.4	26	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-18A, di/dt=100A/μs		13	16	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

I. Revision 0: August 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

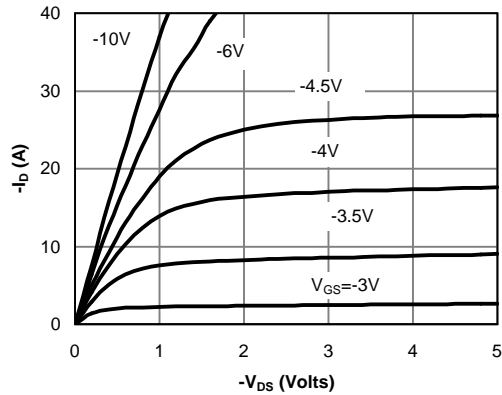


Fig 1: On-Region Characteristics

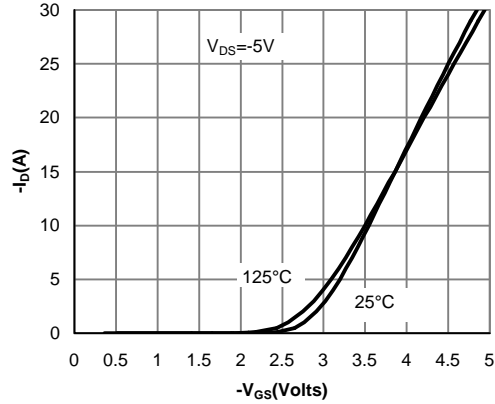


Figure 2: Transfer Characteristics

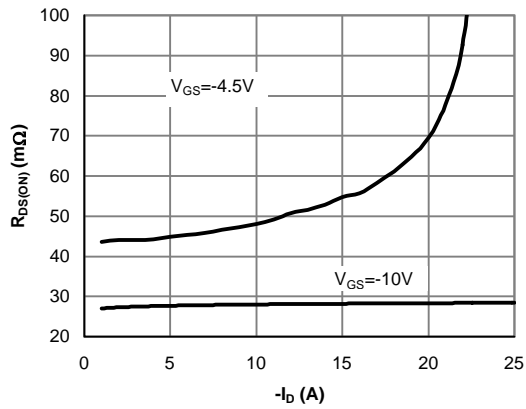


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

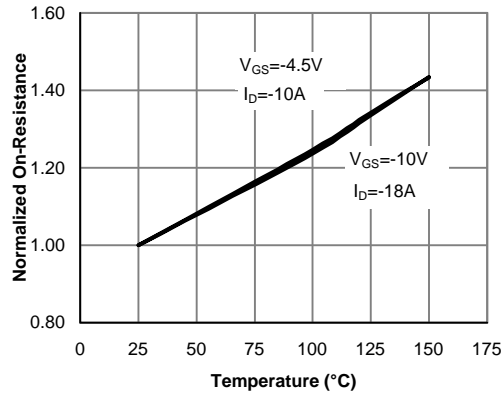


Figure 4: On-Resistance vs. Junction Temperature

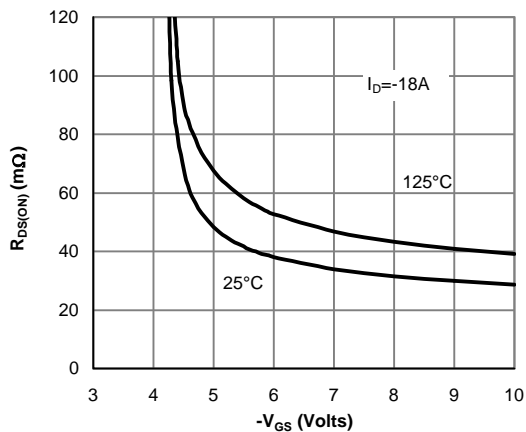


Figure 5: On-Resistance vs. Gate-Source Voltage

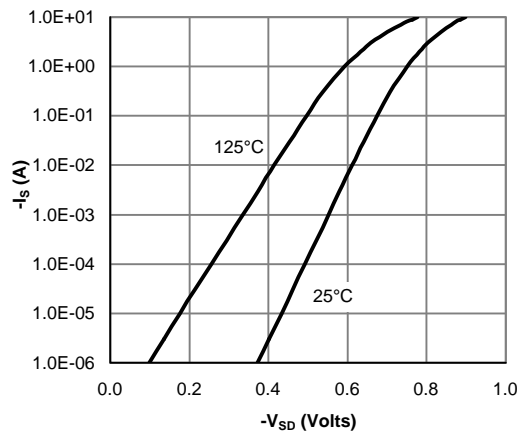


Figure 6: Body-Diode Characteristics

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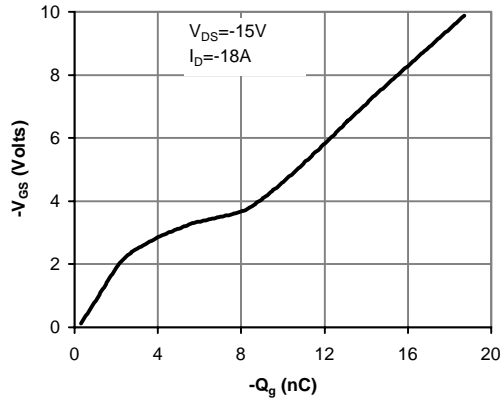


Figure 7: Gate-Charge Characteristics

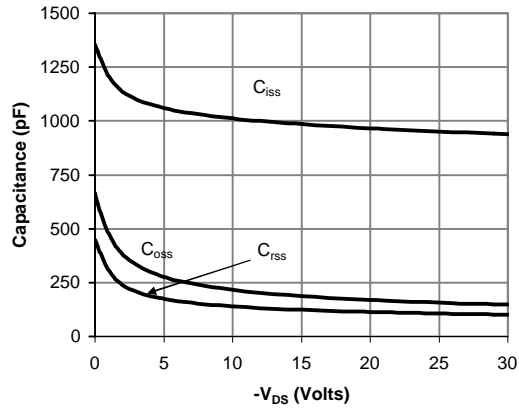


Figure 8: Capacitance Characteristics

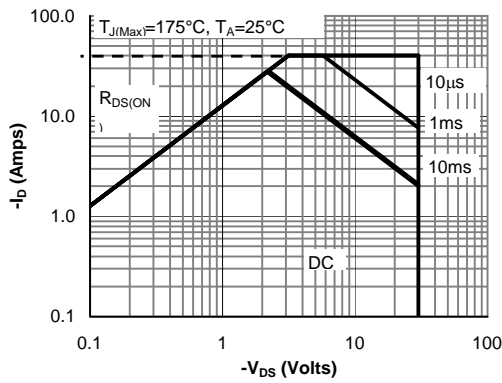


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

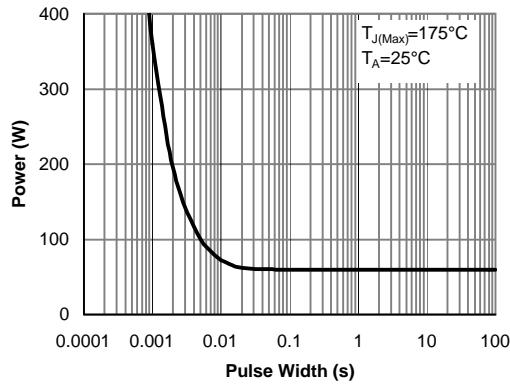


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

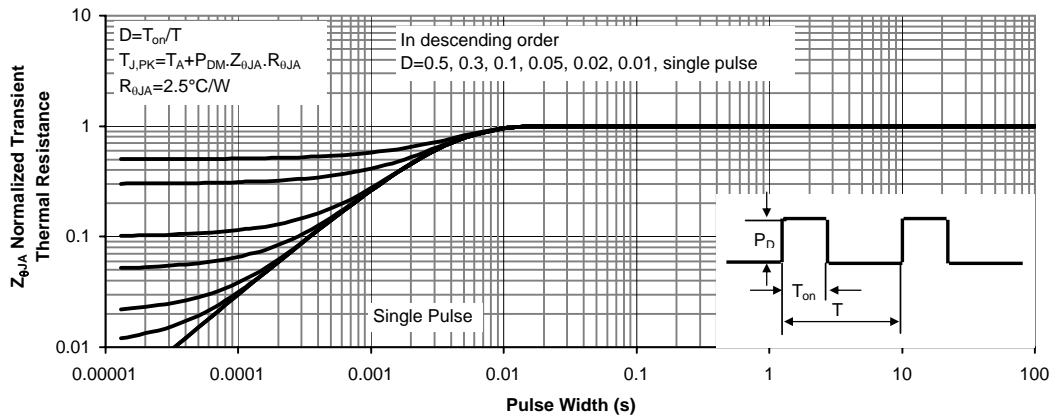


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

