

Dual Precision Instrumentation Switched-Capacitor Building Block

FEATURES

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

APPLICATIONS

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V-F and F-V Converters
- Sample and Hold
- Switched-Capacitor Filters

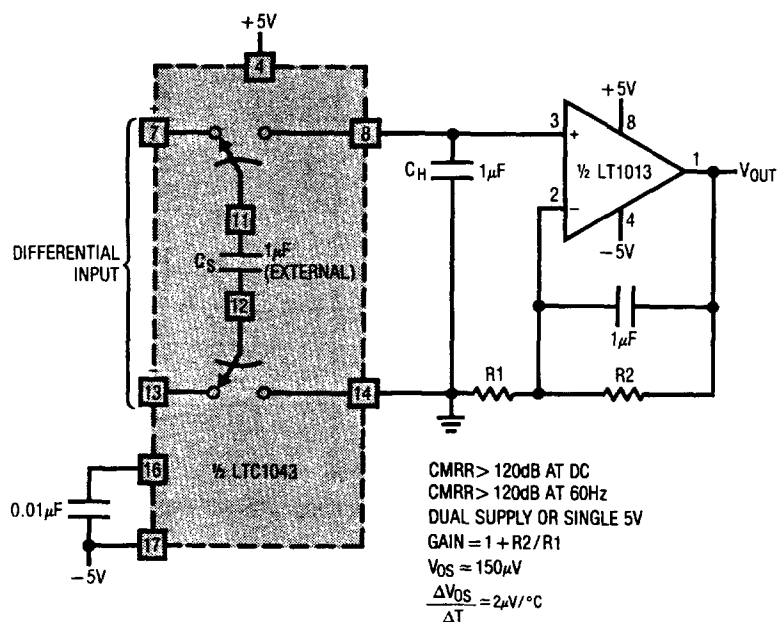
DESCRIPTION

The LTC1043 is a monolithic, charge-balanced, dual switched-capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V-F and F-V circuits without trimming, and it is also a building block for switched-capacitor filters, oscillators and modulators.

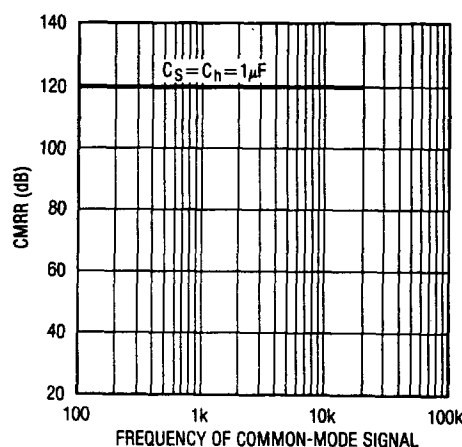
The LTC1043 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

Instrumentation Amplifier



COMMON-MODE INPUT VOLTAGE INCLUDES THE SUPPLIES

CMRR vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 18V
 Input Voltage
 at Any Pin $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
 Operating Temperature Range
 LTC1043C $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
 LTC1043M $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

		ORDER PART NUMBER
		LTC1043CN LTC1043MD

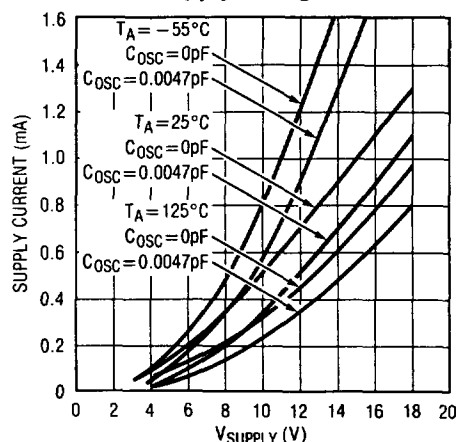
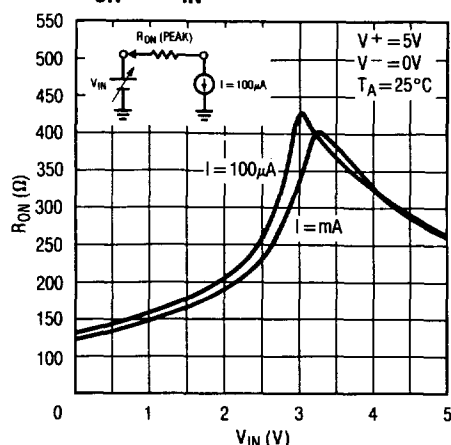
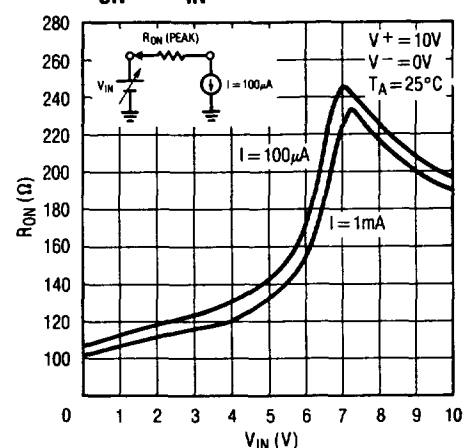
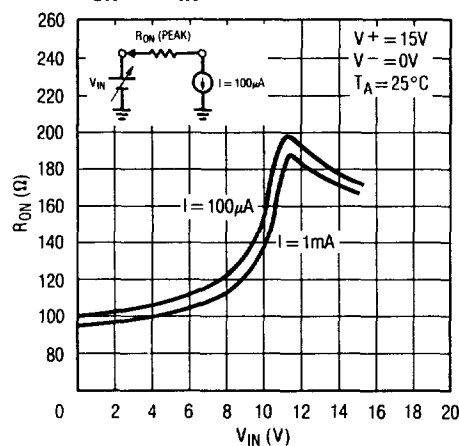
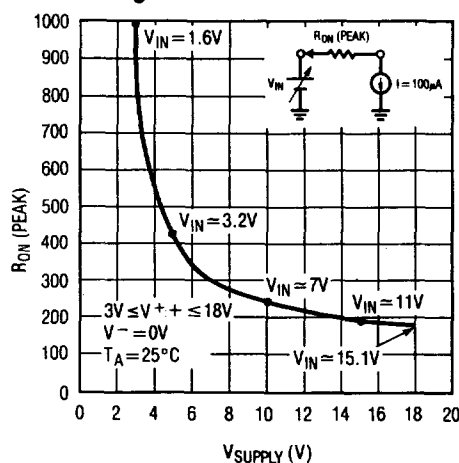
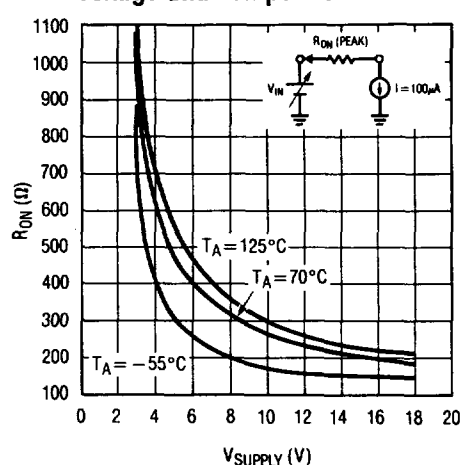
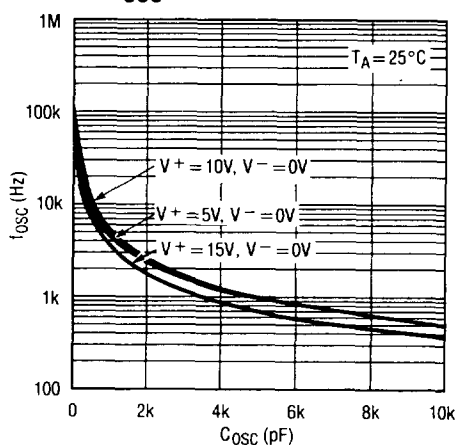
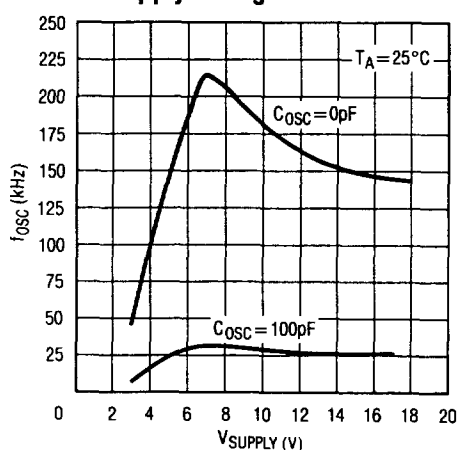
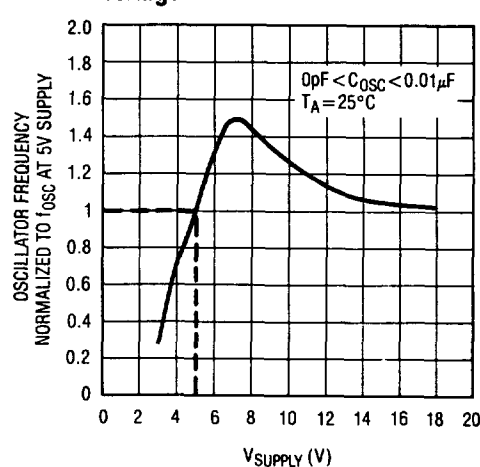
ELECTRICAL CHARACTERISTICS $V^+ = 10V$, $V^- = 0V$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1043M			LTC1043C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Power Supply Current	Pin (16) Connected High or Low	●	0.25	0.4	0.25	0.4		mA
		C_{OSC} (Pin 16 to V^-) = 100pF	●	0.4	0.65	0.4	0.65		mA
I_I	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 1)	●	6	100	6	100		pA
			●	6	500	6			nA
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 7V$, $I = \pm 0.5mA$ $V^+ = 10V$, $V^- = 0V$	●	240	400	240	400		Ω
			●		700		700		Ω
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 3.1V$, $I = \pm 0.5mA$ $V^+ = 5V$, $V^- = 0V$	●	400	700	400	700		Ω
			●		1		1		k Ω
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 16 to V^-) = 0pF		185		185			kHz
		C_{OSC} (Pin 16 to V^-) = 100pF		20	34	20	34		kHz
		Test Circuit 3	●	15	75	15	75		kHz
I_{OSC}	Pin Source or Sink Current	Pin 16 at V^+ or V^-	●	40	70	40	70		μA
			●		100		100		μA
	Break-Before-Make Time			25		25			ns
	Clock to Switching Delay	C_{OSC} Pin Externally Driven		75		75			ns
f_M	Maximum External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels		5		5			MHz
CMRR	Common-Mode Rejection Ratio	$V^+ = 5V$, $V^- = -5V$, $-5V < V_{CM} < 5V$, DC to 400Hz		120		120			dB

The ● denotes the specifications which apply over the full operating temperature range: LTC1043M operates from $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$; LTC1043C operates from $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$.

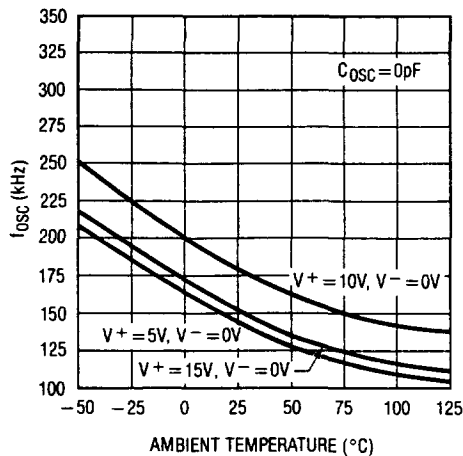
Note 1: OFF leakage current is guaranteed but not tested at 25°C .

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

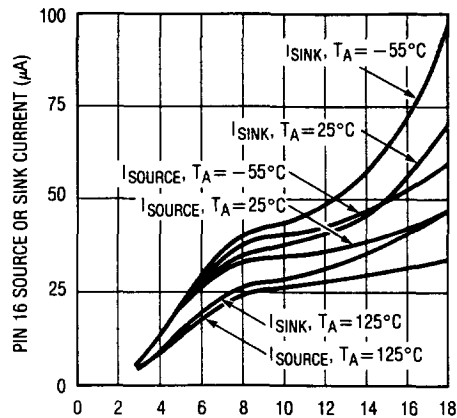
Power Supply Current vs
Power Supply Voltage R_{ON} vs V_{IN}  R_{ON} vs V_{IN}  R_{ON} vs V_{IN}  R_{ON} (Peak) vs Power Supply
Voltage R_{ON} (Peak) vs Power Supply
Voltage and TemperatureOscillator Frequency, f_{OSC} ,
vs C_{OSC} Oscillator Frequency, f_{OSC} ,
vs Supply VoltageNormalized Oscillator
Frequency, f_{OSC} , vs Supply
Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

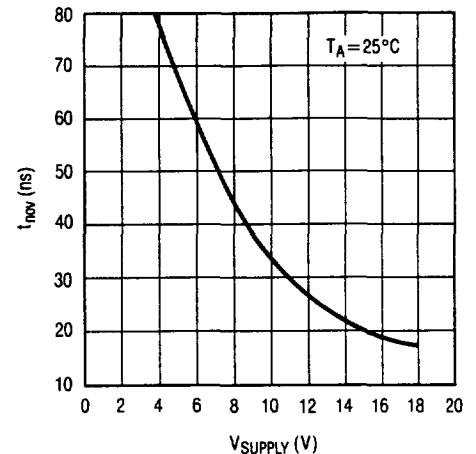
Oscillator Frequency, f_{osc} , vs
Ambient Temperature, T_A



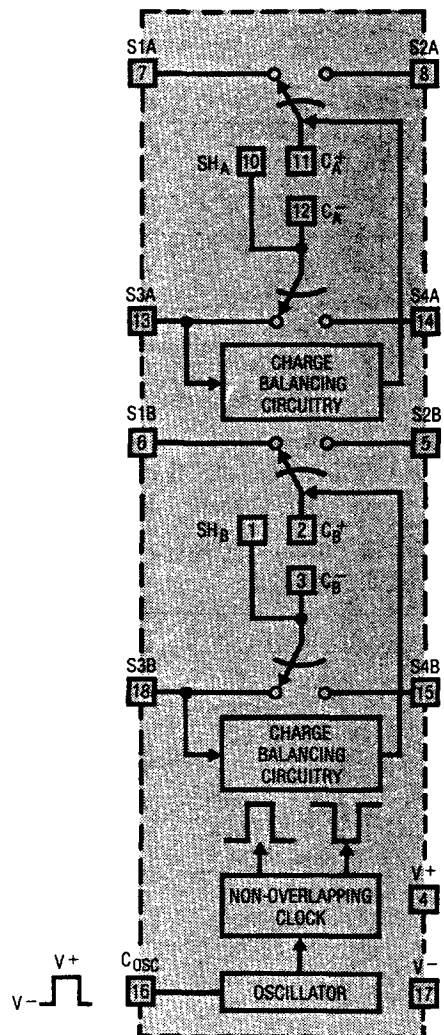
Cosc Pin I_{SINK} , I_{SOURCE} vs
Supply Voltage



Break-Before-Make Time, t_{nov} ,
vs Supply Voltage



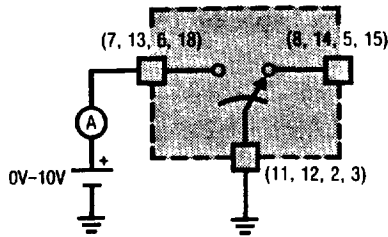
BLOCK DIAGRAM



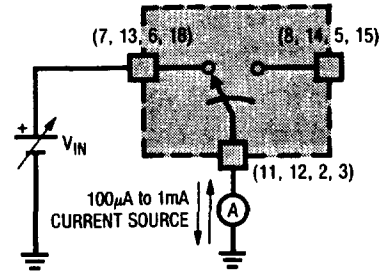
THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT $S3$ WITH RESPECT TO $S4$ (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C^+ PIN (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END. FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, $S3A$ AND $S3B$ SHOULD BE GROUND.

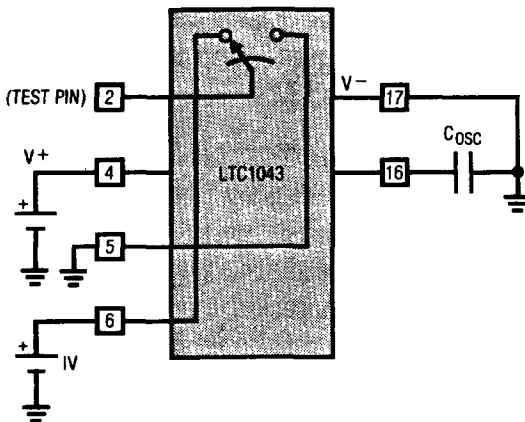
TEST CIRCUITS



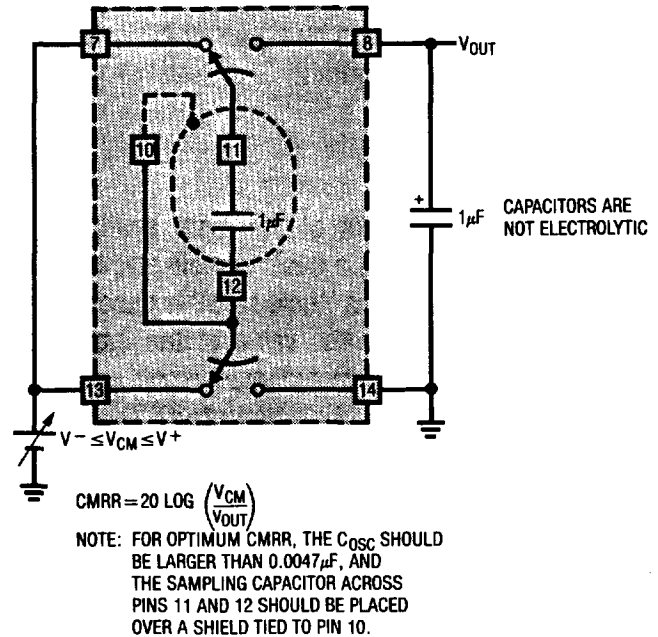
Test Circuit 1. Leakage Current Test



Test Circuit 2. R_{ON} Test



Test Circuit 3. Oscillator Frequency, f_{osc}



Test Circuit 4. CMRR Test

APPLICATIONS INFORMATION

Common-Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter (Figure 1) rejects common-mode signals and preserves differential voltages. Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common-mode voltage frequency. During the sampling mode, the impedance of pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common-mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S , C_H) and on the sampling frequency. Since the common-mode voltages are not sampled, the common-mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1

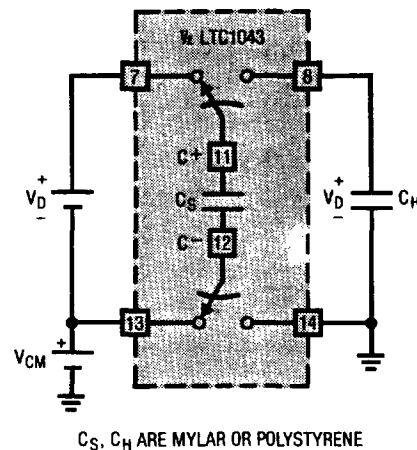


Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

is measured by shorting pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease, Figure 2.

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample and hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pC of charge injected into a 0.01 μ F capacitor causes a 200 μ V hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample and hold small signals around ground without any significant error.

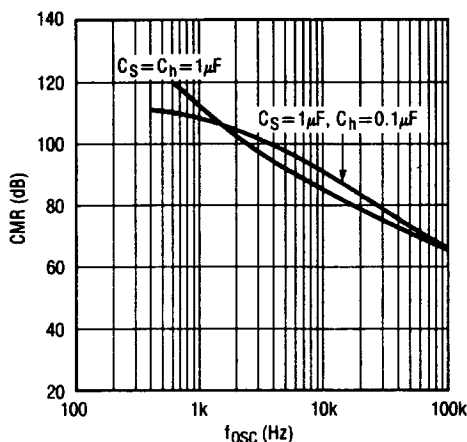


Figure 2. CMRR vs Sampling Frequency

Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043, (Figure 1). The common-mode error due to the internal junction capacitances of the C^+ pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor (Figure 5) and connected to either pin 1 or 3 helps to boost the CMRR in excess of 120dB.

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input Pins, SCR Sensitivity

An internal 60 Ω resistor is connected in series with the input of the switches (pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not

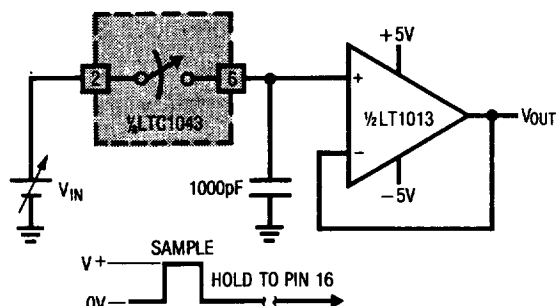


Figure 3

APPLICATIONS INFORMATION

latch until the input current reaches 2mA–3mA. The device will recover from the latch mode when the input drops 3V–4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C⁺ and C[−] pins.

Cosc Pin (16), Figure 6

The Cosc pin can be used with an external capacitor, Cosc, connected from pin 16 to pin 17, to modify the internal oscillator frequency. If pin 16 is floating, the internal 24pF capacitor plus any external interpin capacitance set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator fre-

quency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 16, they will in reality drive the Cosc pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 Cosc pins. The typical trip levels of the Schmitt trigger, Figure 6, are given below.

SUPPLY	TRIP LEVELS	
V ⁺ = 5V, V [−] = 0V	V _H = 3.4V	V _L = 1.35V
V ⁺ = 10V, V [−] = 0V	V _H = 6.5V	V _L = 2.8V
V ⁺ = 15V, V [−] = 0V	V _H = 9.5V	V _L = 4.1V

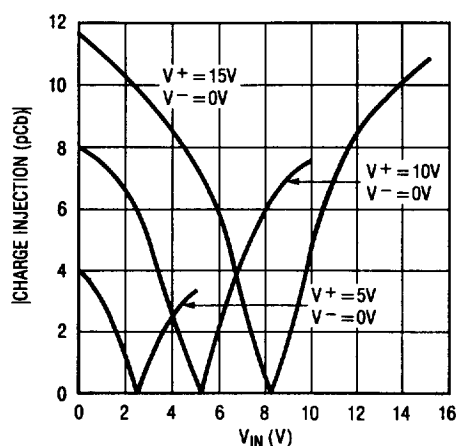


Figure 4. Individual Switch Charge Injection vs Input Voltage

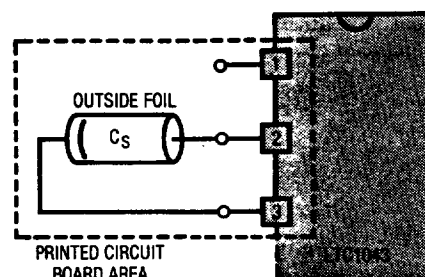


Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

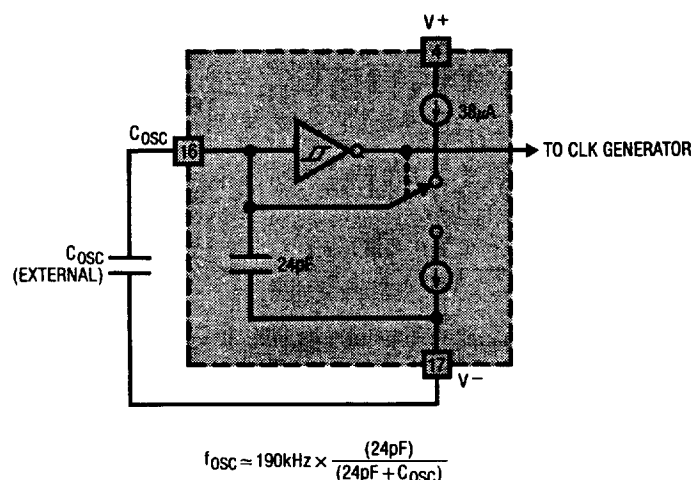
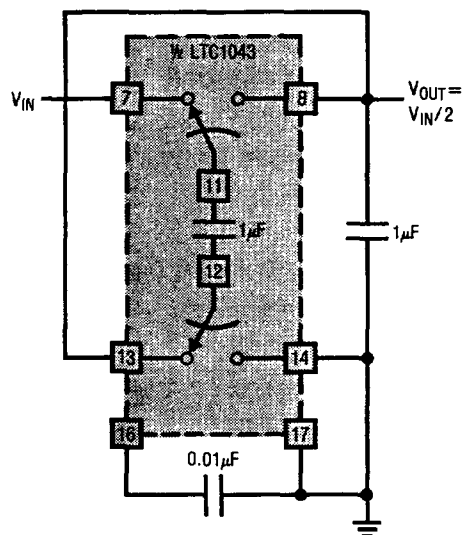


Figure 6. Internal Oscillator

APPLICATIONS

Divide by 2

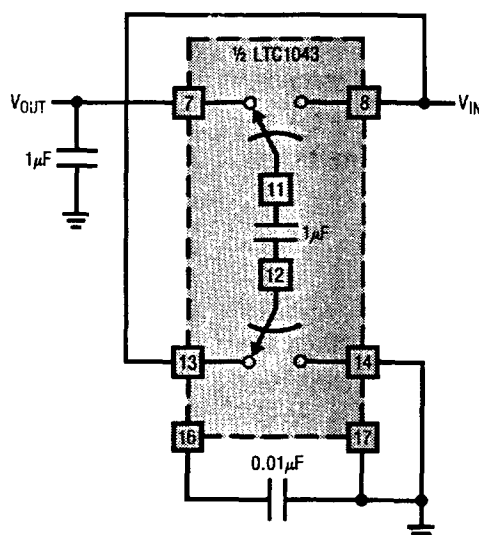


$$V_{OUT} = V_{IN}/2 \pm 1\text{ppm}$$

$$0 \leq V_{IN} \leq V^+$$

$$3 \leq V^+ \leq 18\text{V}$$

Multiply by 2

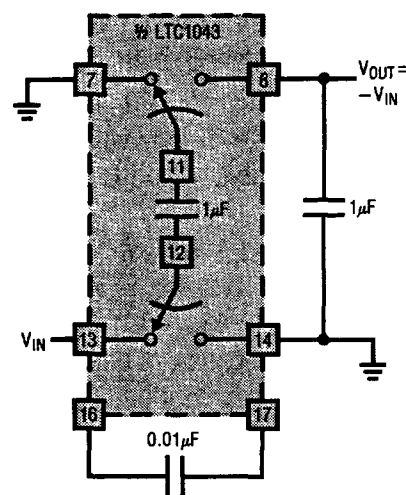


$$V_{OUT} = 2V_{IN} \pm 5\text{ppm}$$

$$0 \leq V_{IN} < V^+ / 2$$

$$3 \leq V^+ \leq 18\text{V}$$

Ultra Precision Voltage Inverter

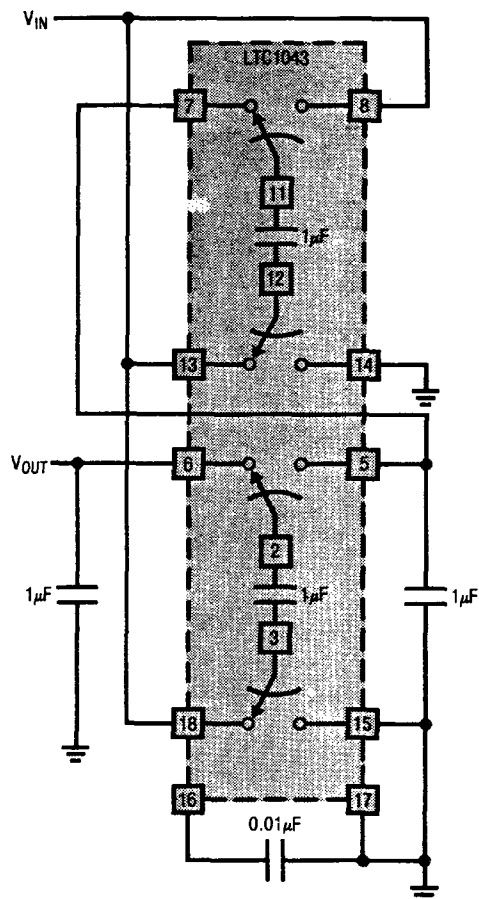


$$V_{OUT} = -V_{IN} \pm 2\text{ppm}$$

$$V^- < V_{IN} < V^+$$

$$V^+ = +5\text{V}, V^- = -5\text{V}$$

Precision Multiply by 3

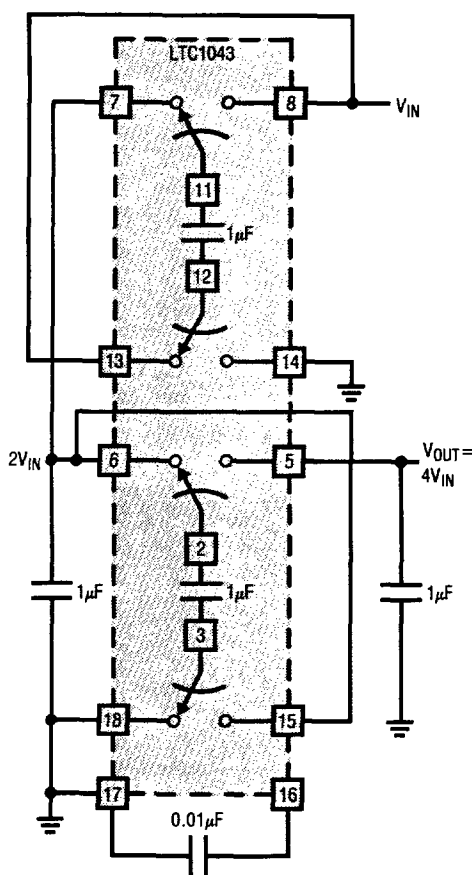


$$V_{OUT} = 3V_{IN} \pm 10\text{ppm}$$

$$0 < V_{IN} < V^+ / 3$$

$$3\text{V} < V^+ < 18\text{V}$$

Precision Multiply by 4

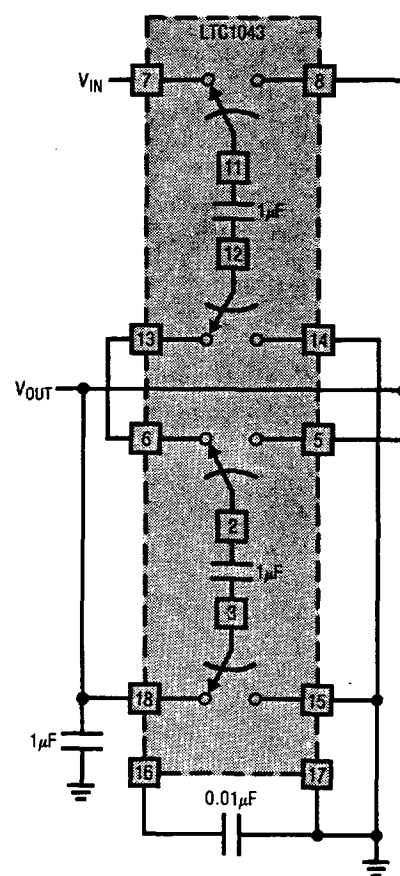


$$V_{OUT} = 4V_{IN} \pm 40\text{ppm}$$

$$0 \leq V_{IN} \leq V^+ / 4$$

$$3\text{V} < V^+ < 18\text{V}$$

Divide by 3

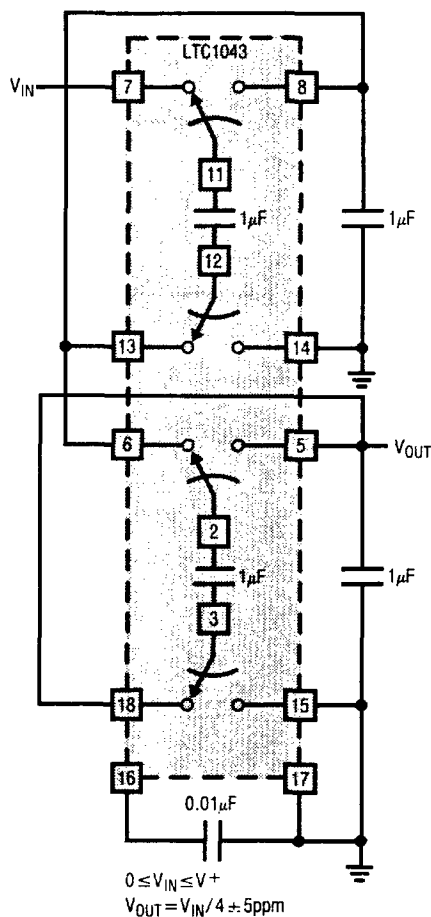


$$V_{OUT} = V_{IN}/3 \pm 3\text{ppm}$$

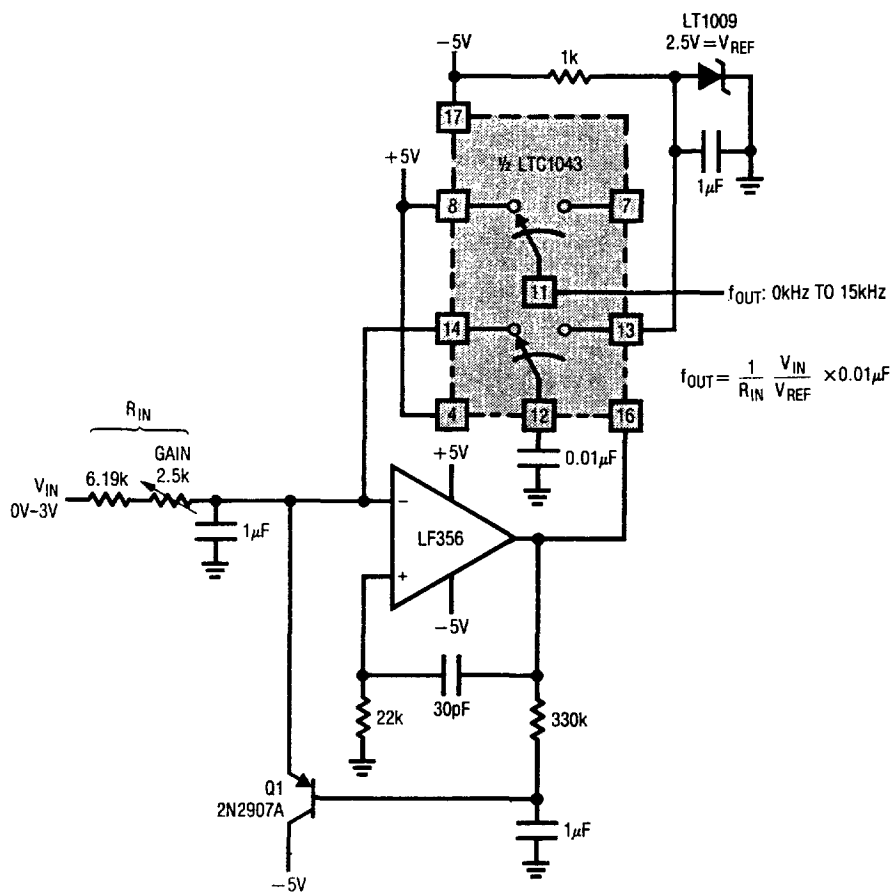
$$0 \leq V_{IN} \leq V^+$$

APPLICATIONS

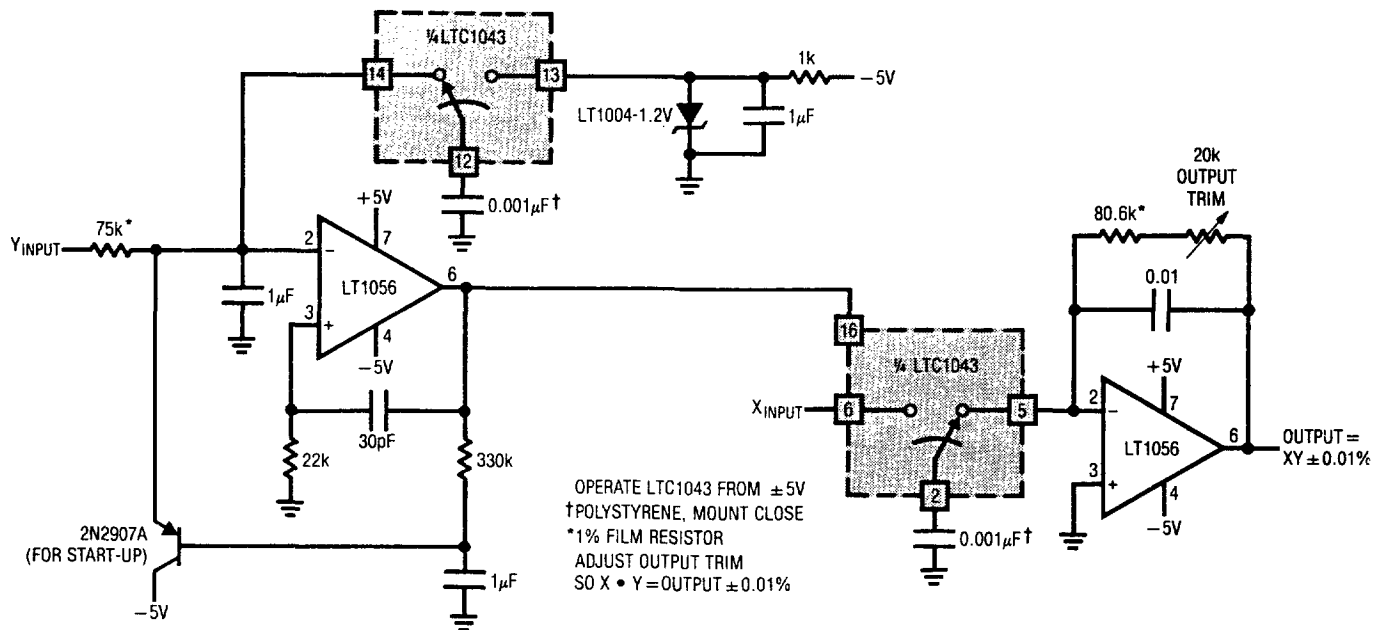
Divide by 4



0.005% V → F Converter

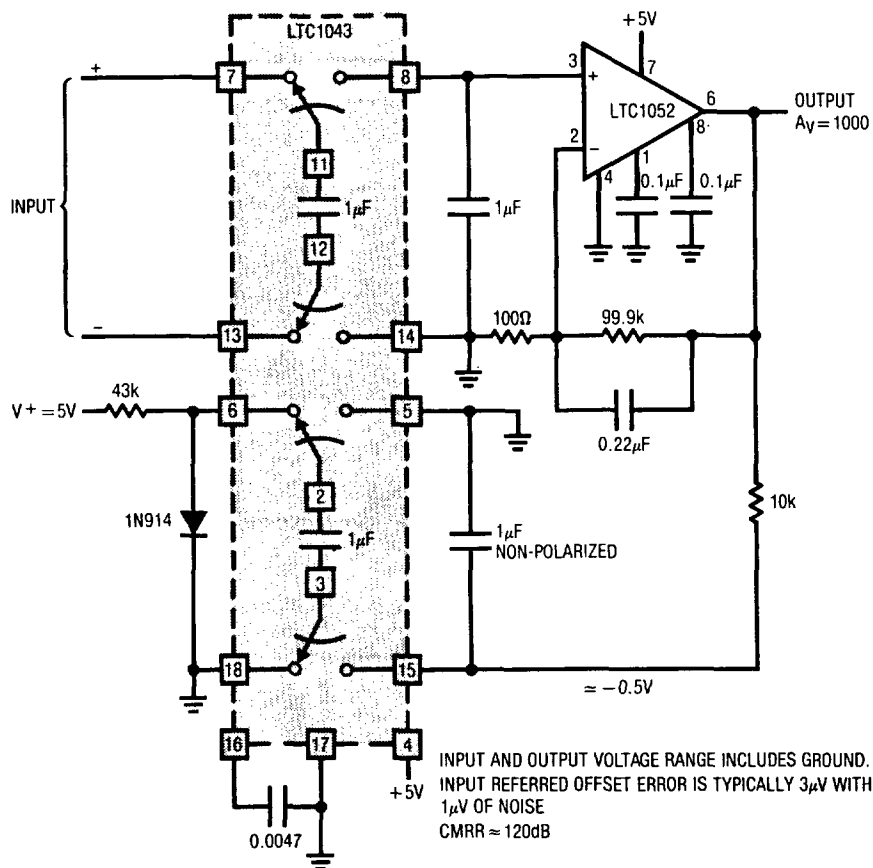


0.01% Analog Multiplier

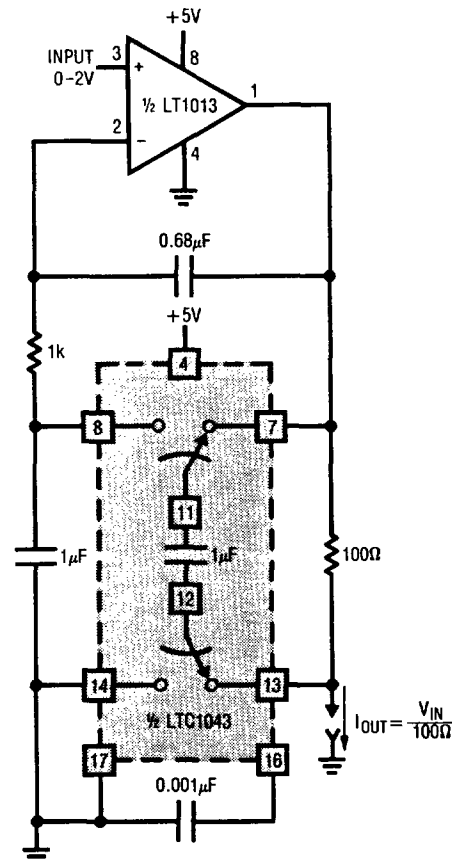


APPLICATIONS

Single 5V Supply, Ultra Precision Instrumentation Amplifier

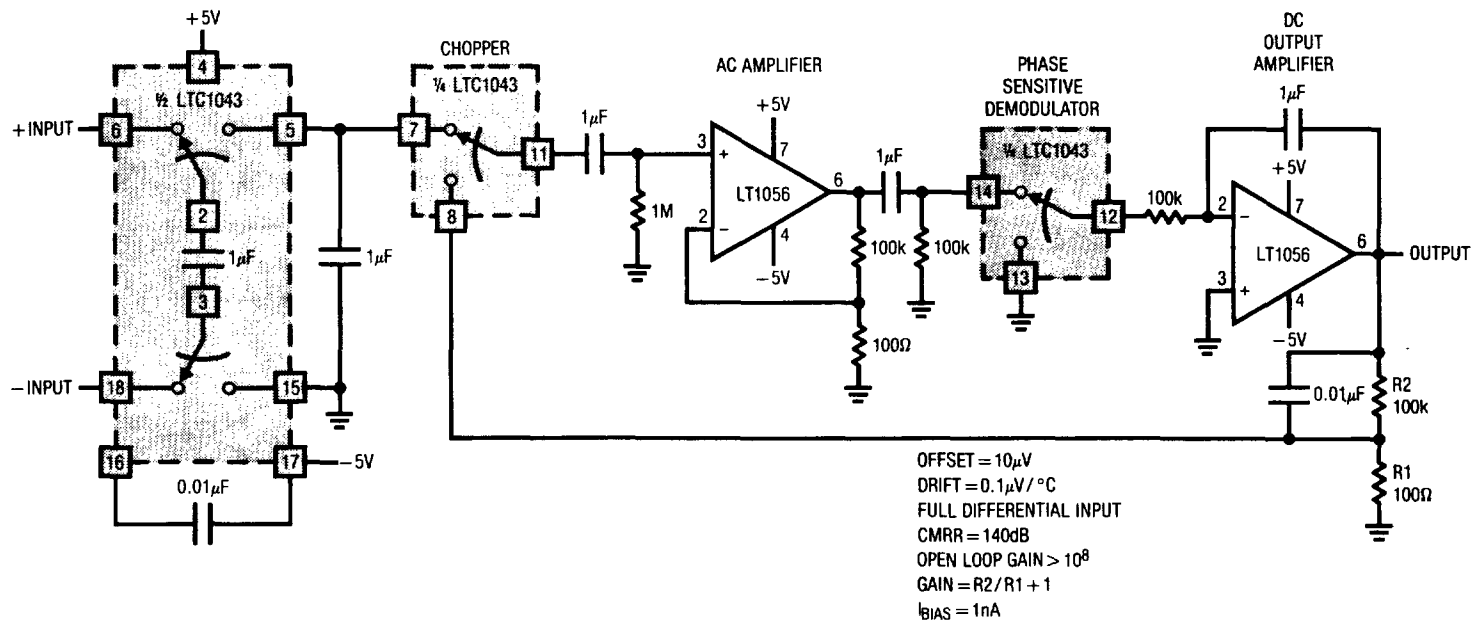


Voltage Controlled Current Source with Ground Referred Input and Output



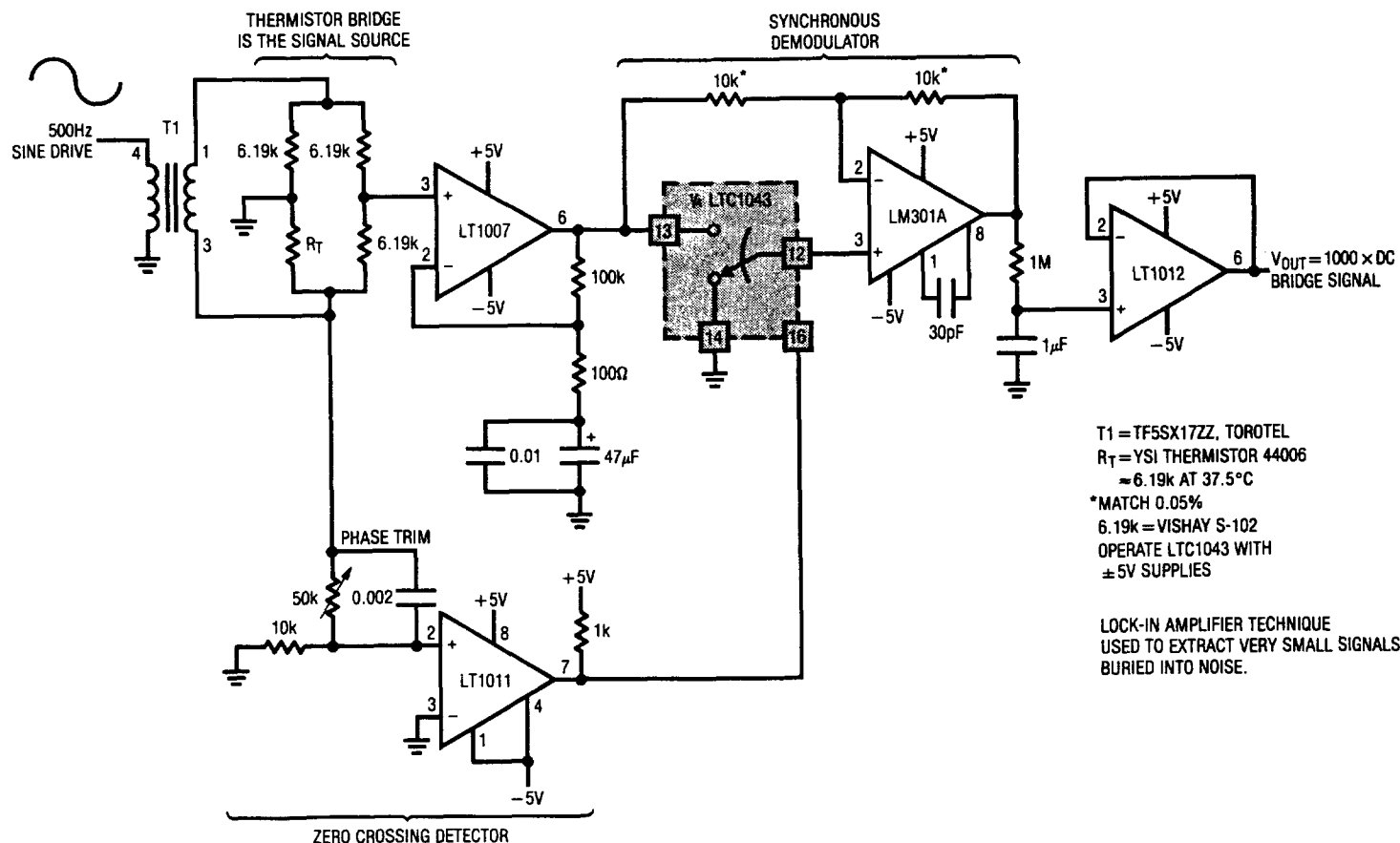
OPERATES FROM A SINGLE 5V SUPPLY

Precision Instrumentation Amplifier

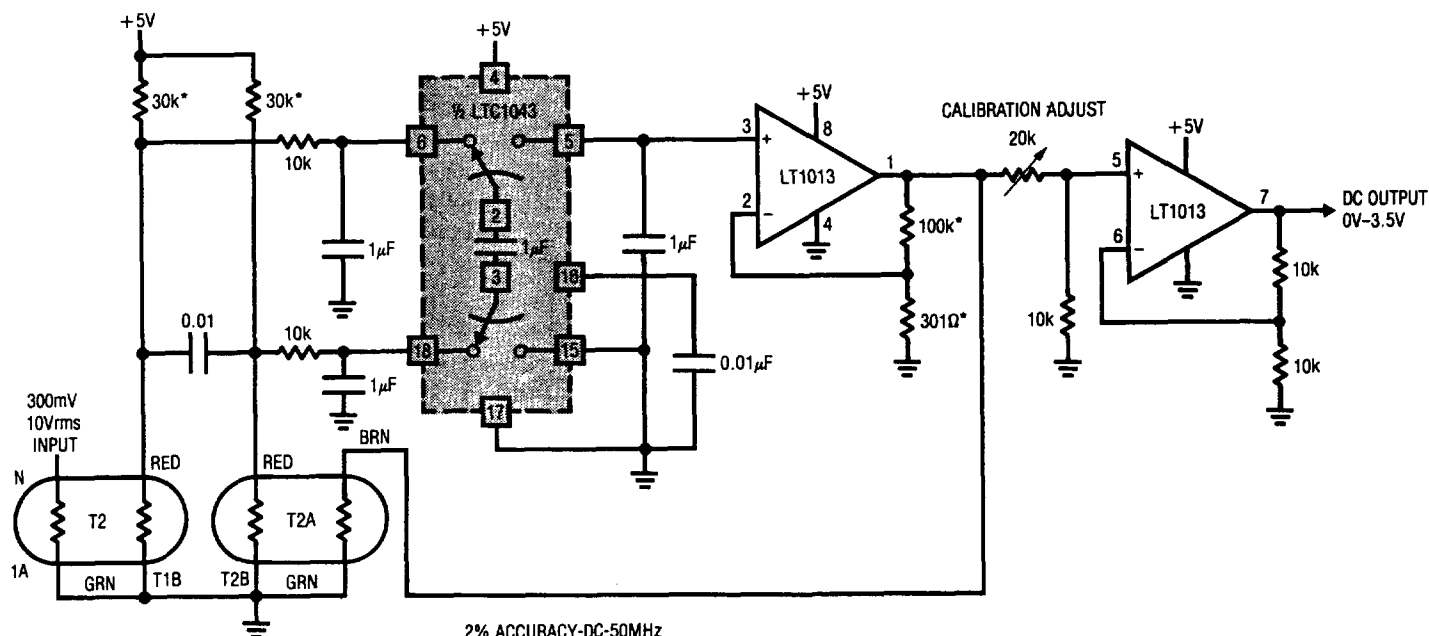


APPLICATIONS

Lock-In Amplifier (= Extremely Narrow-Band Amplifier)



50MHz Thermal rms → DC Converter

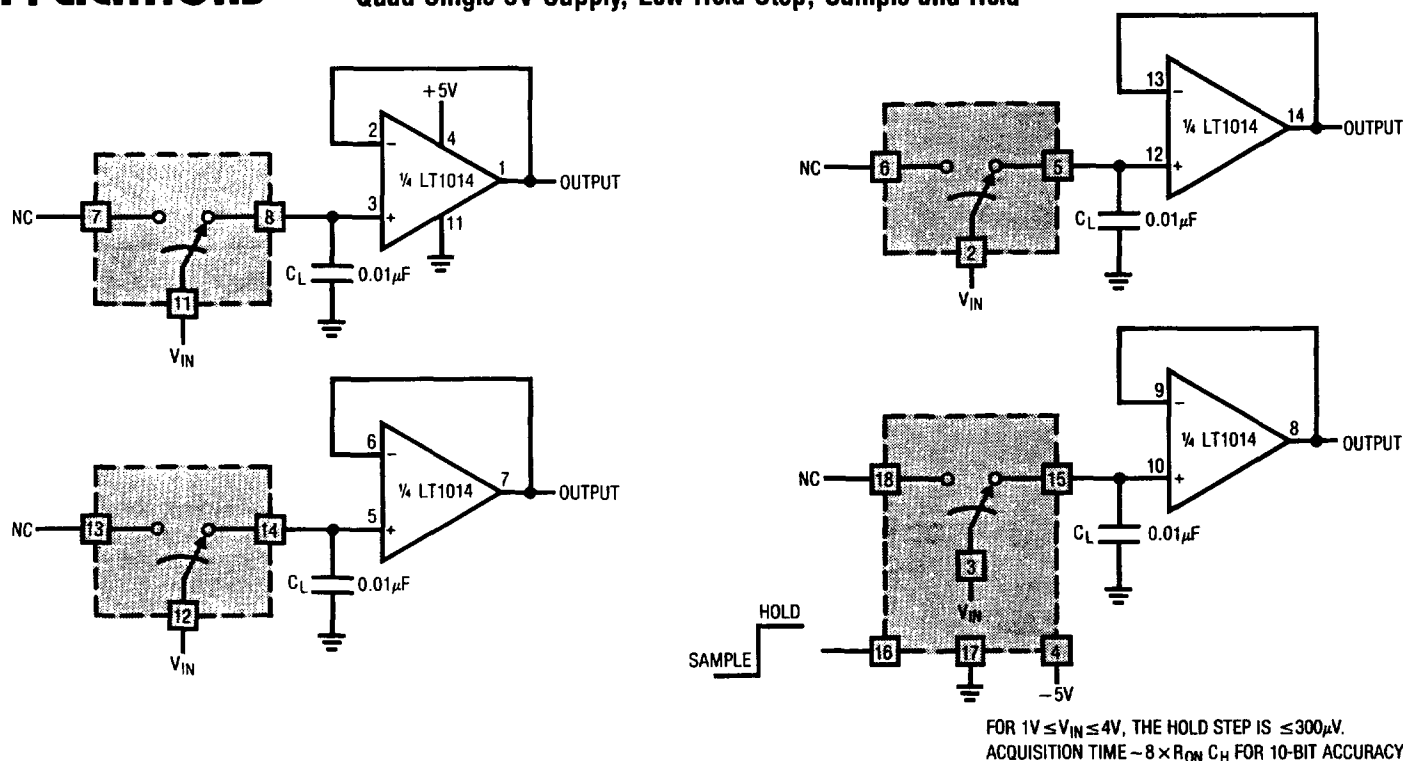


2% ACCURACY-DC-50MHz
 100:1 CREST FACTOR CAPABILITY
 T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE
 ENCLOSE T1 AND T2 IN STYROFOAM

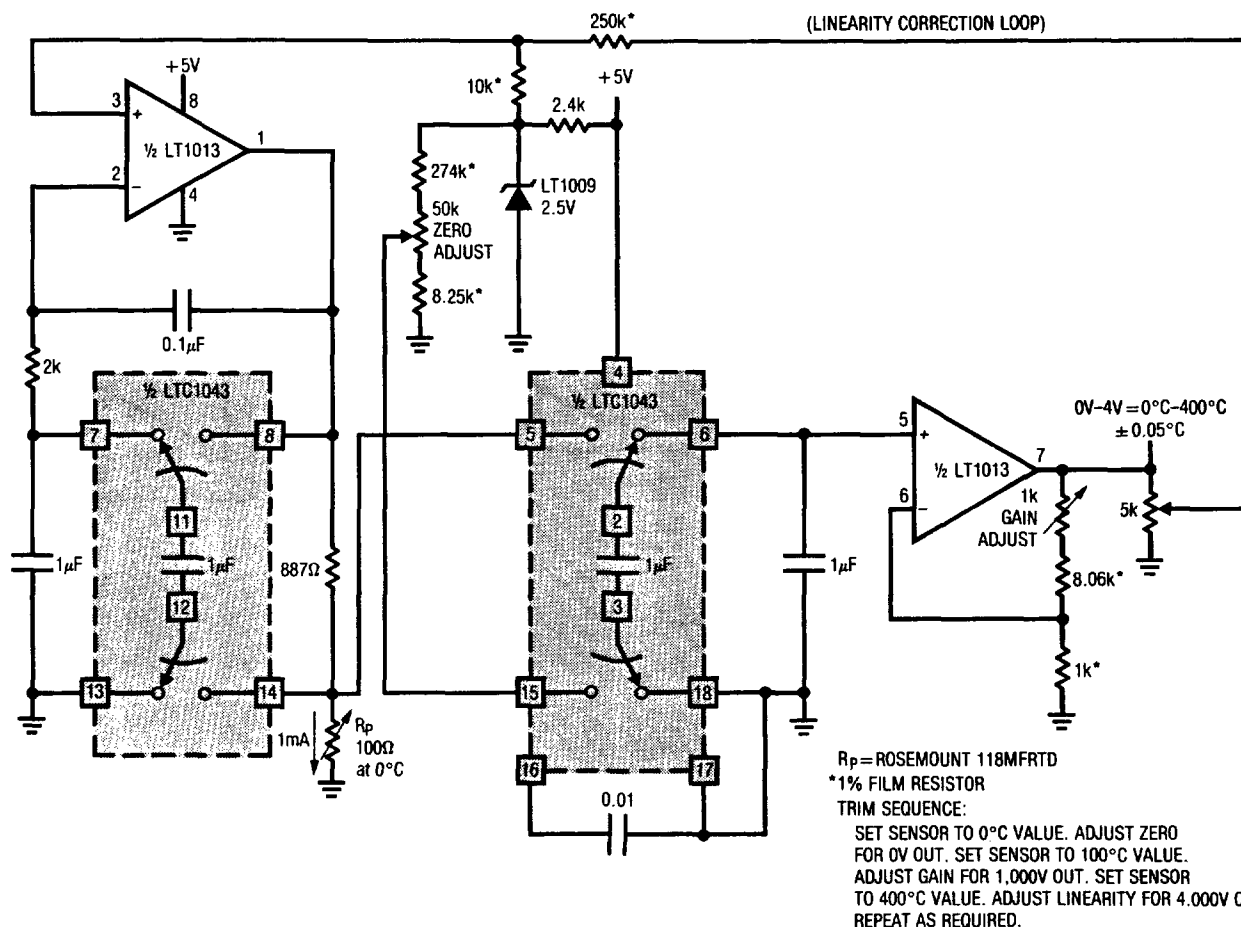
*1% RESISTOR

APPLICATIONS

Quad Single 5V Supply, Low Hold Step, Sample and Hold



Single Supply Precision Linearized Platinum RTD Signal Conditioner



APPLICATIONS

The circuit diagram illustrates a variable Q bandpass filter. It consists of two LTC1043 integrated circuits, each containing a variable capacitor (C1, C2) and a fixed capacitor (C3, C4). The filter is powered by a +5V and -5V supply. The input signal V_{IN} is connected to the non-inverting input of the first LT1056 op-amp (U1) through a 10k resistor R_{IN} . The output of U1 is connected to the input of the first LTC1043 (U2) at pin 7. The output of U2 is connected to the input of the second LT1056 op-amp (U3) at pin 14. The output of U3 is connected to the input of the second LTC1043 (U4) at pin 15. The output of U4 is connected to the output of the filter. The filter's center frequency f_0 is determined by the clock input f_{CLK} and the resistor ratio R_0/R_1 . The filter's Q factor is determined by the resistor ratio R_0/R_1 . The filter's bandwidth is determined by the resistor ratio R_0/R_1 .

BANDPASS CENTER FREQUENCY $f_0 = \frac{f_{CLK}}{31.4} \times \sqrt{\frac{R_2}{R_1}}$

BANDPASS GAIN AT f_0 IS: R_0/R_1

$Q = R_2 \sqrt{R_1}$

$f_0 \text{ MAX} \leq 100\text{kHz}$

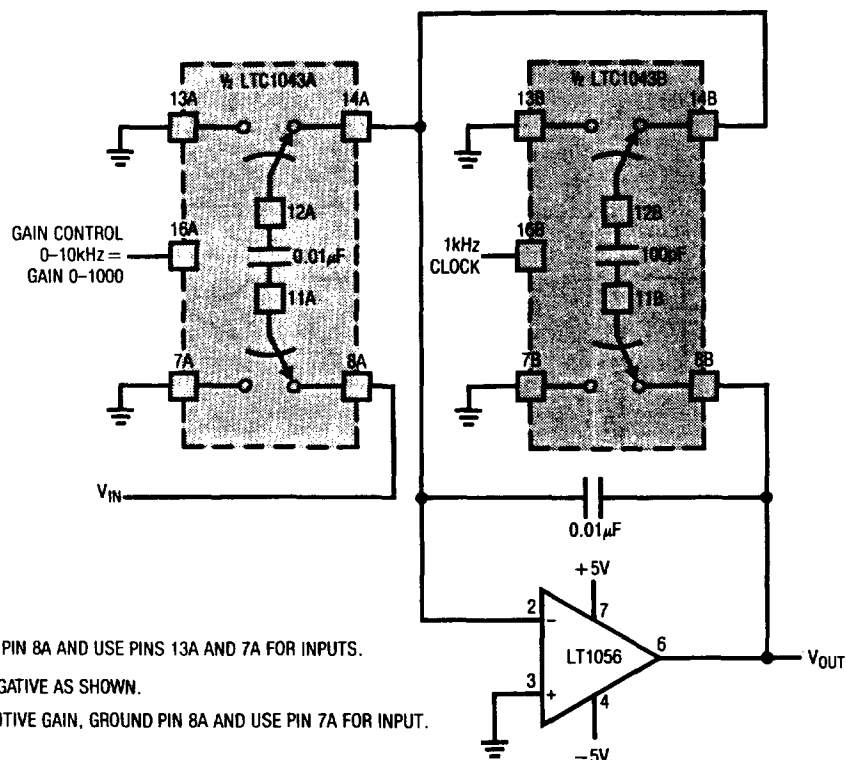
$Q \text{ MAX AT } 100\text{kHz } f_0 \text{ IS } \leq 10$

$(f_0 \times Q) \text{ MAX} \leq 1\text{MHz}$

$f_{CLK} \text{ MAX} \leq 3\text{MHz}, Q < 2$

APPLICATIONS

Frequency-Controlled Gain Amplifier

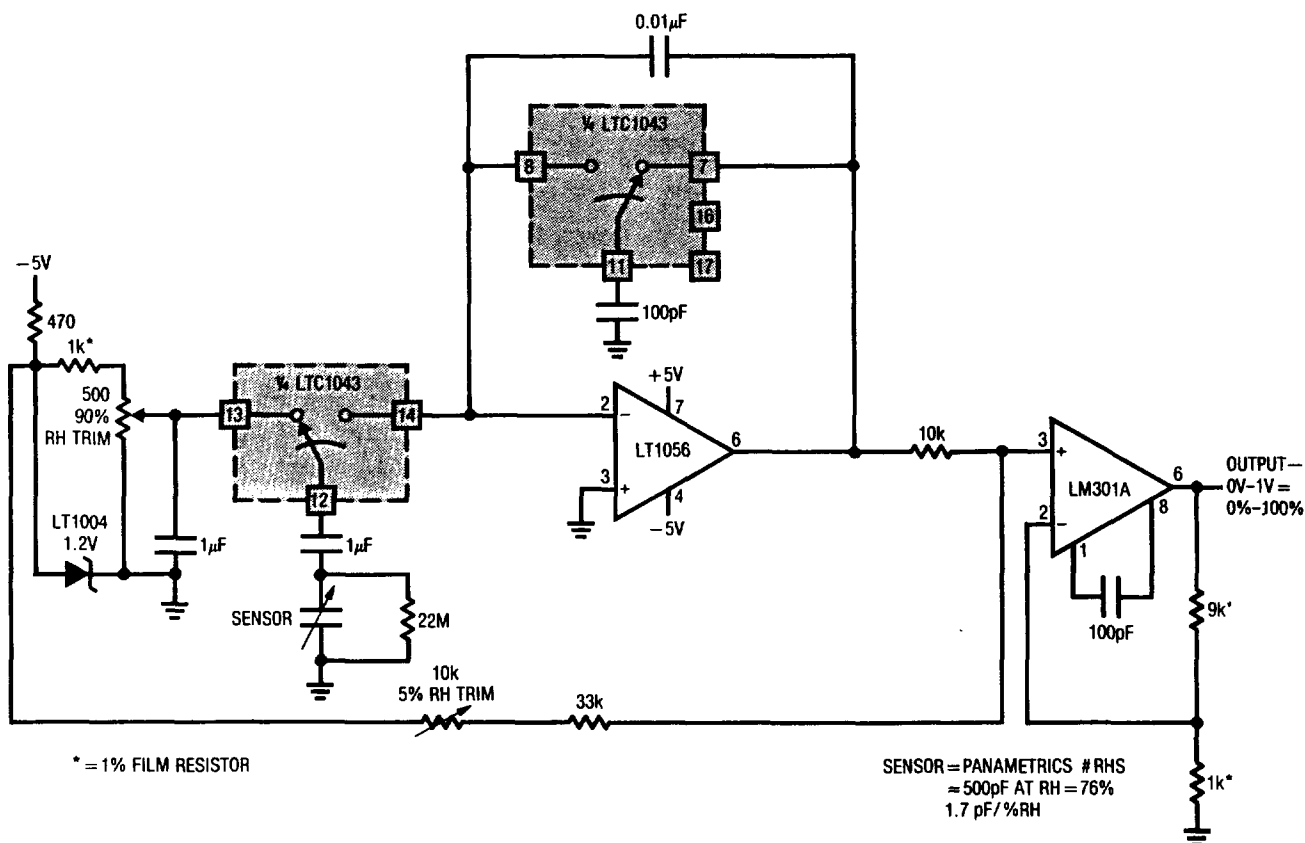


FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS.

$GAIN = \frac{f_{IN} \times 0.01\mu F}{1kHz \times 100pF}$; GAIN IS NEGATIVE AS SHOWN.

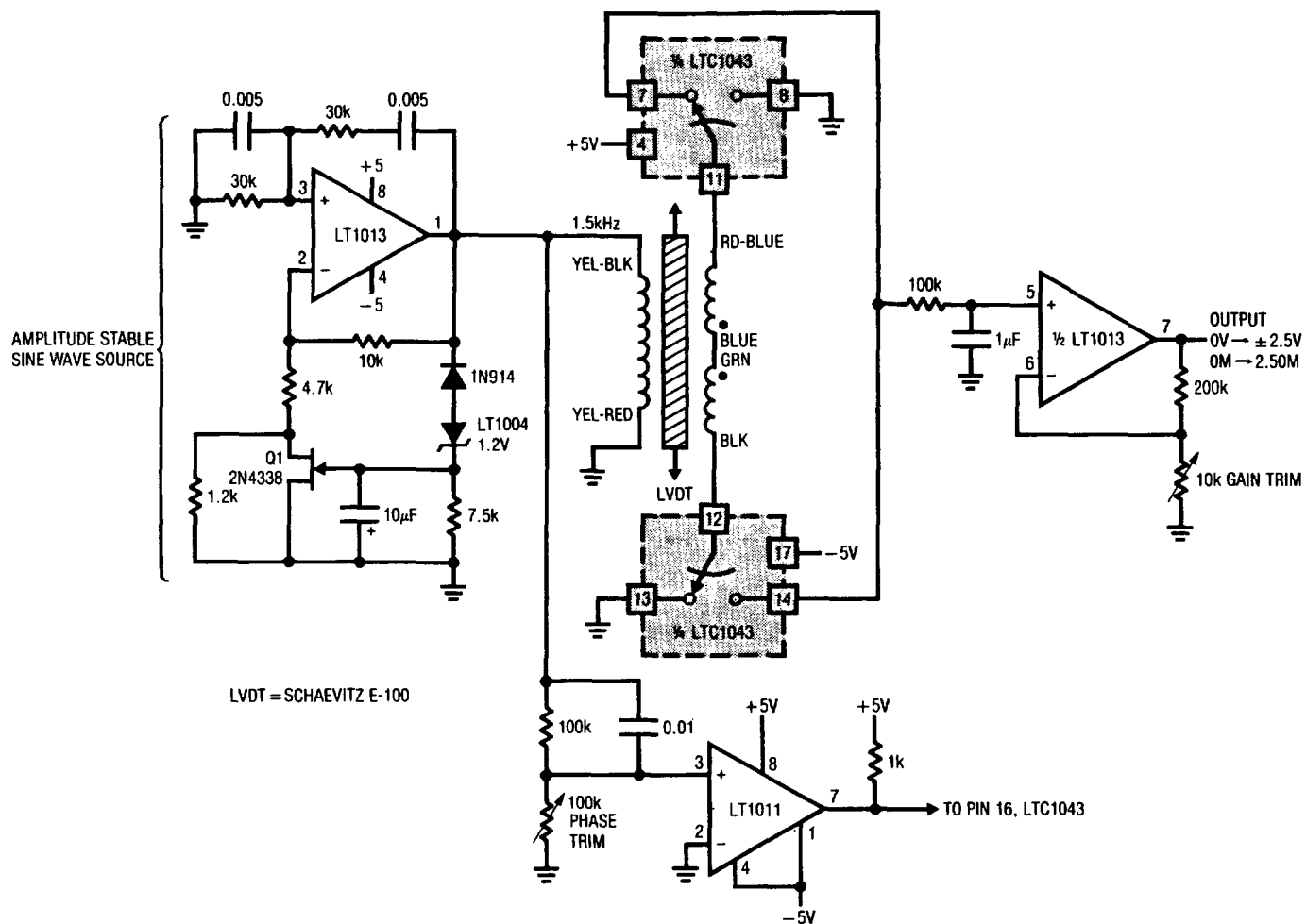
FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT. USE $\pm 5V$ SUPPLIES FOR LTC1043.

Relative Humidity Sensor Signal Conditioner

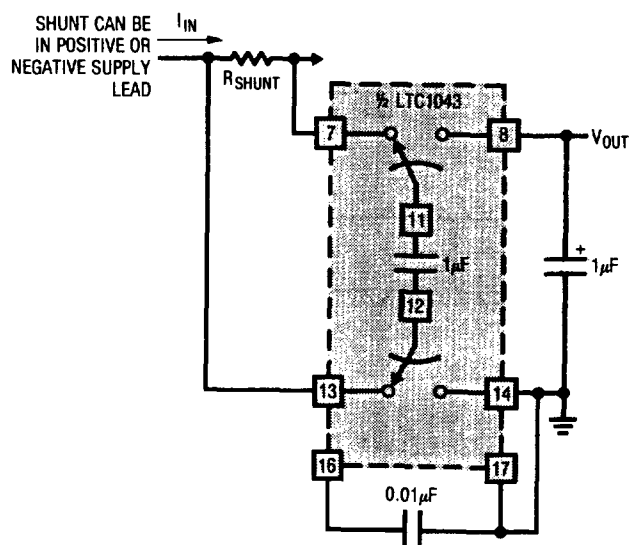


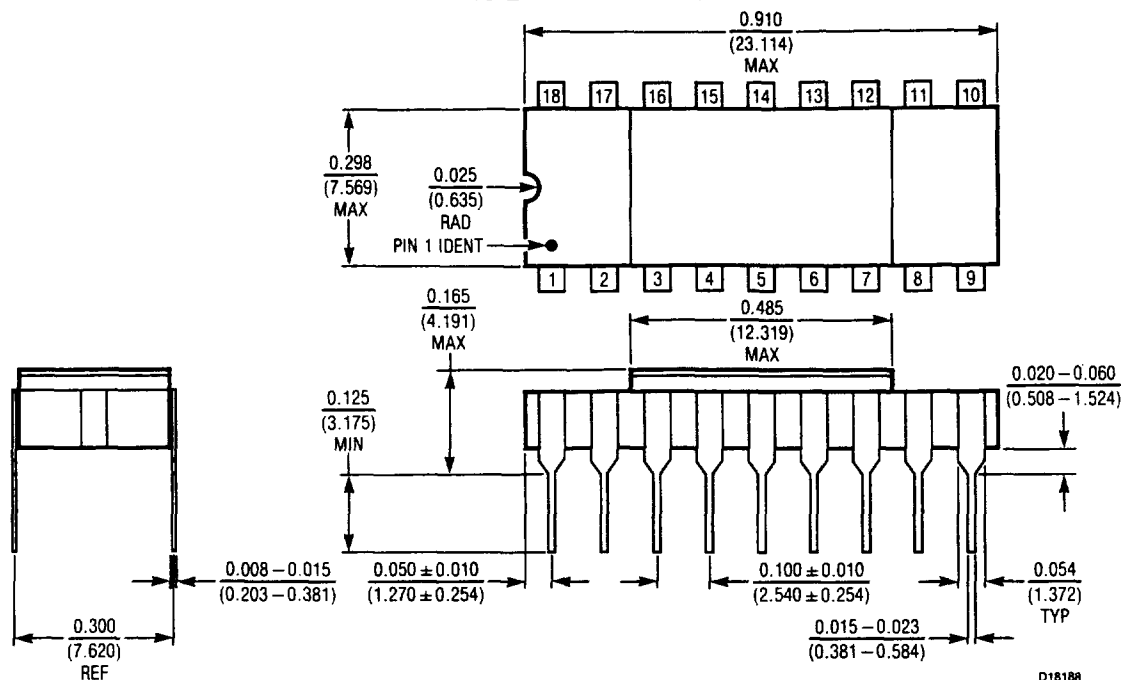
APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner



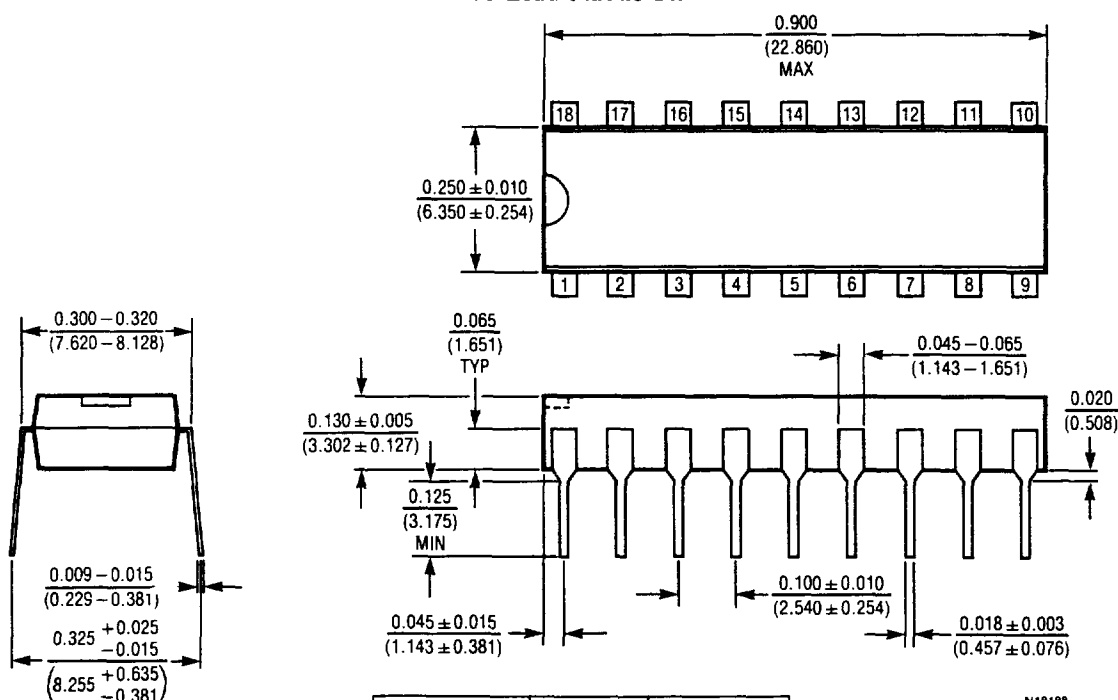
Precision Current Sensing in Supply Rails



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.**D Package**
18 Lead Side Brazed

D18188

	T_{jmax}	θ_{ja}
LTC1043MD	150°C	100°C/W
LTC1043CD	150°C	100°C/W

N Package
18 Lead Plastic DIP

N18188

	T_{jmax}	θ_{ja}
LTC1043CN	100°C	100°C/W