

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3483 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 52 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 14 \text{ A)}$
 $R_{DS(on)2} = 59 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 14 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2300 \text{ pF TYP.}$
- Built-in gate protection diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	100	V
Gate to Source Voltage ($V_{DS} = 0\text{V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 28	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 60	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	40	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	25	A
Single Avalanche Energy ^{Note2}	E_{AS}	62.5	mJ

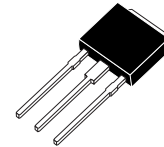
Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

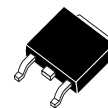
★ ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3483	TO-251 (MP-3)
2SK3483-Z	TO-252 (MP-3Z)

(TO-251)



(TO-252)



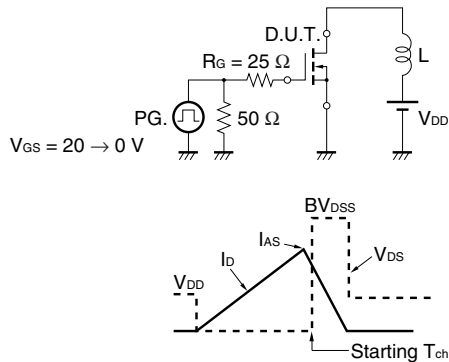
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

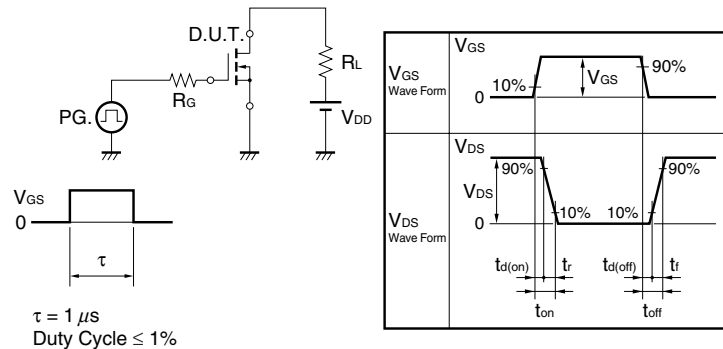
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 14 A	9.0	18		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 14 A		41	52	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 14 A		45	59	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2300		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		230		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		120		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 50 V, I _D = 14 A		12		ns
Rise Time	t _r	V _{GS} = 10 V		9		ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		53		ns
Fall Time	t _f			5		ns
Total Gate Charge	Q _G	V _{DD} = 80 V		49		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		7		nC
Gate to Drain Charge	Q _{GD}	I _D = 28 A		13		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 28 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 28 A, V _{GS} = 0 V		73		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		175		nC

Note Pulsed

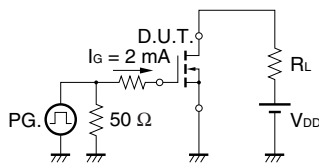
TEST CIRCUIT 1 AVALANCHE CAPABILITY



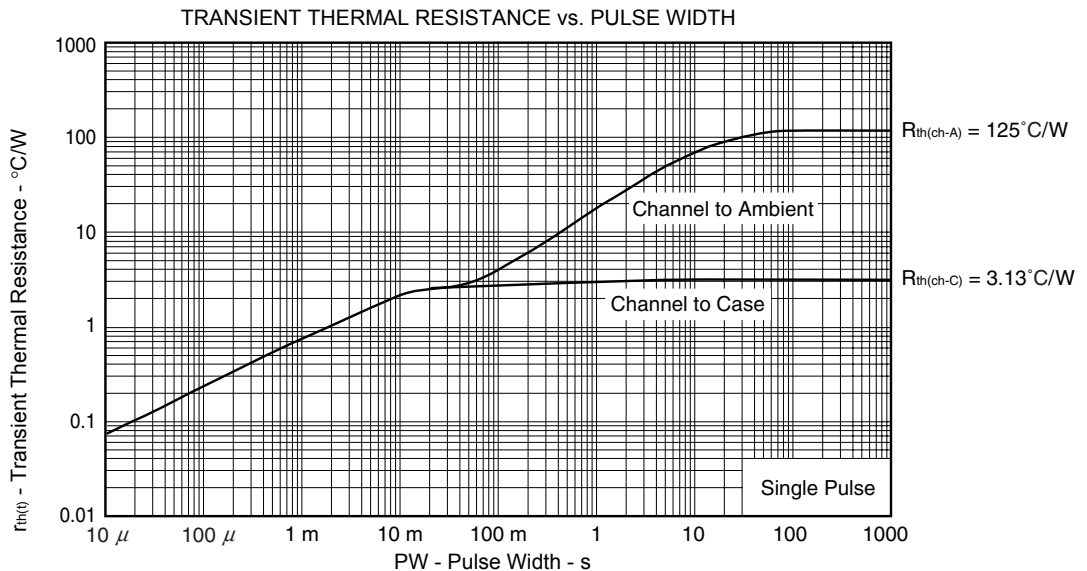
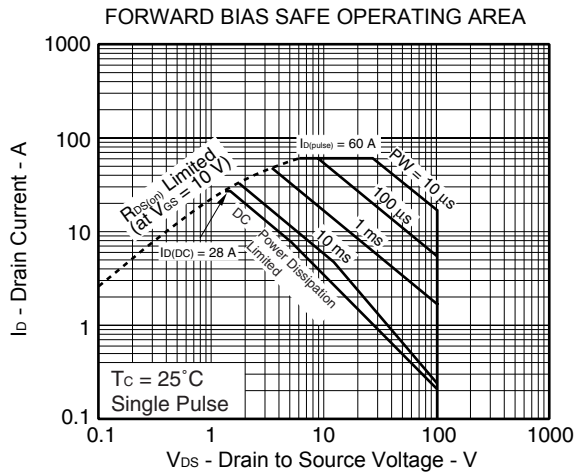
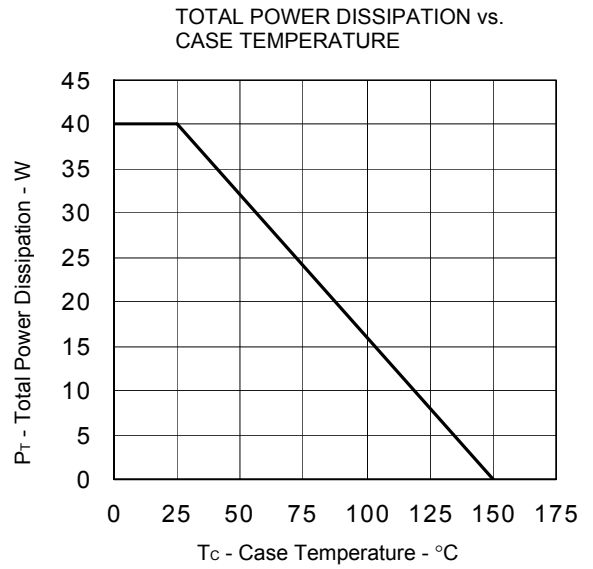
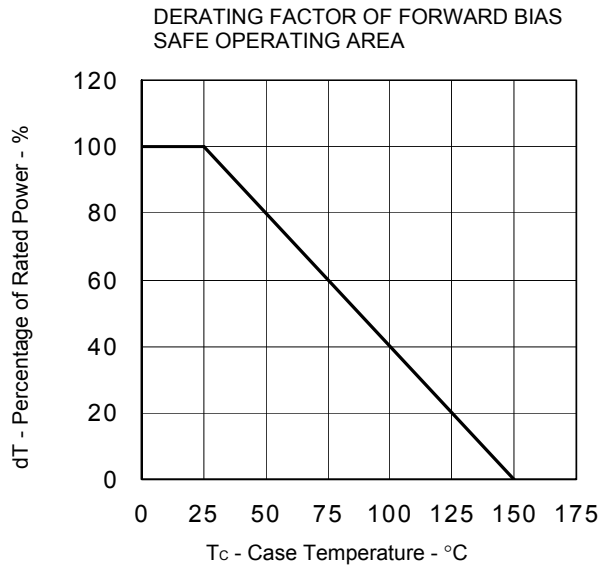
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

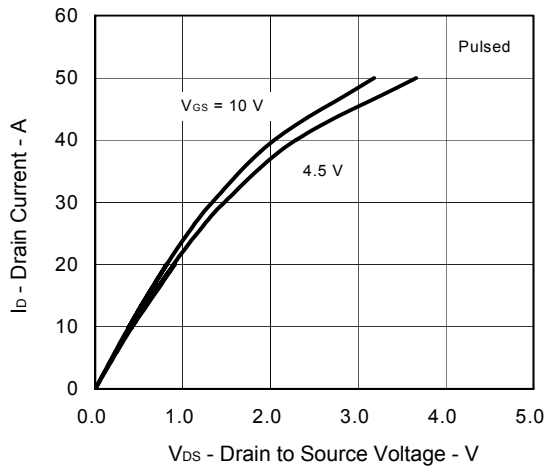


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TYPICAL CHARACTERISTICS (TA = 25°C)

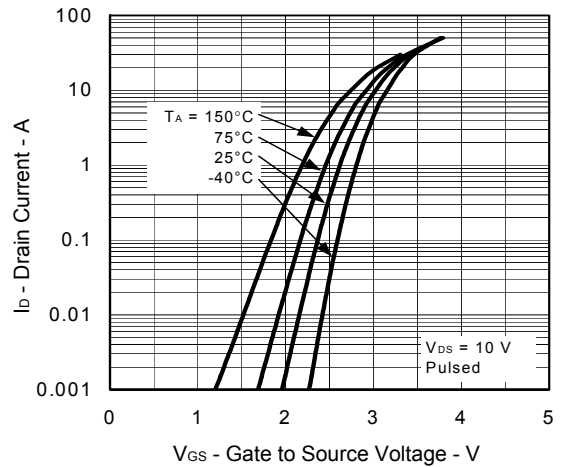


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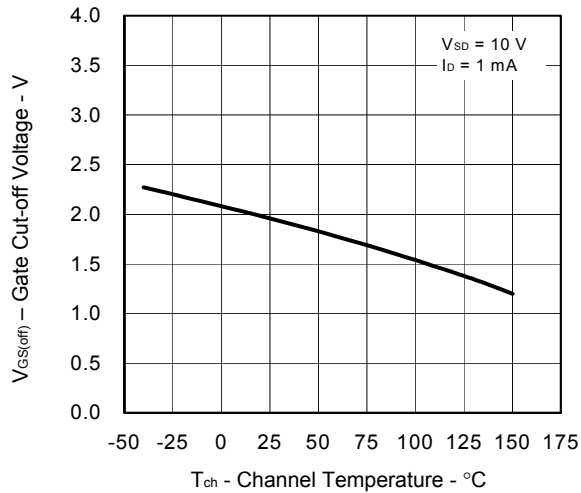
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



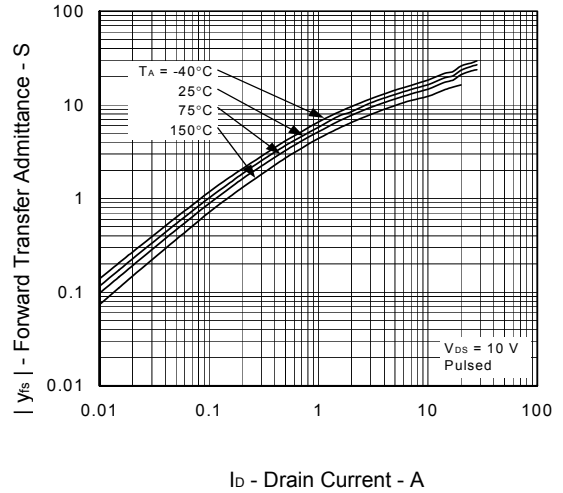
FORWARD TRANSFER CHARACTERISTICS



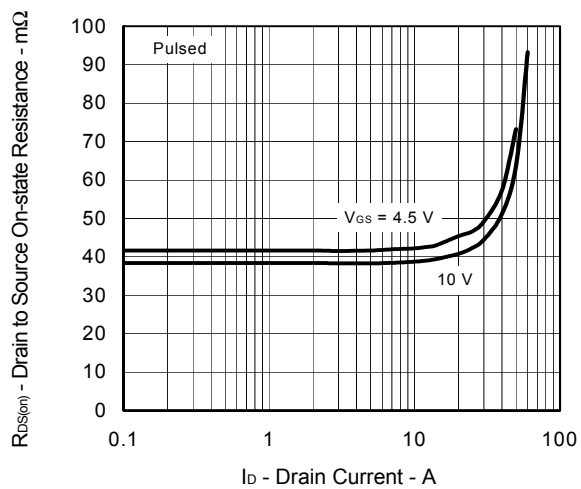
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



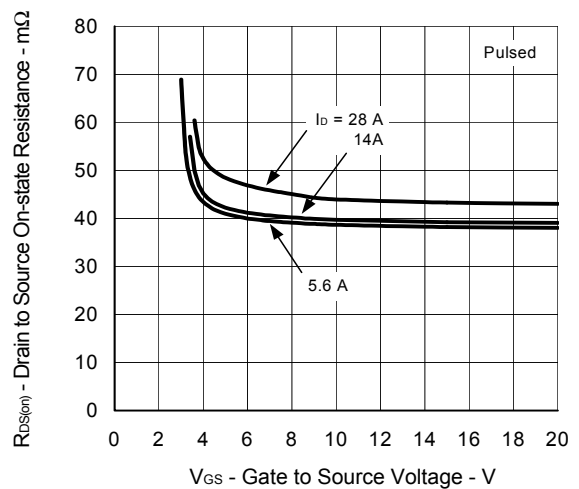
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

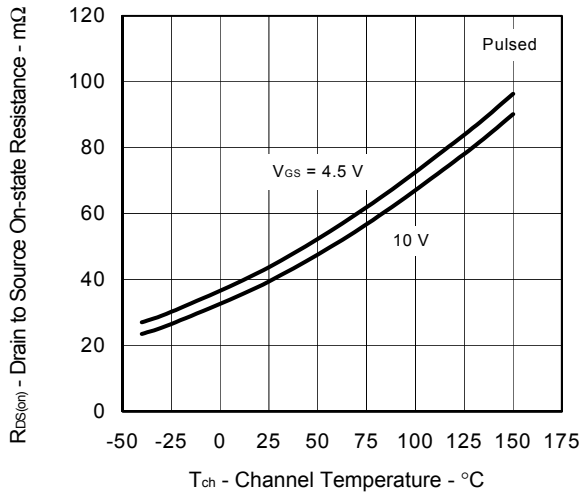


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

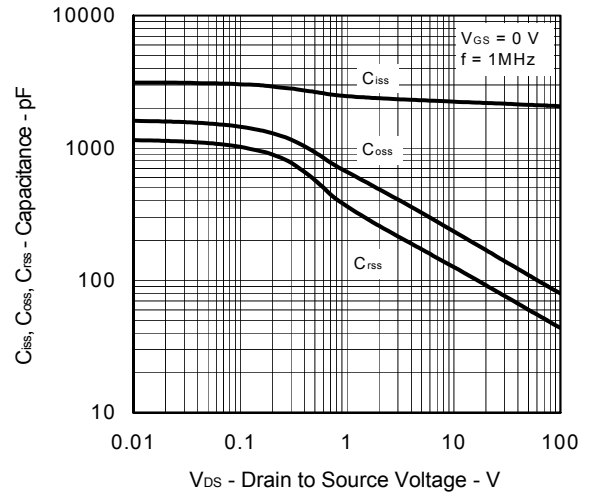


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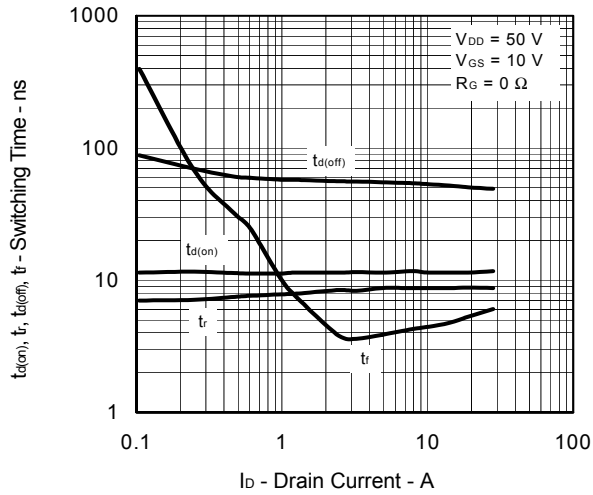
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



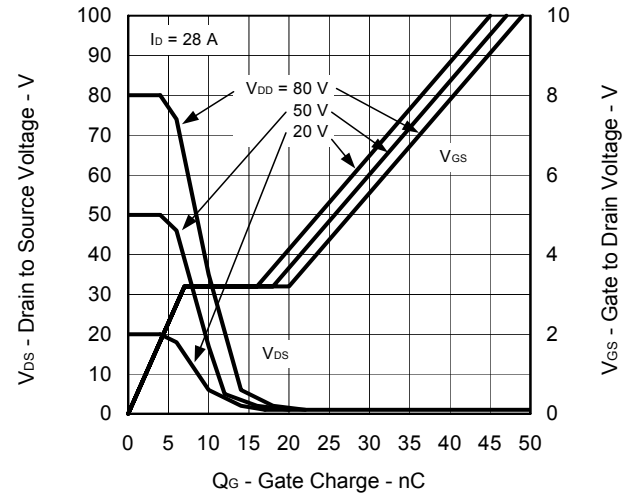
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



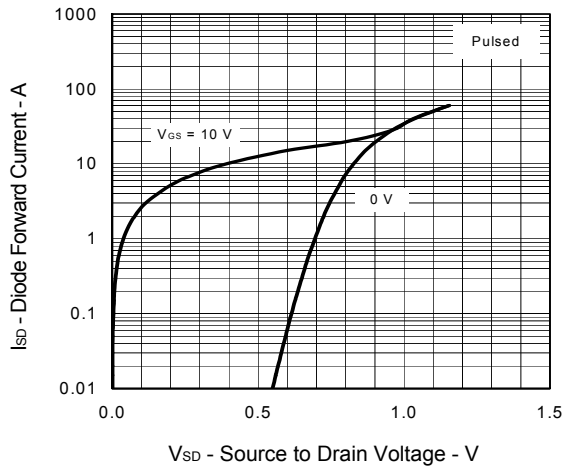
SWITCHING CHARACTERISTICS



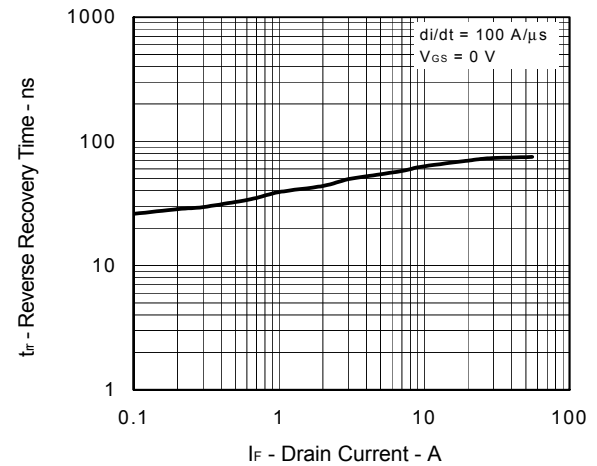
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

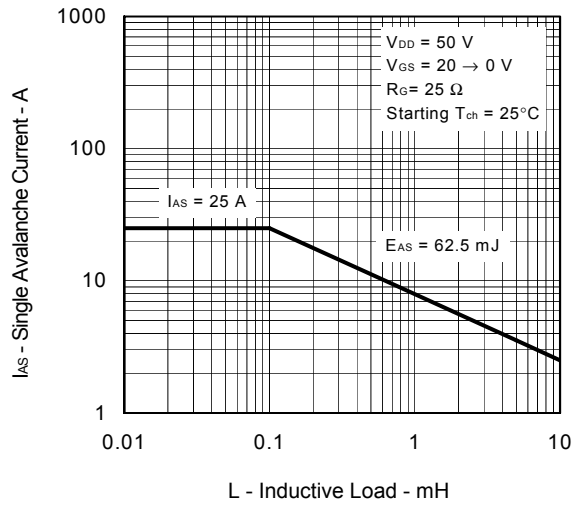


REVERSE RECOVERY TIME vs. DRAIN CURRENT

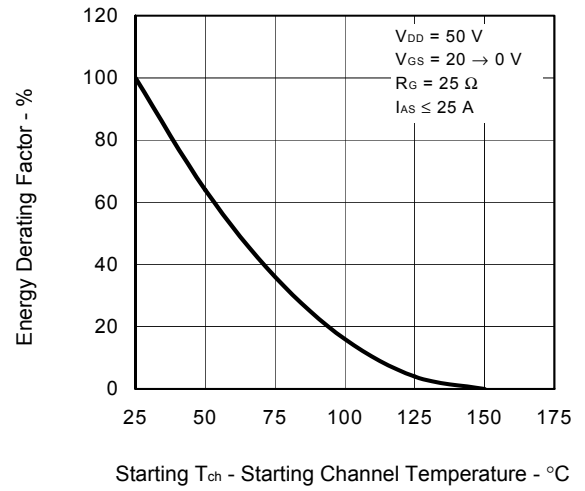


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SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

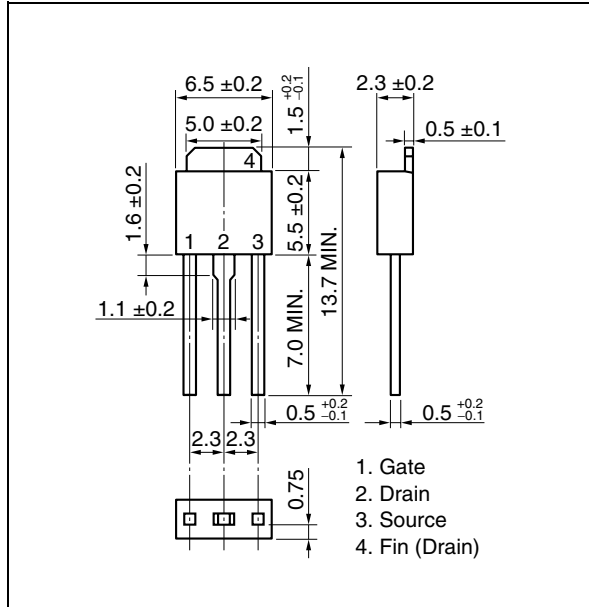


SINGLE AVALANCHE ENERGY DERATING FACTOR

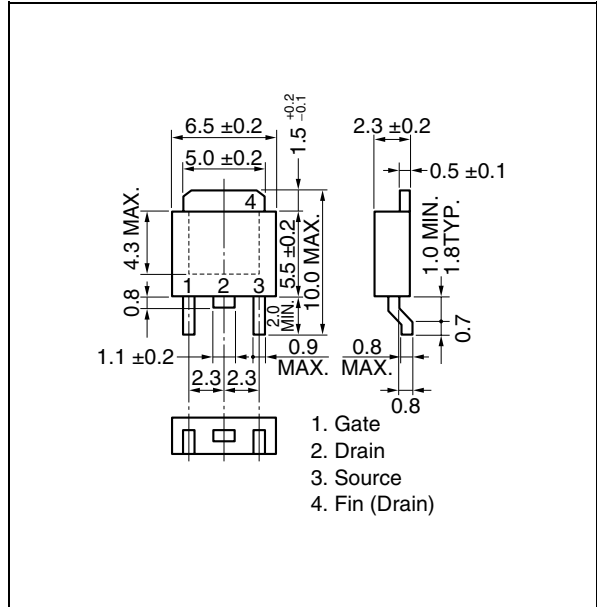


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PACKAGE DRAWINGS (Unit: mm)

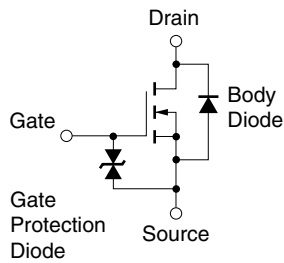
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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