19-2578; Rev 0; 10/02

Single/Dual LVDS Line Receivers with "In-Path" Fail-Safe

General Description

The MAX9171/MAX9172 single/dual low-voltage differential signaling (LVDS) receivers are designed for high-speed applications requiring minimum power consumption, space, and noise. Both devices support switching rates exceeding 500Mbps while operating from a single 3.3V supply.

The MAX9171 is a single LVDS receiver and the MAX9172 is a dual LVDS receiver. Both devices conform to the ANSI TIA/EIA-644 LVDS standard and convert LVDS to LVTTL/LVCMOS-compatible outputs. A fail-safe feature sets the outputs high when the inputs are undriven and open, terminated, or shorted. The MAX9171/MAX9172 are available in 8-pin SO packages and space-saving thin QFN and SOT23 packages.

For lower skew devices, refer to the MAX9111/ MAX9113 data sheet.

Applications

Multipoint Backplane Interconnect

Laser Printers

Digital Copiers

Cellular Phone Base Stations

LCD Displays

Network Switches/Routers

Clock Distribution

Features

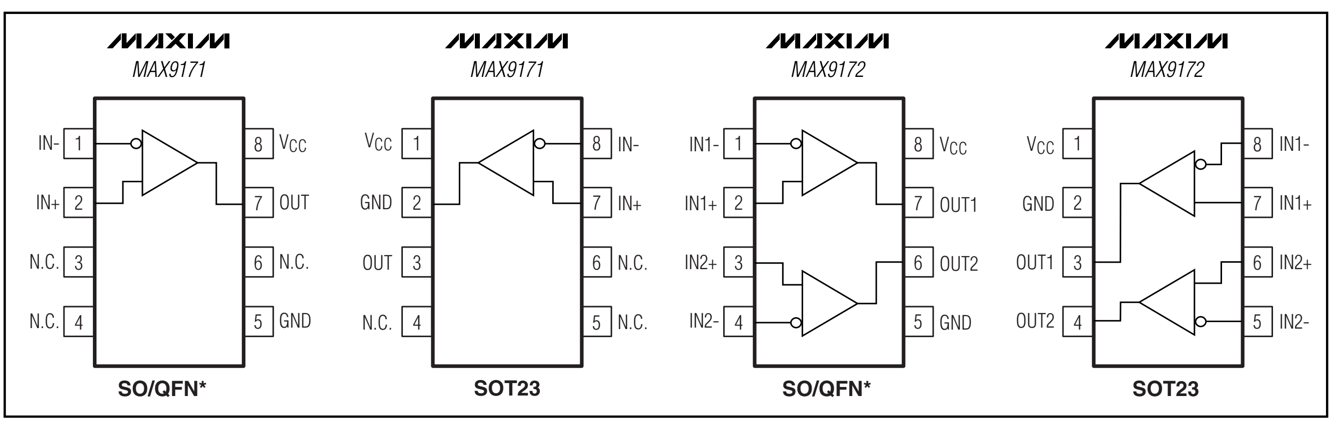
- ♦ **Input Accepts LVDS and LVPECL**
- ♦ **In-Path Fail-Safe Circuit**
- ♦ **Space-Saving 8-Pin QFN and SOT23 Packages**
- ♦ **Fail-Safe Circuitry Sets Output High for Open, Undriven Shorted, or Undriven Terminated Output**
- ♦ **Flow-Through Pinout Simplifies PC Board Layout**
- ♦ **Guaranteed 500Mbps Data Rate**
- ♦ **Second Source to DS90LV018A and DS90LV028A (SO Packages Only)**
- ♦ **Conforms to ANSI TIA/EIA-644 Standard**
- ♦ **3.3V Supply Voltage**
- ♦ **-40°C to +85°C Operating Temperature Range**
- ♦ **Low Power Dissipation**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9171EKA-T	-40°C to +85°C	8 SOT23-8	AALX
MAX9171ESA	-40°C to +85°C	8 SO	—
MAX9171ETA*	-40°C to +85°C	8 Thin QFN	—
MAX9172EKA-T	-40°C to +85°C	8 SOT23-8	AALY
MAX9172ESA	-40°C to +85°C	8 SO	—
MAX9172ETA*	-40°C to +85°C	8 Thin QFN	—

**Future product—contact factory for availability.*

Pin Configurations



Single/Dual LVDS Line Receivers with "In-Path" Fail-Safe

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +4.0V
IN_+, IN_- to GND ....-0.3V to +4.0V
OUT_ to GND ....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C) 714mW
8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
8-Pin QFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
ESD Protection
Human Body Model (IN_+, IN_-) ....±13kV
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, receiver input voltage = 0 to V_{CC}, common-mode voltage V_{CM} = $|V_{ID}/2|$ to (V_{CC} - $|V_{ID}/2|$), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS INPUTS (IN_+, IN_-)							
Differential Input High Threshold	V_{TH}	Figure 1			-40	0	mV
Differential Input Low Threshold	V_{TL}	Figure 1		-100	-40		mV
Input Current (Noninverting Input)	I_{IN+}	Figure 1		+0.5	-2.1	-5.0	µA
Power-Off Input Current (Noninverting Input)	I_{IN+OFF}	V_{IN+} = 0 to 3.6V, V_{IN-} = 0 to 3.6V, V_{CC} = 0 or open (Figure 1)		-0.5	0	+0.5	µA
Input Current (Inverting Input)	I_{IN-}	Figure 1		-0.5	+4.4	+10.0	µA
Power-Off Input Current (Inverting Input)	I_{IN-OFF}	V_{IN+} = 0 to 3.6V, V_{IN-} = 0 to 3.6V, V_{CC} = 0 or open (Figure 1)		-0.5	0	+0.5	µA
LVCMOS/LVTTL OUTPUTS (OUT_)							
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	Open, undriven short, or undriven parallel termination	2.7	3.2		V
			V_{ID} = 0V	2.7	3.2		
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA, V_{ID} = -100mV			0.1	0.4	V
Output Short-Circuit Current	I_{OS}	$V_{OUT\_}$ = 0 (Note 3)		-45	-77	-120	mA
POWER SUPPLY							
Supply Current	I_{CC}	Inputs open	MAX9171		3.6	6	mA
			MAX9172		7.0	9	

SWITCHING CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, C_L = 15pF, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 4, 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	Figures 2, 3	1.0	1.65	2.5	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figures 2, 3	1.0	1.62	2.5	ns
Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$	t_{SKD1}	Figures 2, 3 (Note 7)		30	400	ps
Differential Channel-to-Channel Skew (MAX9172)	t_{SKD2}	Figures 2, 3 (Note 8)		40	500	ps
Differential Part-to-Part Skew	t_{SKD3}	Figures 2, 3 (Note 9)			1	ns
	t_{SKD4}	Figures 2, 3 (Note 10)			1.5	
Rise Time	t_{TLH}	Figures 2, 3		0.55	0.8	ns
Fall Time	t_{THL}	Figures 2, 3		0.51	0.8	ps
Maximum Operating Frequency	f_{MAX}	All channels switching, $V_{OL(MAX)}$ = 0.4V, $V_{OH(MIN)}$ = 2.7V, 40% < duty cycle < 60%	250	300		MHz

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to GND except V_{TH}, V_{TL}, and V_{ID}.

Note 2: All devices are 100% production tested at T_A = +25°C and are guaranteed by design for T_A = -40°C to +85°C, as specified.

Note 3: Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

Note 4: AC parameters are guaranteed by design and not production tested.

Note 5: C_L includes scope probe and test jig capacitance.

Note 6: Pulse generator output conditions: $t_R = t_F$ < 1ns (0% to 100%), frequency = 250MHz, 50% duty cycle, V_{OH} = 1.3V, V_{OL} = 1.1V.

Note 7: t_{SKD1} is the magnitude of the difference of differential propagation delays in a channel. $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 8: t_{SKD2} is the magnitude of the difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of the other channel on the same part.

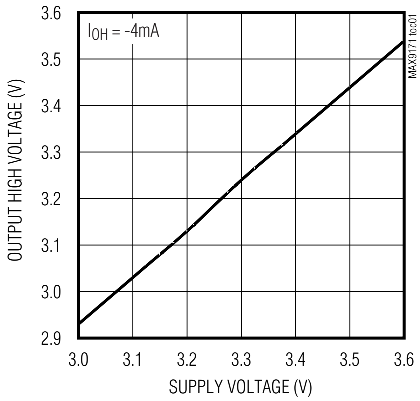
Note 9: t_{SKD3} is the magnitude of the difference of any differential propagation delays between parts at the same V_{CC} and within 5°C of each other.

Note 10: t_{SKD4} is the magnitude of the difference of any differential propagation delays between parts operating over the rated supply and temperature ranges.

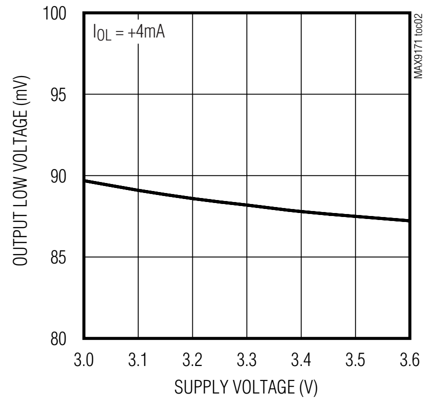
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{CM} = 1.2V, $|V_{ID}|$ = 0.2V, f_{IN} = 200MHz, C_L = 15pF, T_A = +25°C, unless otherwise specified.)

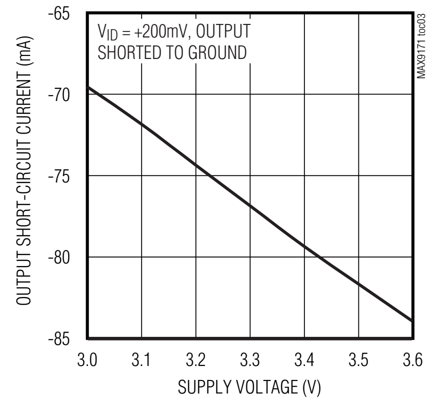
OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



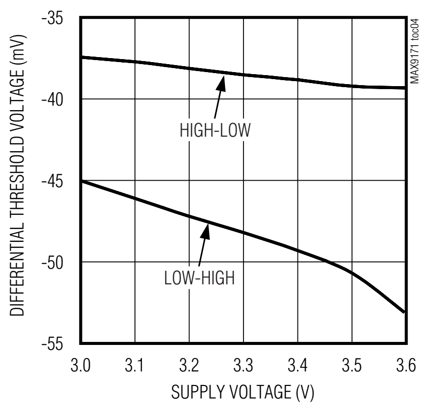
OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



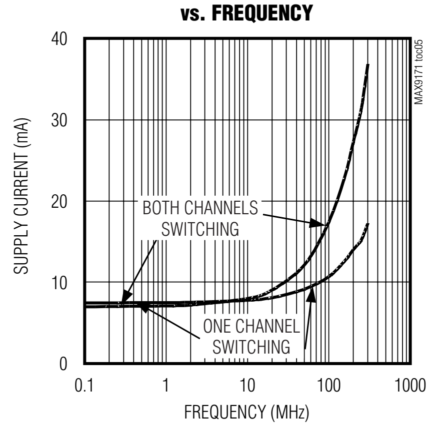
OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



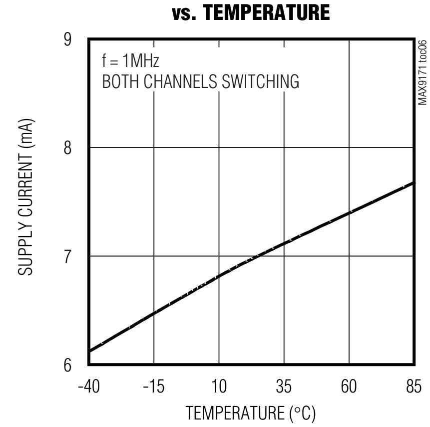
DIFFERENTIAL THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



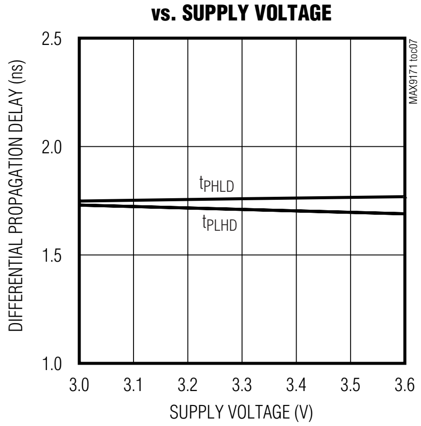
MAX9172 SUPPLY CURRENT vs. FREQUENCY



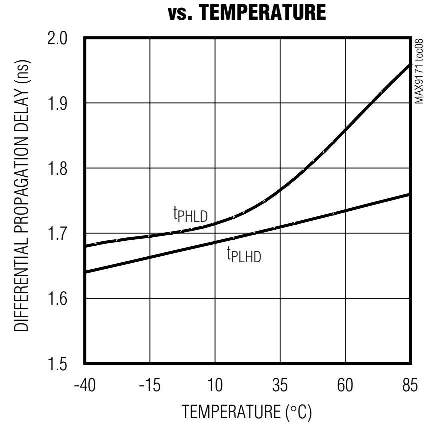
MAX9172 SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



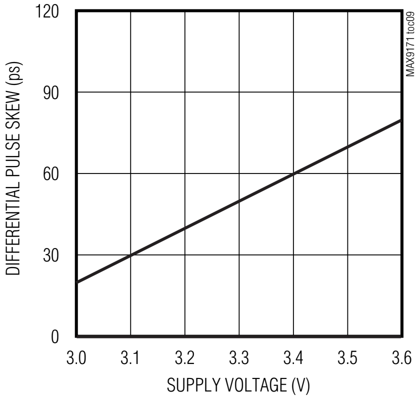
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



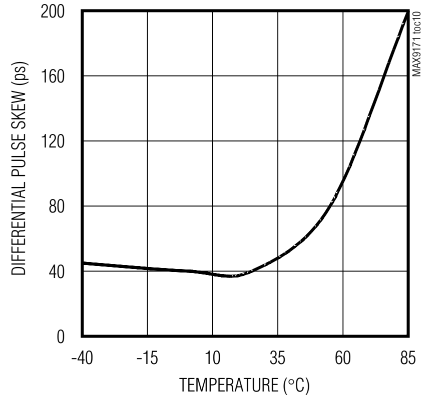
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_{CM} = 1.2V, $|V_{ID}|$ = 0.2V, f_{IN} = 200MHz, C_L = 15pF, T_A = +25°C, unless otherwise specified.)

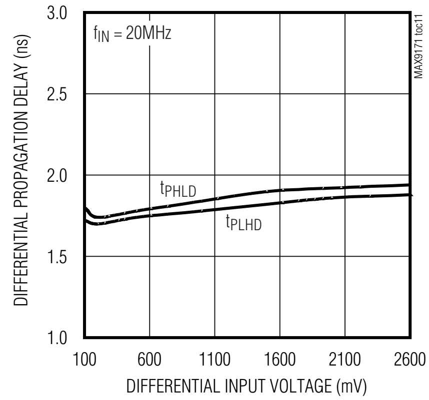
DIFFERENTIAL PULSE SKEW vs. SUPPLY VOLTAGE



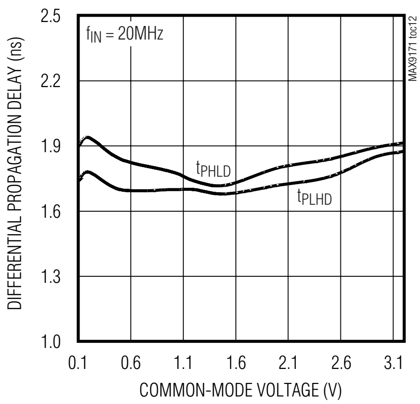
DIFFERENTIAL PULSE SKEW vs. TEMPERATURE



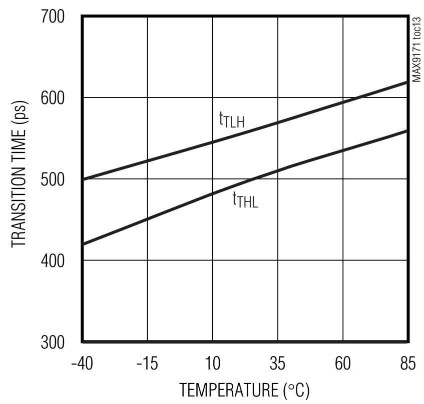
DIFFERENTIAL PROPAGATION DELAY vs. DIFFERENTIAL INPUT VOLTAGE



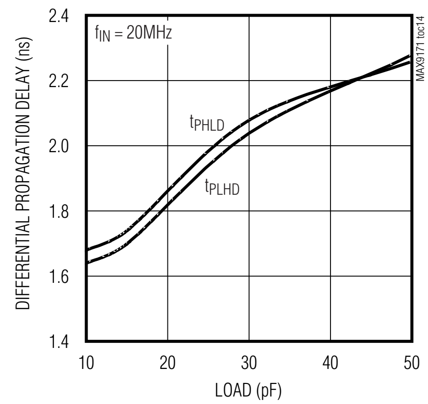
DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



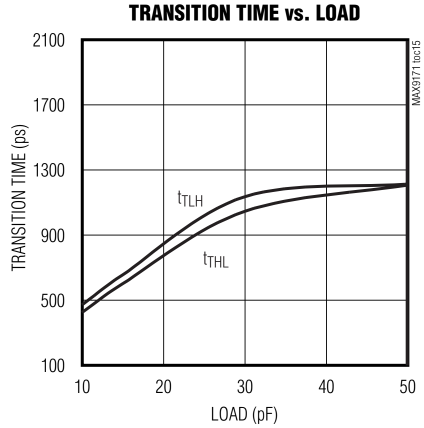
TRANSITION TIME vs. TEMPERATURE



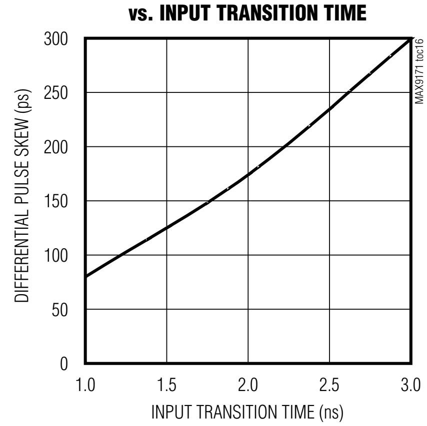
DIFFERENTIAL PROPAGATION DELAY vs. LOAD



TRANSITION TIME vs. LOAD



DIFFERENTIAL PULSE SKEW vs. INPUT TRANSITION TIME



Single/Dual LVDS Line Receivers with "In-Path" Fail-Safe

MAX9171 Pin Description

PIN		NAME	FUNCTION
SOT23	SO/QFN		
1	8	V_{CC}	Positive Power-Supply Input. Bypass with a 0.1µF and a 0.001µF capacitor to GND with the smallest capacitor closest to the pin.
2	5	GND	Ground
3	7	OUT	Receiver Output
4, 5, 6	3, 4, 6	N.C.	No Connection. Not internally connected.
7	2	IN+	Noninverting Differential Receiver Input
8	1	IN-	Inverting Differential Receiver Input
—	(QFN only)	EP	Exposed Paddle. Solder to PC board ground.

MAX9172 Pin Description

PIN		NAME	FUNCTION
SOT23	SO/QFN		
1	8	V_{CC}	Positive Power-Supply Input. Bypass with a 0.1µF and a 0.001µF capacitor to GND with the smallest capacitor closest to the pin.
2	5	GND	Ground
3	7	OUT1	Receiver Output 1
4	6	OUT2	Receiver Output 2
5	4	IN2-	Inverting Differential Receiver Input 2
6	3	IN2+	Noninverting Differential Receiver Input 2
7	2	IN1+	Noninverting Differential Receiver Input 1
8	1	IN1-	Inverting Differential Receiver Input 1
—	(QFN only)	EP	Exposed Paddle. Solder to PC board ground.

Detailed Description

LVDS Inputs

The MAX9171/MAX9172 feature LVDS inputs for interfacing high-speed digital circuitry. The LVDS interface standard is a signaling method intended for point-to-point communication over controlled-impedance media, as defined by the ANSI TIA/EIA-644 standards. The technology uses low-voltage signals to achieve fast transition times and minimize power dissipation and noise immunity. The MAX9171/MAX9172 convert LVDS signals to LVCMOS/LVTTL signals at rates in excess of 500Mbps. These devices are capable of detecting differential signals as low as 100mV and as high as 1.2V within a 0 to V_{CC} input voltage range. Table 1 is the input-output function table.

Table 1. Input-Output Function Table

INPUTS	OUTPUT
(IN_+) - (IN_-)	OUT_
≥ 0mV	High
≤ -100mV	Low
Open	High
Undriven short	High
Undriven parallel termination	High

Fail-Safe

The MAX9171/MAX9172 fail-safe drives the receiver output high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without fail-safe, differential noise at the input may switch the receiver and appear as data to the receiving system. An open input occurs when a cable and termination are disconnected. An undriven, terminated input occurs when a cable is disconnected with the termination still connected across the receiver inputs or when the driver of a receiver is in high impedance. An undriven, shorted input can occur due to a shorted cable.

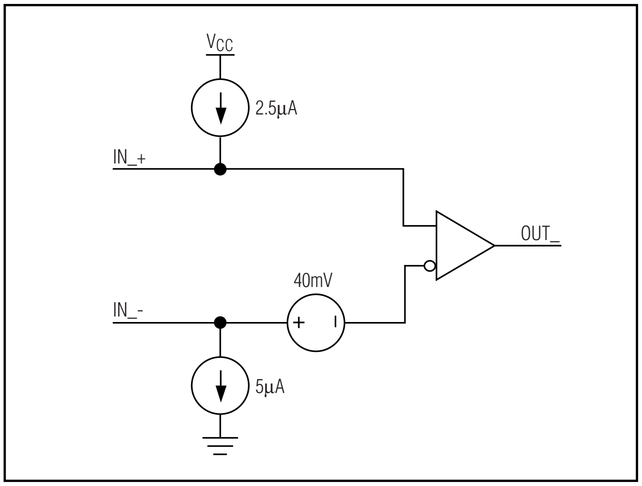


Figure 1. Input with In-Path Fail-Safe Network Equivalent Circuit

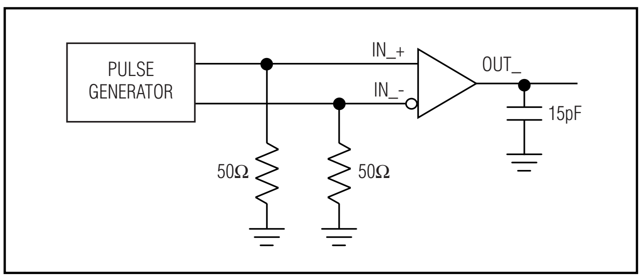


Figure 2. Propagation Delay and Transition Test Time Circuit

In-Path vs. Parallel Fail-Safe

The MAX9171/MAX9172 have in-path fail-safe that is compatible with in-path fail-safe receivers, such as the DS90LV018A and DS90LV028A. Refer to the MAX9111/MAX9113 data sheet for pin-compatible receivers with parallel fail-safe and lower jitter. Refer to the MAX9130 data sheet for a single LVDS receiver with parallel fail-safe in an SC70 package.

The MAX9171/MAX9172 with in-path fail-safe are designed with a +40mV input offset voltage, a 2.5µA current source between V_{CC} and the noninverting input, and a 5µA current sink between the inverting input and ground (Figure 1). If the differential input is open, the 2.5µA current source pulls the input to V_{CC} - 0.7V and the 5µA source sink pulls the inverting input to ground, which drives the receiver output high. If the differential input is shorted or terminated with a typical value termination resistor, the +40mV offset drives the receiver output high. If the input is terminated and floating, the receiver output is driven high by the +40mV offset, and the 2:1 current sink to current source ratio (5µA:2.5µA) pulls the inputs to ground. This can be an advantage when switching between drivers on a multipoint bus because the change in common-mode voltage from ground to the typical driver offset voltage of 1.2V is not as much as the change from V_{CC} to 1.2V (parallel fail-safe pulls the bus to V_{CC}). Figure 2 shows the propagation delay and transition test time circuit and Figure 3 shows the propagation delay and transition test time waveforms.

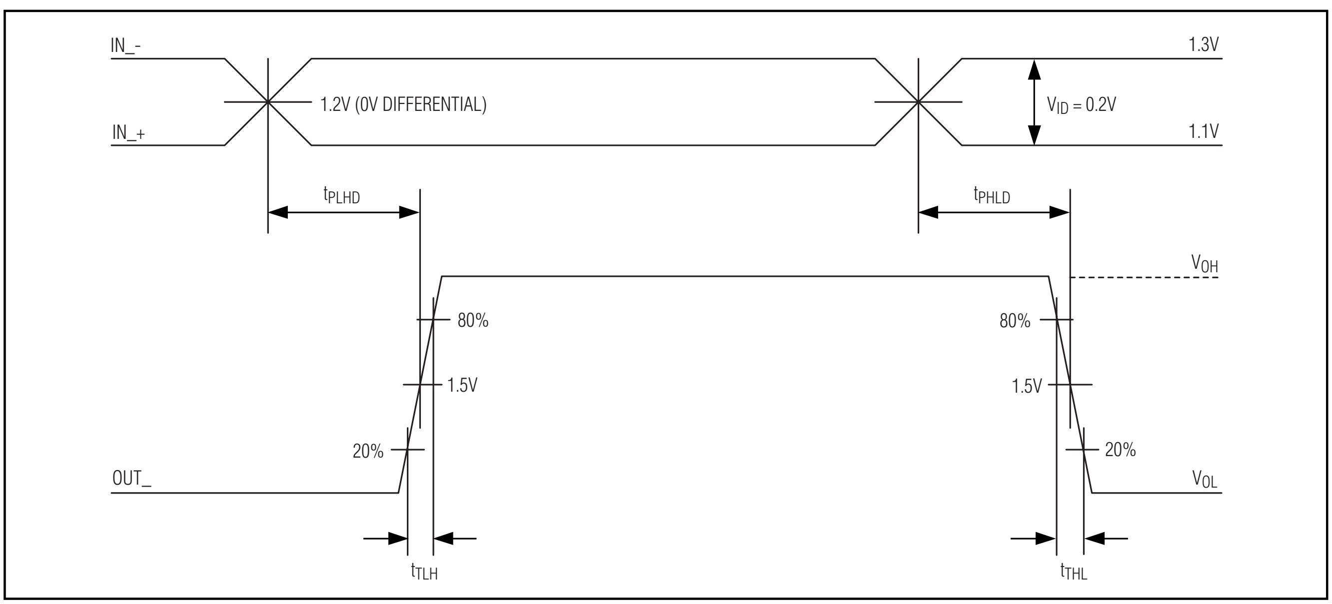


Figure 3. Propagation Delay and Transition Time Waveforms

ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The receiver inputs of the MAX9171/MAX9172 have extra protection against static electricity. These pins are protected to ±13kV without damage. The structures withstand ESD during normal operation and when powered down.

The receiver inputs of these devices are characterized for protection to the limit of ±13kV using the Human Body Model.

Human Body Model

Figure 4a shows the Human Body Model, and Figure 4b shows the current waveform it generates when discharged into a low-impedance load. This model consists of a 100pF capacitor charged to the ESD test voltage, which is then discharged into the test device through a 1.5kΩ resistor.

Applications Information

Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel, as close to the device as possible, with the 0.001µF capacitor closest to the device. For additional supply bypassing, place a 10µF tantalum or ceramic capacitor at the point where power enters the circuit board.

Differential Traces

Input trace characteristics affect the performance of the MAX9171/MAX9172. Use controlled-impedance PC board traces to match the cable characteristic impedance.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of traces.

Each channel's differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media typically have a controlled differential impedance of about 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9171/MAX9172 require an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance values may range between 90Ω to 132Ω, depending on the characteristic impedance of the transmission medium.

When using the MAX9171/MAX9172, minimize the distance between the input termination resistors and the MAX9171/MAX9172 receiver inputs. Use a single 1% surface-mount resistor.

Board Layout

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and output signals is recommended. Separate the input LVDS signals from the output signals to prevent crosstalk. Solder the exposed pad on the QFN package to a pad connected to the PC board ground plane by a matrix of vias. Connecting the exposed pad is not a substitute for connecting the ground pin. Always connect pin 5 on the QFN package to ground.

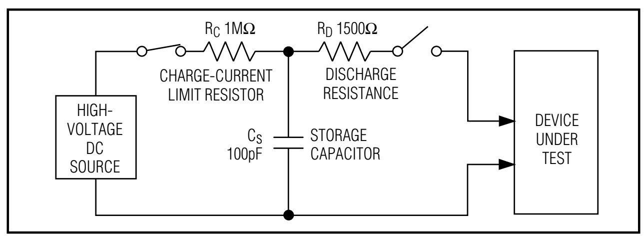


Figure 4a. Human Body ESD Test Modules

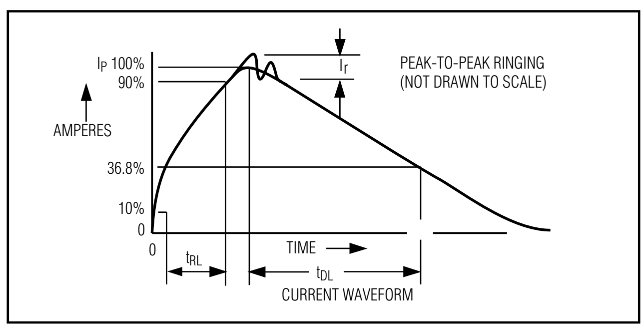


Figure 4b. Human Body Current Waveform

Chip Information

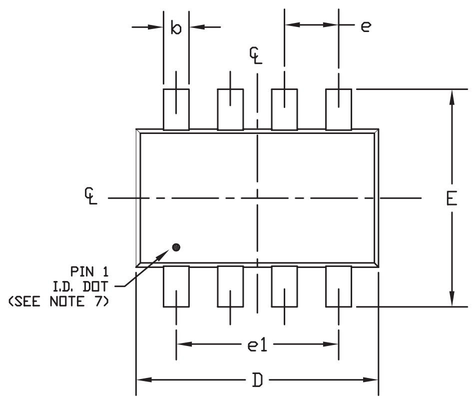
TRANSISTOR COUNT: 624

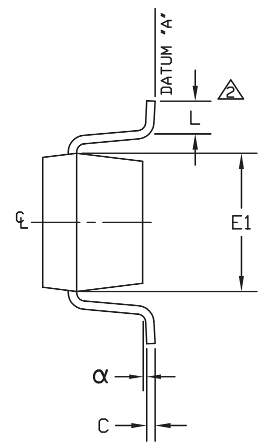
PROCESS: CMOS

Package Information

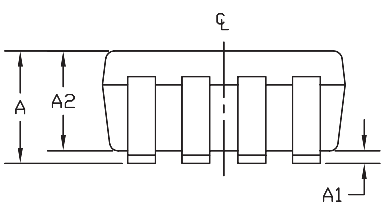
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 8L

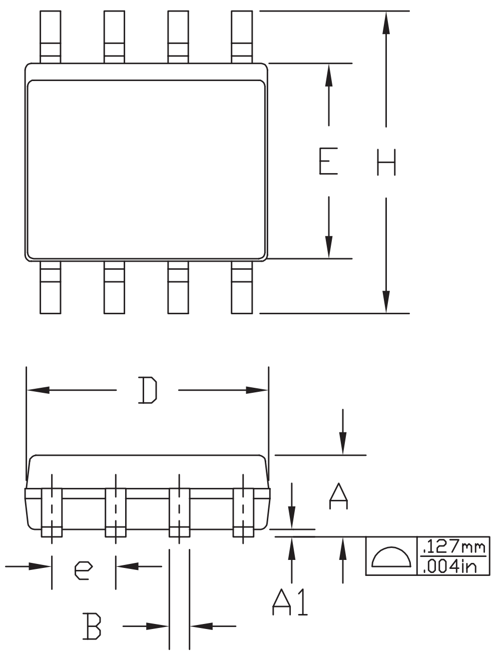
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1

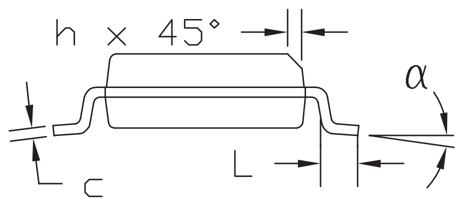
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0?	8?	0?	8?



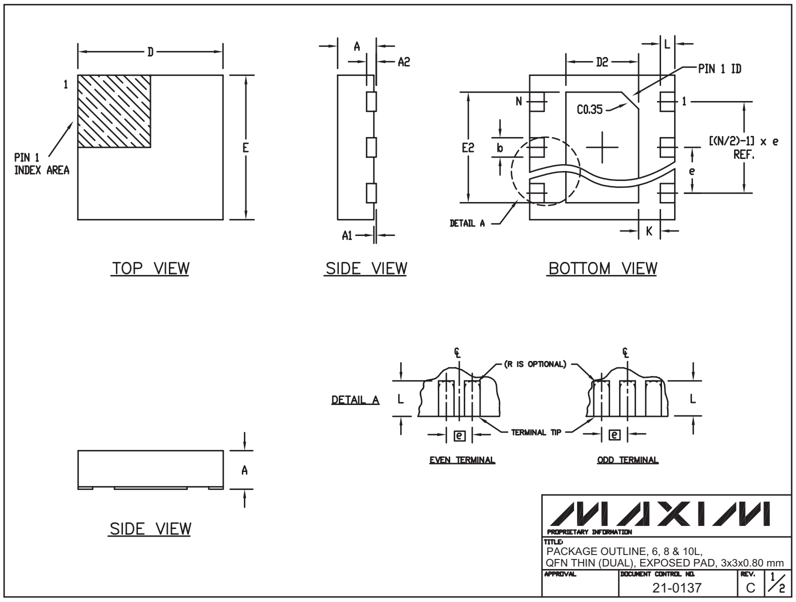


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA.

MAXIM
PROPRIETARY INFORMATION
TITLE
8L SOIC OUTLINE
APPROVAL | DWG 21-0325 | REV A | 1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO220.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 6, 8 & 10L,
QFN THIN (DUAL), EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	C	2/2

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