查询"DS92LV3242"供应商

National Semiconductor

September 17, 2009

DS92LV3241/DS92LV3242

20-85 MHz 32-Bit Channel Link II Serializer / Deserializer

General Description

The DS92LV3241 (SER) serializes a 32-bit data bus into 2 or 4 (selectable) embedded clock LVDS serial channels for a data payload rate up to 2.72 Gbps over cables such as CATx, or backplanes FR-4 traces. The companion DS92LV3242 (DES) deserializes the 2 or 4 LVDS serial data channels, deskews channel-to-channel delay variations and converts the LVDS data stream back into a 32-bit LVCMOS parallel data bus.

On-chip data Randomization/Scrambling and DC balance encoding and selectable serializer Pre-emphasis ensure a robust, low-EMI transmission over longer, lossy cables and backplanes. The Deserializer automatically locks to incoming data without an external reference clock or special sync patterns, providing an easy “plug-and-lock” operation.

By embedding the clock in the data payload and including signal conditioning functions, the Channel-Link II SerDes devices reduce trace count, eliminate skew issues, simplify design effort and lower cable/connector cost for a wide variety of video, control and imaging applications. A built-in AT-SPEED BIST feature validates link integrity and may be used for system diagnostics.

Features

- Wide Operating Range Embedded Clock SER/DES
  - Up to 32-bit parallel LVCMOS data
  - 20 to 85 MHz parallel clock
  - Up to 2.72 Gbps application data paylod
- Selectable Serial LVDS Bus Width
  - Dual Lane Mode (20 to 50 MHz)
  - Quad Lane Mode (40 to 85 MHz)
- Simplified Clocking Architecture
  - No separate serial clock line
  - No reference clock required
  - Receiver locks to random data
- On-chip Signal Conditioning for Robust Serial Connectivity
  - Transmit Pre-Emphasis
  - Data randomization
  - DC-balance encoding
  - Receive channel deskew
  - Supports up to 10m CAT-5 at 2.7 Gbps
- Integrated LVDS Terminations
- Built-in AT-SPEED BIST for end-to-end system testing
- AC-coupled interconnect for isolation and fault protection
- > 4KV HBM ESD protection
- Space-saving 64-pin TQFP package
- Full industrial temperature range : -40° to +85°C

Applications

- Industrial imaging (Machine-vision) and control
- Security & Surveillance cameras and infrastructure
- Medical imaging
- Up to 30 bits per pixel, VGA to HD video transport and display

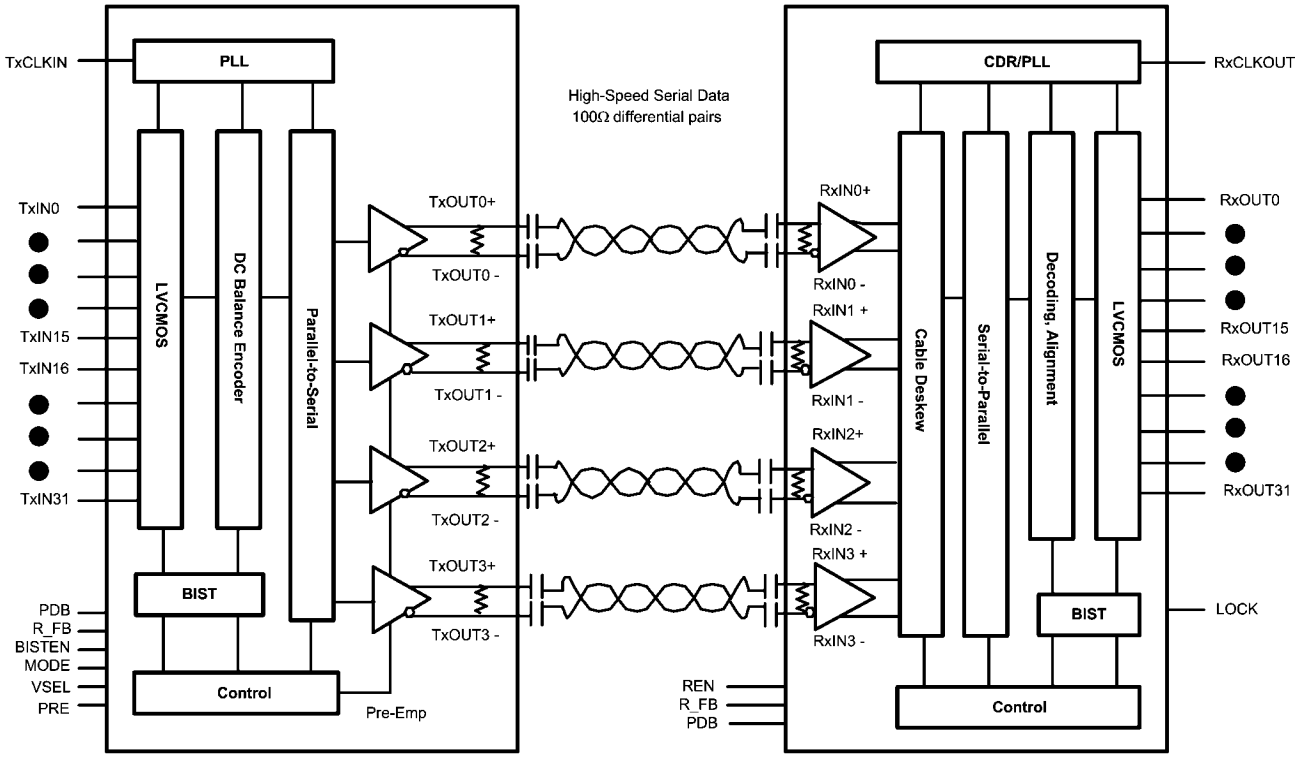
TRI-STATE® is a registered trademark of National Semiconductor Corporation.

© 2010 National Semiconductor Corporation

pdf.dzsc.com

查询 DS92LV3242 供应商

Block Diagram



30103627

Mode Diagrams

查询"DS92LV3242"供应商

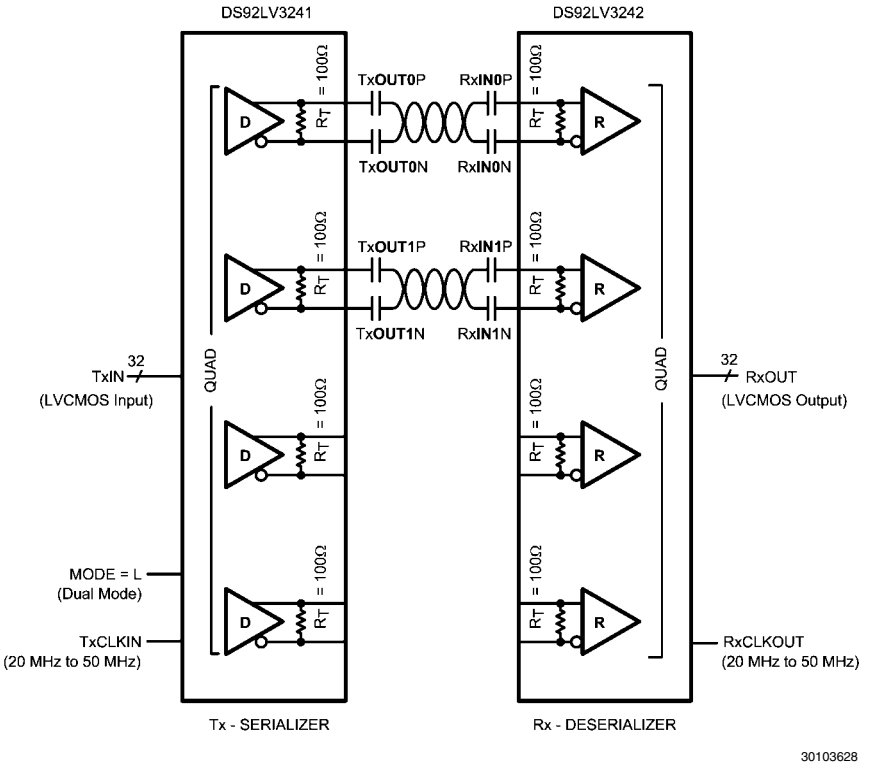


FIGURE 1. Dual Mode

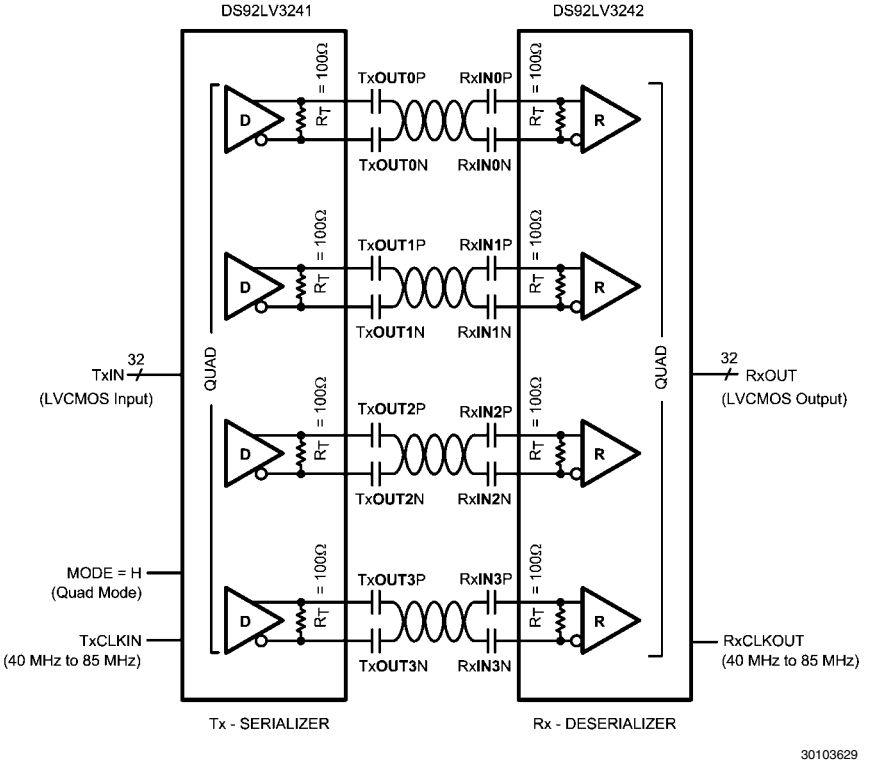


FIGURE 2. Quad Mode

DS92LV3241 Pin Diagram

查询"DS92LV3242"供应商

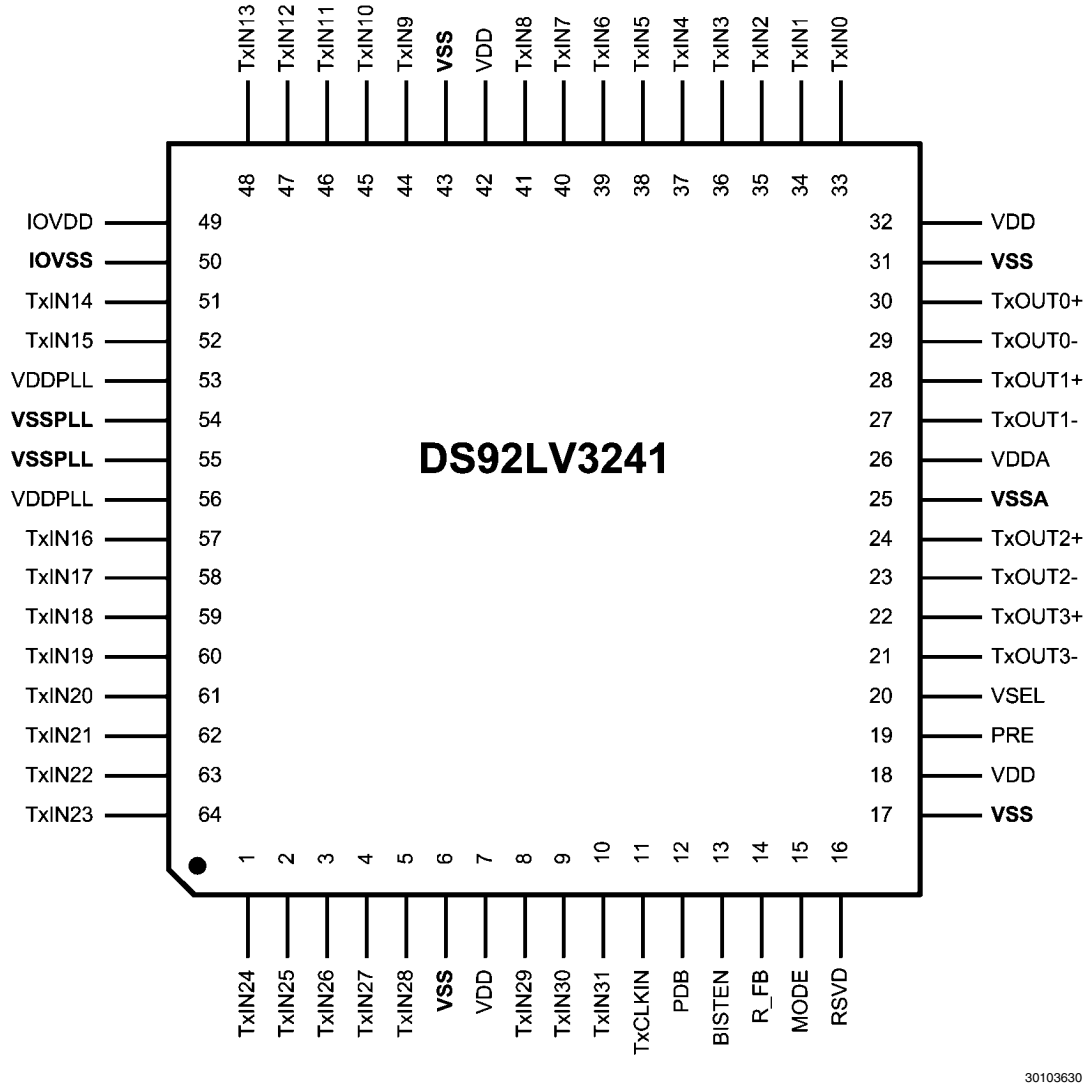


FIGURE 3. DS92LV3241 Pin Diagram— Top View

DS92LV3241 Serializer Pin Descriptions

查询"DS92LV3242"供应商

Pin #	Pin Name	I/O, Type	Description
LVCMOS PARALLEL INTERFACE PINS			
10–8, 5–1, 64–57, 52–51, 48–44. 41–33	TxIN[31:29], TxIN[28:24], TxIN[23:16], TxIN[15:14], TxIN[13:9], TxIN[8:0]	I, LVCMOS	Serializer Parallel Interface Data Input Pins.
11	TxCLKIN	I, LVCMOS	Serializer Parallel Interface Clock Input Pin. Strobe edge set by R_FB configuration pin.
CONTROL AND CONFIGURATION PINS			
12	PDB	I, LVCMOS	Serializer Power Down Bar (ACTIVE LOW) PDB = L; Device Disabled, Differential serial outputs are put into TRI-STATE® stand-by mode, PLL is shutdown PDB = H; Device Enabled
15	MODE	I, LVCMOS	Dual or Quad mode select (ACTIVE H) MODE = L (default); Dual Mode, MODE = H; Quad Mode
19	PRE	I, LVCMOS	PRE-emphasis level select pin PRE = (RPRE > 12kΩ); Imax = [(1.2/R) x 20 x 2], Rmin = 12kΩ. PRE = H or floating; pre-emphasis is disabled.
14	R_FB	I, LVCMOS	Rising/Falling Bar Clock Edge Select R_FB = H; Rising Edge, R_FB = L; Falling Edge
20	VSEL	I, LVCMOS	VOD (Differential Output Voltage) Llevel Select VSEL = L; Low Swing, VSEL = H; High Swing
13	BISTEN	I, LVCMOS	BIST Enable BISTEN = L; BIST OFF, (default), normal operating mode. BISTEN = H; BIST Enabled (ACTIVE HIGH)
16	RSVD	I, LVCMOS	Reserved — MUST BE TIED LOW
LVDS SERIAL INTERFACE PINS			
22, 24, 28, 30	TxOUT[3:0]+	O, LVDS	Serializer LVDS Non-Inverted Outputs(+)
21, 23, 27, 29	TxOUT[3:0]-	O, LVDS	Serializer LVDS Inverted Outputs(-)
POWER / GROUND PINS			
7, 18, 32, 42	VDD	VDD	Digital Voltage supply, 3.3V
6, 17, 31, 43	VSS	GND	Digital ground
53, 56	VDDPLL	VDD	Analog Voltage supply, PLL POWER, 3.3V
54, 55	VSSPLL	GND	Analog ground, PLL GROUND
26	VDDA	VDD	Analog Voltage supply
25	VSSA	GND	Analog ground
49	IOVDD	VDD	Digital IO Voltage supply Connect to 1.8V typ for 1.8V LVCMOS interface Connect to 3.3V typ for 3.3V LVCMOS interface
50	IOVSS	GND	Digital IO ground

DS92LV3242 Pin Diagram

查询"DS92LV3242"供应商

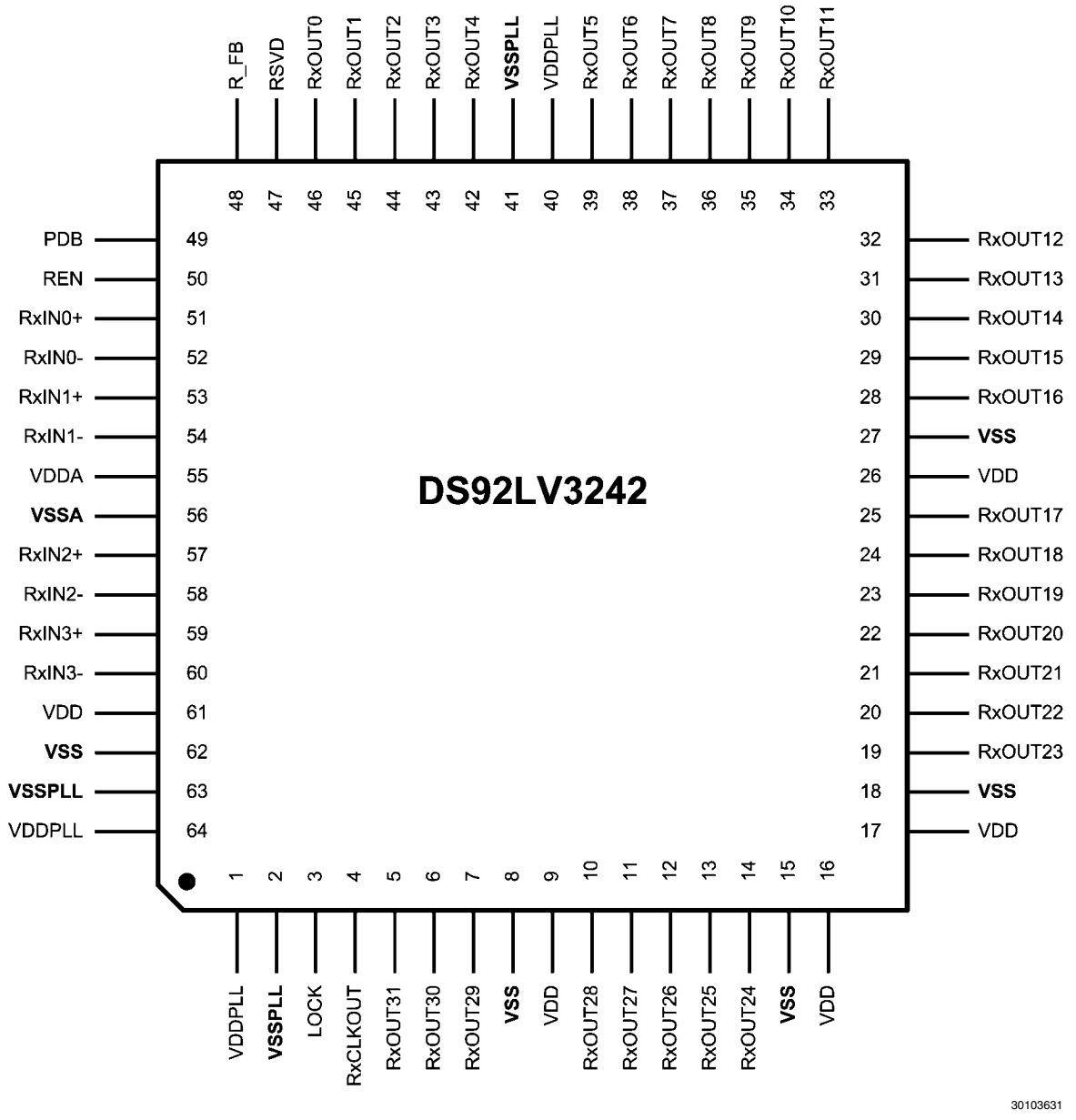


FIGURE 4. DS92LV3242 Pin Diagram — Top View

DS92LV3242 Deserializer Pin Descriptions

查询"DS92LV3242"供应商

Pin #	Pin Name	I/O, Type	Description
LVCMOS PARALLEL INTERFACE PINS			
5–7, 10–14, 19–25, 28–32, 33–39, 42–46	RxOUT[31:29], RxOUT[28:24], RxOUT[23:17], RxOUT[16:12], RxOUT[11:5], RxOUT[4:0]	O, LVCMOS	Deserializer Parallel Interface Data Output Pins.
4	RxCLKOUT	O, LVCMOS	Deserializer Recovered Clock Output. Parallel data rate clock recovered from the embedded clock.
3	LOCK	O, LVCMOS	LOCK indicates the status of the receiver PLL LOCK = L; deserializer CDR/PLL is not locked, RxOUT[31:0] and RCLK are TRI-STATED® LOCK = H; deserializer CDR/PLL is locked
CONTROL AND CONFIGURATION PINS			
48	R_FB	I, LVCMOS	Rising/Falling Bar Clock Edge Select R_FB = H; RxOUT clocked on rising edge R_FB = L; RxOUT clocked on falling edge
50	REN	I, LVCMOS	Deserializer Enable, DES Output Enable Control Input (ACTIVE HIGH) REN = L; disabled, RxOUT[31:0] and RxCLKOUT TRI-STATED, PLL still operational REN = H; Enabled (ACTIVE HIGH)
49	PDB	I, LVCMOS	Power Down Bar, Control Input Signal (ACTIVE LOW) PDB = L; disabled, RxOUT[31:0], RCLK, and LOCK are TRI-STATED in stand-by mode, PLL is shutdown PDB = H; Enabled
47	RSVD	I, LVCMOS	Reserved — MUST BE TIED LOW
LVDS SERIAL INTERFACE PINS			
51, 53, 57, 59	RxIN[0:3]+	I, LVDS	Deserializer LVDS Non-Inverted Inputs(+)
52, 54, 58, 60	RxIN[0:3]-	I, LVDS	Deserializer LVDS Inverted Inputs(-)
POWER / GROUND PINS			
9, 16, 17, 26, 61	VDD	VDD	Digital Voltage supply, 3.3V
8, 15, 18, 27, 62	VSS	GND	Digital Ground
55	VDDA	VDD	Analog LVDS Voltage supply, POWER, 3.3V
56	VSSA	GND	Analog LVDS GROUND
1, 40, 64	VDDPLL	VDD	Analog Voltage supply PLL VCO POWER, 3.3V
2, 41, 63	VSSPLL	GND	Analog ground, PLL VCO GROUND

查询"DS92LV3242"供应商

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{DD} +0.3V)
LVCMOS Output Voltage	−0.3V to (V_{DD} +0.3V)
LVDS Deserializer Input Voltage	−0.3V to +3.9V
LVDS Driver Output Voltage	−0.3V to +3.9V
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity	
Package Derating:	1/θ_{JA} °C/W above +25°C
θ_{JA}	35.7 °C/W*
θ_{JC}	12.6 °C/W
	**4 Layer JEDEC*
ESD Rating (HBM)	>4 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD})	3.135	3.3	3.465	V
Supply Voltage(IOV_{DD}) (SER ONLY)				
3.3V I/O Interface	3.135	3.3	3.465	V
1.8V I/O Interface	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Input Clock Rate				
Dual Mode	20		50	MHz
Quad Mode	40		85	MHz
Tolerable Supply Noise			100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	Tx: IOV_{DD} = 1.71V to 1.89V	0.65 x IOV_{DD}		IOV_{DD} + 0.3	V
		Tx: IOV_{DD} = 3.135V to 3.465V	2.0		V_{DD}	
		Rx				
V_{IL}	Low Level Input Voltage	Tx: IOV_{DD} = 1.71V to 1.89V	GND		0.35 x IOV_{DD}	V
		Tx: IOV_{DD} = 3.135V to 3.465V	GND		0.8	
		Rx				
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.8	−1.5	V
I_{IN}	Input Current	Tx: V_{IN} = 0V or 3.465V(1.89V) IOV_{DD} = 3.465V(1.89V)	−10		+10	µA
		Rx: V_{IN} = 0V or 3.465V	−10		+10	
V_{OH}	High Level Output Voltage	I_{OH} = −2mA (Dual)	2.4	3.0	V_{DD}	V
		I_{OH} = −2mA (Quad)				
V_{OL}	Low Level Output Voltage	I_{OH} = −2mA (Dual)	GND	0.33	0.5	V
		I_{OH} = −2mA (Quad)				
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Dual)		−22	−40	mA
		V_{OUT} = 0V (Quad)		−33	−70	mA
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	−10		+10	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIALIZER LVDS DC SPECIFICATIONS						
V_{OD}	Output Differential Voltage	No pre-emphasis, VSEL = L (VSEL = H)	350 (629)	440 (850)	525 (1000)	mV_{P-P}
ΔV_{OD}	Output Differential Voltage Unbalance	VSEL = L, No pre-emphasis		1	50	mV_{P-P}
V_{OS}	Offset Voltage	VSEL = L, No pre-emphasis	1.00	1.25	1.50	V
ΔV_{OS}	Offset Voltage Unbalance	VSEL = L, No pre-emphasis		4	50	mV
I_{OS}	Output Short Circuit Current	TxOUT[3:0] = 0V, PDB = V_{DD}, VSEL = L, No pre-emphasis	−2	−5		mA
		TxOUT[3:0] = 0V, PDB = V_{DD}, VSEL = H, No pre-emphasis	−6	−10		
I_{OZ}	TRI-STATE® Output Current	PDB = 0V, TxOUT[3:0] = 0V OR V_{DD}	−15	±1	+15	µA
		PDB = V_{DD}, TxOUT[3:0] = 0V OR V_{DD}	−15	±1	+15	µA
R_T	Output Termination	Internal differential output termination between differential pairs	90	100	130	Ω

查询"DS92LV3242"供应商

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIALIZER SUPPLY CURRENT (DVDD*, PVDD* AND AVDD* PINS) **DIGITAL, PLL, AND ANALOG VDDS*						
I_{DDTQ}	Serializer (Tx) Total Supply Current Quad Mode (includes load current)	f = 85 MHz, CHECKER BOARD pattern MODE = H, VSEL = H, PRE = OFF		150	200	mA
		f = 85 MHz, CHECKER BOARD pattern MODE = H, VSEL = H, RPRE = 12 kΩ		150	200	
		f = 85 MHz, RANDOM pattern MODE = H, VSEL = H, PRE = OFF		140	195	
		f = 85 MHz, RANDOM pattern MODE = H, VSEL = H, RPRE = 12 kΩ		140	195	
I_{DDTD}	Serializer (Tx) Total Supply Current Dual Mode (includes load current)	f= 50 MHz, CHECKER BOARD pattern MODE = L, VSEL = H, PRE = OFF		120	145	mA
		f= 50 MHz, CHECKER BOARD pattern MODE = H, VSEL = H, RPRE = 12 kΩ		120	145	
		f= 50 MHz, RANDOM pattern MODE = L, VSEL = H, PRE = OFF		115	135	
		f= 50 MHz, RANDOM pattern MODE = L, VSEL = H, RPRE = 12 kΩ		115	135	
I_{DDTZ}	Serializer Supply Current Power-down	TPWDNB = 0V (All other LVCMOS Inputs = 0V)		2	50	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DESERIALIZER LVDS DC SPECIFICATIONS						
V_{TH}	Differential Threshold High Voltage	V_{CM} = +1.8V			+50	mV
V_{TL}	Differential Threshold Low Voltage		–50			mV
R_T	Input Termination	Internal differential output termination between differential pairs	90	100	130	Ω
I_{IN}	Input Current	V_{IN} = +2.4V, V_{DD} = 3.6V		±100	±250	µA
		V_{IN} = 0V, V_{DD} = 3.6V		±100	±250	µA
DESERIALIZER SUPPLY CURRENT (DVDD*, PVDD* AND AVDD* PINS) *DIGITAL, PLL, AND ANALOG VDDS*						
I_{DDR}	Deserializer Total Supply Current (includes load current)	f = 85 MHz, C_L = 8 pF, CHECKER BOARD pattern, Quad Mode		240	265	mA
		f = 85 MHz, C_L = 8 pF, RANDOM pattern, Quad Mode		190	210	
		f = 50 MHz, C_L = 8 pF, CHECKER BOARD pattern, Dual Mode		145	185	mA
		f = 50 MHz, C_L = 8 pF, RANDOM pattern, Dual Mode		122	140	
I_{DDRZ}	Deserializer Supply Current Power-down	PDB = 0V (All other LVCMOS Inputs = 0V, RxIN[3:0](P/N) = 0V)			100	µA

Serializer Input Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CIP}	TxCLKIN Period	MODE = L (Dual Mode)	20	t_{CIP}	50	ns
		MODE = H (Quad Mode)	11.76	t_{CIP}	25	
t_{CIH}	TxCLKIN High Time	20 MHz – 50 MHz	0.45 x t_{CIP}	0.5 x t_{CIP}	0.55 x t_{CIP}	ns
		40 MHz – 85 MHz	0.45 x t_{CIP}	0.5 x t_{CIP}	0.55 x t_{CIP}	
t_{TCIL}	TxCLKIN Low Time	20 MHz – 50 MHz *Figure 7*	0.45 x t_{CIP}	0.5 x t_{CIP}	0.55 x t_{CIP}	ns
		40 MHz – 85 MHz	0.45 x t_{CIP}	0.5 x t_{CIP}	0.55 x t_{CIP}	
t_{CIT}	TxCLKIN Transition Time	20 MHz – 50 MHz *Figure 6*	0.5		1.2	ns
		40 MHz – 85 MHz	0.5		1.2	
t_{JIT}	TxCLKIN Jitter				±100	ps_{P-P}

查询 DS92LV3242 供应商

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	LVDS Low-to-High Transition Time	No pre-emphasis *Figure 5*		350		ps
t_{LHLT}	LVDS High-to-Low Transition Time			350		ps
t_{STC}	TxIN[31:0] Setup to TxCLKIN	IOVDD = 1.71V to 1.89V *Figure 7*	0			ns
		IOVDD = 3.135V to 3.465V	0			
t_{HTC}	TxIN[31:0] Hold from TxCLKIN	IOVDD = 1.71V to 1.89V	2.5			ns
		IOVDD = 3.135V to 3.465V	2.25			
t_{PLD}	Serializer PLL Lock Time	*Figure 9*		4400 x t_{CIP}	5000 x t_{CIP}	ns
t_{LZD}	Data Output LOW to TRI-STATE® Delay	(*Note 4*)		5	10	ns
t_{HZD}	Data Output TRI-STATE® to HIGH Delay	(*Note 4*)		5	10	ns
t_{SD}	Serializer Propagation Delay - Latency	f = 50 MHz, R_FB = H, PRE = OFF, MODE = L *Figure 8*		4.5 t_{CIP} + 6.77		ns
		f = 50 MHz, R_FB = L, PRE = OFF, MODE = L	4.5 t_{CIP} + 5.63	4.5 t_{CIP} + 7.09	4.5 t_{CIP} + 9.29	
		f = 20 MHz, R_FB = H, PRE = OFF, MODE = L	4.5 t_{CIP} + 6.57	4.5 t_{CIP} + 8.74	4.5 t_{CIP} + 10.74	
		f = 85MHz, R_FB = H, PRE = OFF, MODE = H		9.0 t_{CIP} + 6.99		
		f = 85MHz, R_FB = L, PRE = OFF, MODE = H	9.0 t_{CIP} + 5.97	9.0 t_{CIP} + 7.38	9.0 t_{CIP} + 9.64	
		f = 40 MHz, R_FB = HL, PRE = OFF, MODE = H	9.0 t_{CIP} + 6.30	9.0 t_{CIP} + 8.26	9.0 t_{CIP} + 10.49	
t_{LVSKD}	LVDS Output Skew	LVDS differential output channel-to-channel skew		30	500	ps

查询"DS92LV3242"供应商

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Λ_{STXBW}	Jitter Transfer Function (−3 dB Bandwidth	Dual Mode f = 50 MHz *Figure 15*		2.8		MHz
		Quad Mode f = 85 MHz		2		
δ_{STX}	Serializer Jitter Transfer Function Peaking	Dual Mode f = 50 MHz		0.3		dB
		Quad Mode f = 85 MHz		0.9		

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ROCP}	Receiver Output Clock Period	$t_{ROCP} = t_{CIP}$ (Dual Mode) *Figure 11*	20	t_{ROCP}	50	ns
		$t_{ROCP} = t_{CIP}$ (Quad Mode)	11.76	t_{ROCP}	25	
t_{RODC}	RxCLKOUT Duty Cycle		45	50	55	%
t_{ROTR}	LVCMOS Low-to-High Transition Time	C_L = 8pF (lumped load) (Dual Mode) *Figure 10*		3.2		ns
t_{ROTF}	LVCMOS High-to-Low Transition Time			3.5		ns
t_{ROTR}	LVCMOS Low-to-High Transition Time	C_L = 8pF (lumped load) (Quad Mode)		2.4		ns
t_{ROTF}	LVCMOS High-to-Low Transition Time			1.9		ns
t_{ROSC}	RxOUT[31:0] Setup to RxCLKOUT	f = 50 MHz (Dual Mode)	5.6	0.5 x t_{ROCP}		ns
t_{ROHC}	RxOUT[31:0] Hold to RxCLKOUT		7.4	0.5 x t_{ROCP}		ns
t_{ROSC}	RxOUT[31:0] Setup to RxCLKOUT	f = 85 MHz (Quad Mode)	3.4	0.5 x t_{ROCP}		ns
t_{ROHC}	RxOUT[31:0] Hold to RxCLKOUT		3.4	0.5 x t_{ROCP}		ns
t_{HZR}	Data Output High to TRI-STATE® Delay	*Figure 13*		5	10	ns
t_{LZR}	Data Output Low to TRI-STATE® Delay			5	10	ns
t_{ZHR}	Data Output TRI-STATE® to High Delay			5	10	ns
t_{ZLR}	Data Output TRI-STATE® to Low Delay			5	10	ns

查询"DS92LV3242"供应商

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RD}	Deserializer Propagation Delay – Latency	f = 20 MHz (Dual Mode) *Figure 12*		5.5 x t_{ROCP} + 3.35		ns
		f = 50 MHz (Dual Mode)		5.5 x t_{ROCP} + 6.00		ns
		f = 40 MHz (Quad Mode)		12.0 x t_{ROCP} + 7.4		ns
		f = 85 MHz (Quad Mode)		12.0 x t_{ROCP} + 5.7		ns
t_{RPLLS}	Deserializer PLL Lock Time	20 MHz – 50 MHz (Dual Mode) *Figure 13* (*Note 5*)			128k x t_{ROCP}	ns
		40 MHz – 85 MHz (Quad Mode) *Figure 13* (*Note 5*)			256k x t_{ROCP}	ns
TOL_{JIT}	Deserializer Input Jitter Tolerance			0.25		UI
t_{LVSKR}	LVDS Differential Input Skew Tolerance	20 MHz – 85 MHz *Figure 17*			0.4 x t_{ROCP}	ns

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: Typical values represent most likely parametric norms at V_{DD} = 3.3V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Note 3: Current into a the device is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH}, V_{TL} which are differential voltages.

Note 4: When the Serializer output is at TRI-STATE® the Deserializer will lose PLL lock. Resynchronization MUST occur before data transfer.

Note 5: t_{RPLLS} is the time required by the Deserializer to obtain lock when exiting power-down mode.

AC Timing Diagrams and Test Circuits

查询"DS92LV3242"供应商

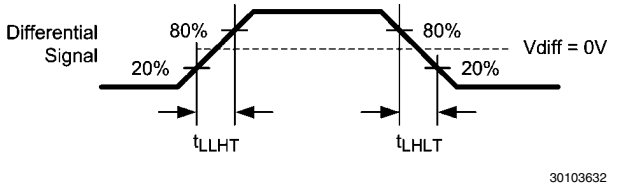


FIGURE 5. Serializer LVDS Transition Times

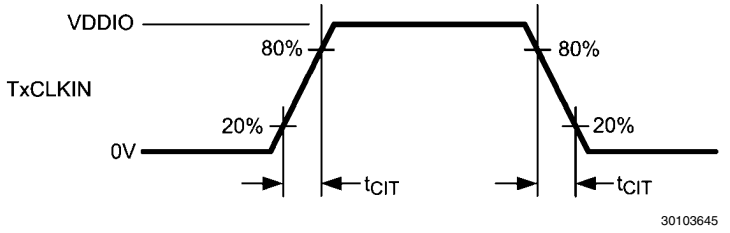


FIGURE 6. Serializer Input Clock Transition Time

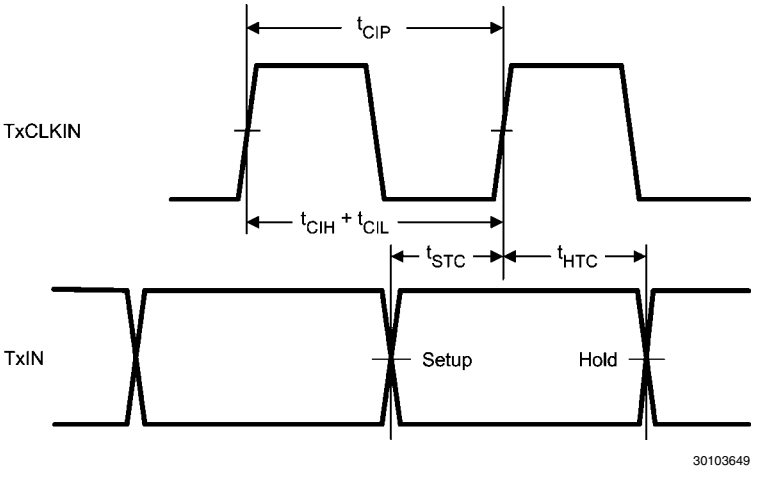


FIGURE 7. Serializer Setup/Hold and High/Low Times

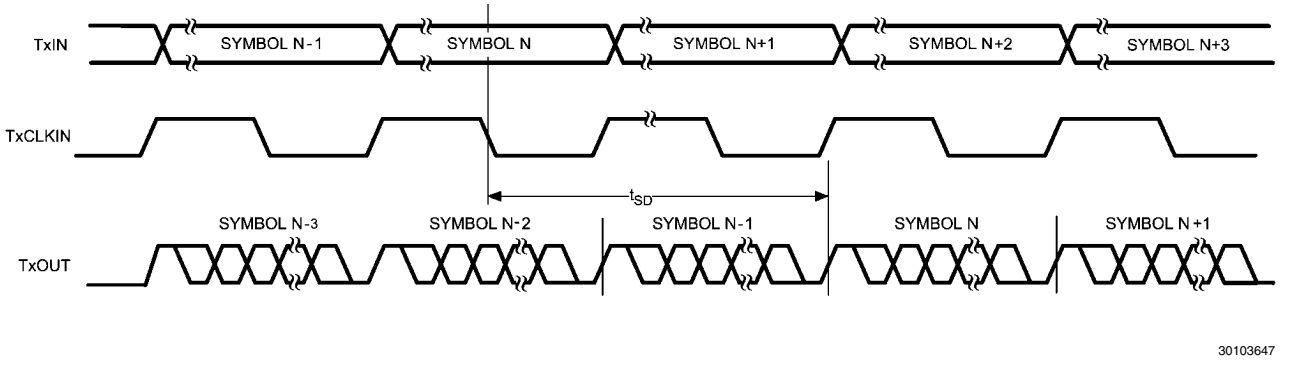


FIGURE 8. Serializer Propagation Delay

查询"DS92LV3242"供应商

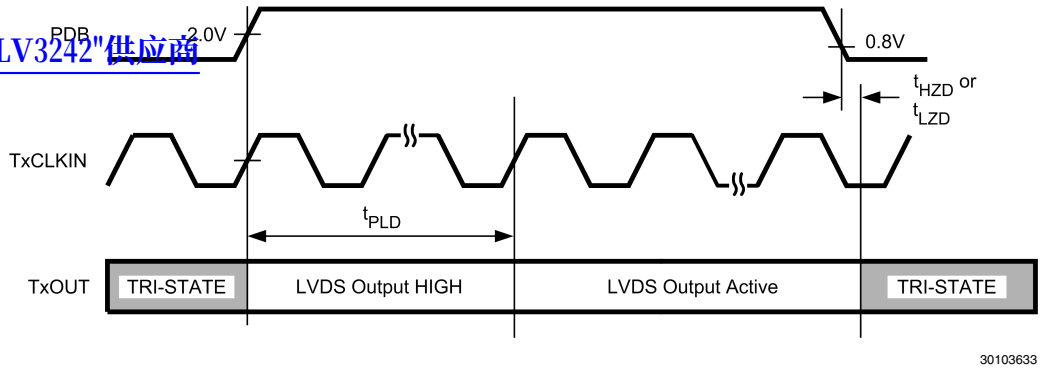


FIGURE 9. Serializer PLL Lock Time

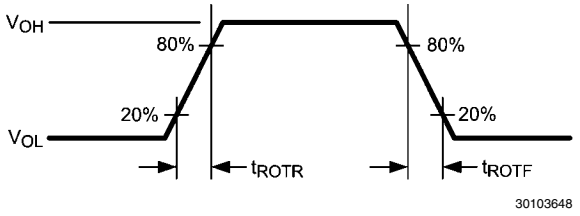


FIGURE 10. Deserializer LVCMOS Output Transition Time

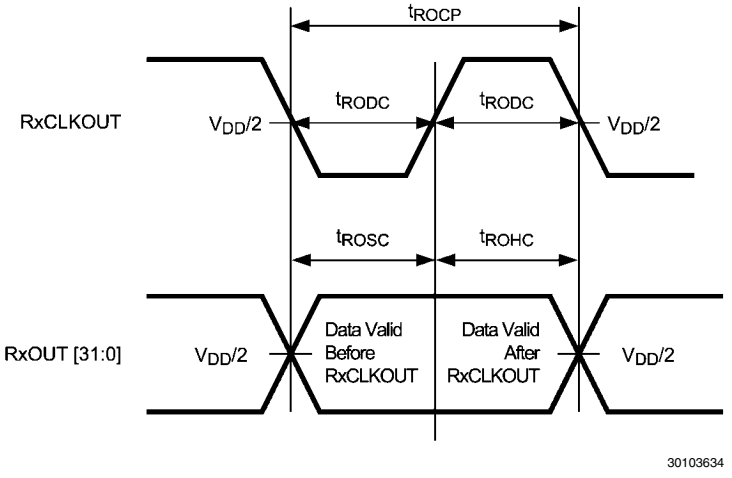


FIGURE 11. Deserializer Setup and Hold times

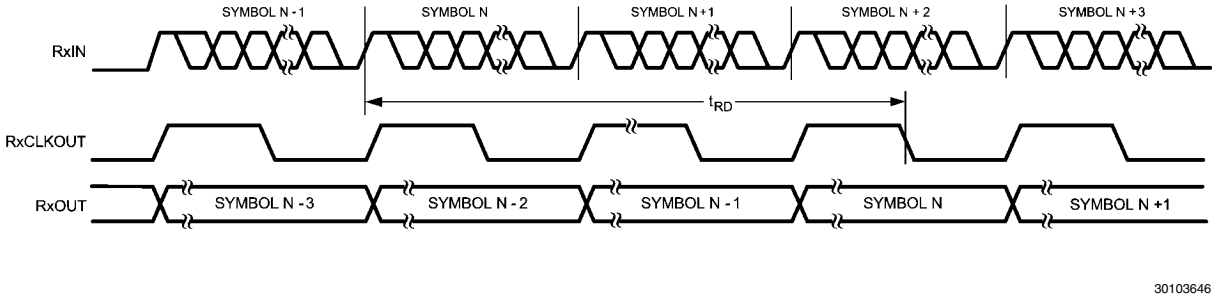


FIGURE 12. Deserializer Propagation Delay

查询"DS92LV3242"供应商

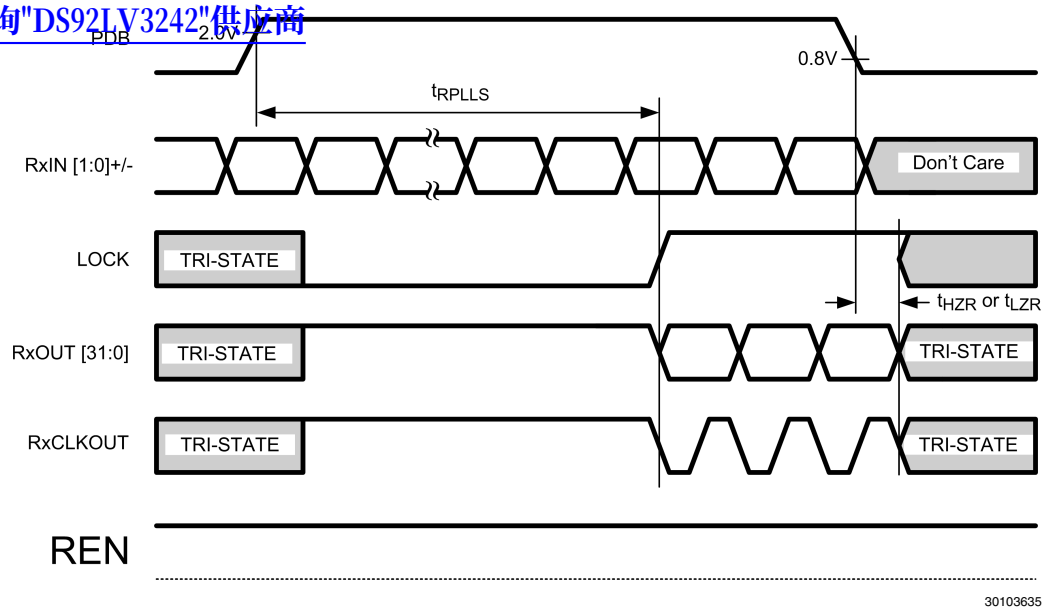
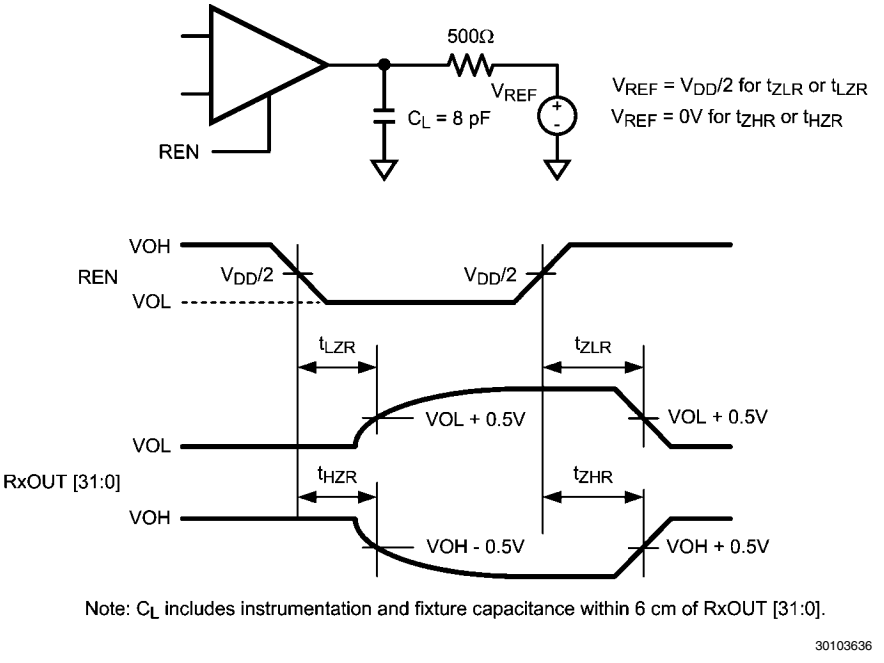


FIGURE 13. Deserializer PLL Lock Time and PDB TRI-STATE® Delay



Note: C_L includes instrumentation and fixture capacitance within 6 cm of RxOUT [31:0].

FIGURE 14. Deserializer TRI_STATE Test Circuit and Timing

查询"DS92LV3242"供应商

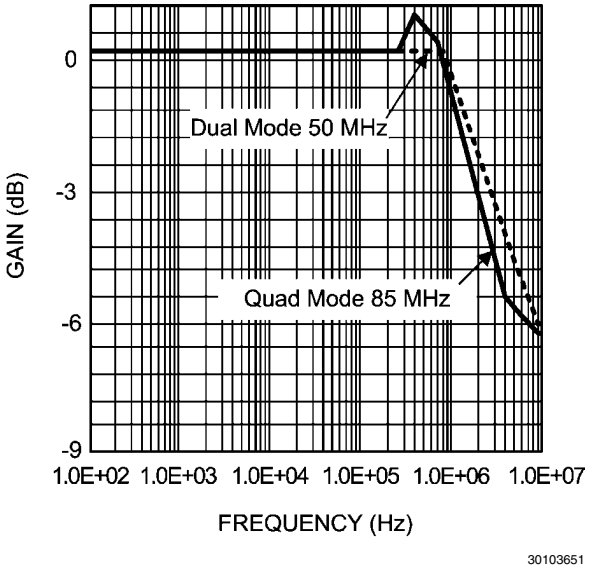


FIGURE 15. Serializer Jitter Transfer

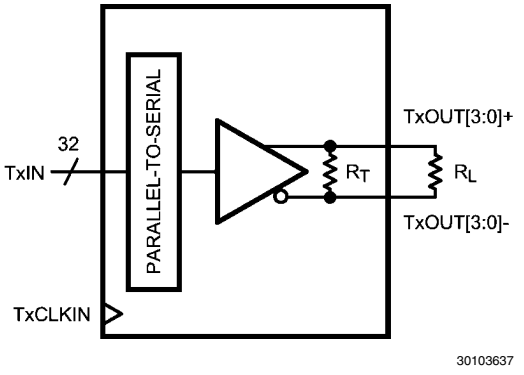


FIGURE 16. Serializer V_{OD} Test Circuit Diagram

查询"DS92LV3242"供应商

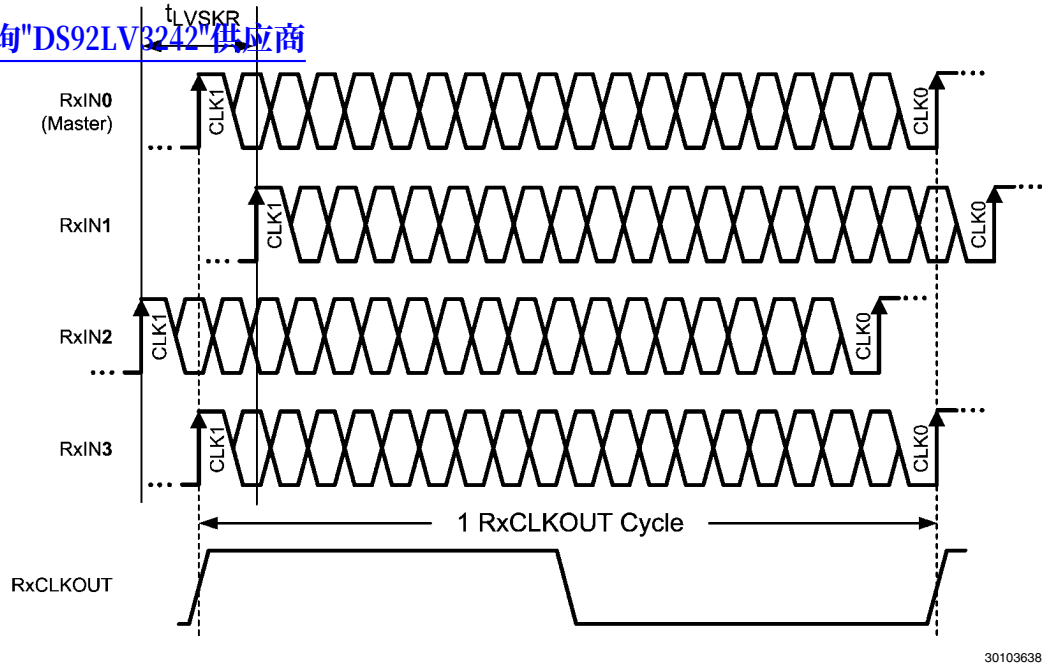


FIGURE 17. LVDS Deserializer Input Skew

查询"DS92LV3242"供应商

Functional Description

The DS92LV3241 Serializer (SER) and DS92LV3242 Deserializer (DES) chipset is a flexible SER/DES chipset that translates a 32-bit parallel LVCMOS data bus into a quad (4 pairs) or dual (2 pairs) LVDS serial links with embedded clock. The DS92LV3241 serializes the 32-bit wide parallel LVCMOS word into four or two high-speed LVDS serial data streams with embedded clock, scrambles and DC Balances the data to support AC coupling and enhance signal quality. The DS92LV3242 receives the dual/quad LVDS serial data streams and converts it back into a 32-bit wide parallel data with a recovered clock. The dual/quad LVDS serial data stream reduces cable size, the number of connectors, and eases skew concerns.

Parallel clocks between 20 MHz to 85 MHz are supported by the dual or quad operating modes. The modes are user selectable through a control pin on Serializer. In dual mode, the transmit clock frequency supports 20 MHz to 50 MHz and in quad mode the transmit clock frequency supports 40 MHz to 85 MHz. In the dual mode configuration, the embedded clock LVDS serial streams have an effective data payload of 640 Mbps (20MHz x 32-bit) to 1.6 Gbps (50MHz x 32- bit). In the quad mode configuration, the embedded clock LVDS serial streams have an effective data payload of 1.28 Gbps (40MHz x 32-bit) to 2.72 Gbps (85MHz x 32-bit). The SER/DES chipset is designed to transmit data over long distances through standard twisted pair (TWP) cables. The differential inputs and outputs are internally terminated with 100 ohm resistors to provide source and load termination, minimize stub length, to reduce component count and further minimize board space.

The DES can attain lock to a data stream without the use of a separate reference clock source; greatly simplifying system complexity and reducing overall cost. The DES synchronizes to the SER regardless of data pattern, delivering true automatic “plug-and-lock” performance. It will lock to the incoming serial stream without the need of special training patterns or special sync characters. The DES recovers the clock and data by extracting the embedded clock information, deskews the serial data channels and then deserializes the data. The DES also monitors the incoming clock information, determines lock status, and asserts the LOCK output high when lock occurs. In addition the DES also supports an optional AT-SPEED BIST (Built In Self Test) mode, BIST error flag, and LOCK status reporting pin. The SER and the DES have a power down control signal to enable efficient operation in various applications.

DESKEW AND CHANNEL ALIGNMENT

The DES automatically detects dual or quad serial channel mode and provides a clock alignment and deskew function without the need for any special training patterns. During the locking phase, the embedded clock information is recovered on all channels and the serial links are internally synchronized, de-skewed, and auto aligned. The internal CDR circuitry will dynamically compensate for up to 0.4 times the parallel clock period of per channel phase skew (channel-to-channel) between the recovered clocks of the serial links. This provides skew phase tolerance from mismatches in interconnect wires such as PCB trace routing, cable pair-to-pair length differences, and connector imbalances.

DATA TRANSFER

After SER lock is established (SER PLL to TxCLKIN), the inputs TxIN0–TxIN31 are latched into the encoder block. Data is clocked into the SER by the TxCLKIN input. The edge of TxCLKIN used to strobe the data is selectable via the R_FB (SER) pin. R_FB (SER) high selects the rising edge for clocking data and low selects the falling edge. The SER outputs (TxOUT[3:0]+/-) are intended to drive a AC Coupled point-to-point connections.

The SER latches 32-bit parallel data bus and performs several operations to it. The 32-bit parallel data is internally encoded and sequentially transmitted over the two high-speed serial LVDS channels. For each serial channel, the SER transmits 20 bits of information per payload to the DES. In the dual mode, the 32-bit parallel data is scaled and bit-mapped across two 20-bit data payloads per channel, resulting in a per channel throughput of 400 Mbps to 1.0 Gbps (20 bits x clock rate). Under quad mode, the internal PLL operates at ½ the input clock frequency rate. The 32 bits are bit-mapped and sequenced per every 2 cycles at ½ the TxCLKIN frequency across four channels, resutling in a per channel throughput of 400 Mbps to 850 Mbps (20 bits x clock rate/2). The chipset supports frequency ranges of 20 MHz to 85 MHz.

When all of the DES channels obtain lock , the LOCK pin is driven high and synchronously delivers valid data and recovered clock on the output. The DES locks to the clock, uses it to generate multiple internal data strobes, and then drives the recovered clock to the RxCLKOUT pin. The recovered clock (RxCLKOUT) is synchronous to the data on the RxOUT[31:0] pins. While LOCK is high, data on RxOUT[31:0] is valid. Otherwise, RxOUT[31:0] is invalid. The polarity of the RxCLKOUT edge is controlled by its R_FB (DES) input. RxOUT [31:0], LOCK and RxCLKOUT outputs will each drive a maximum of 8 pF load. REN controls TRI-STATE® for RxOUT0–RxOUT31 and the RxCLKOUT pin on the DES.

RESYNCHRONIZATION

In the absence of data transitions on one of the channels into the DES (e.g. a loss of the link), it will automatically try to resynchronize and re-establish lock using the standard lock sequence on the master channel (Channel 0). For example, if the embedded clock is not detected one time in succession on any of the serial links, the LOCK pin is driven low. The DES then monitors the master channel for lock, once that is obtained, the second channel is locked and aligned. The logic state of the LOCK signal indicates whether the data on RxOUT is valid; when it is high, the data is valid. The system may monitor the LOCK pin to determine whether data on the RxOUT is valid.

POWERDOWN

The Powerdown state is a low power sleep mode that the SER and DES may use to reduce power when no data is being transferred. The respective PDB pins are used to set each device into power down mode, which reduces supply current into the µA range. The SER enters Powerdown when the SER PDB pin is driven low. In Powerdown, the PLL stops and the outputs go into TRI-STATE®, disabling load current and reducing current supply. To exit Powerdown, SER PDB must be driven high. When the SER exits Powerdown, its PLL must lock to TxCLKIN before it is ready for sending data to the DES. The system must then allow time for the DES to lock before data can be recovered.

The DES enters Powerdown mode when DES PDB is driven low. In Powerdown mode, the PLL’s stop and the outputs enter TRI-STATE®. To bring the DES block out of the Powerdown state, the system drives DES PDB high. Both the SER and DES must relock before data can be transferred from Host and received by the Target. The DES will startup and assert LOCK high when it is locked to the embedded clocks. See also *Figure 13*.

TRI-STATE®

For the SER, TRI-STATE® is enabled when the SER PDB pin is driven low. This will TRI-STATE® the driver output pins on TxOUT[3:0]+/-. In addition, when MODE=0 (dual mode), the TxOUT[3:2]+/- outputs pins are in TRI-STATE®.

When you drive the REN or DES PDB pin low, the DES output pins (RxOUT[31:0]) and RxCLKOUT will enter TRI-STATE®. The LOCK output remains active, reflecting the state of the PLL. The DES input pins are high impedance during receiver Powerdown (DES PDB low) and power-off (VDD = 0V). See also *Figure 13*.

TRANSMIT PARALLEL DATA AND CONTROL INPUTS

The DS92LV3241 operates on a core supply voltage of 3.3V with an optional digital supply voltage for 1.8V, low-swing, input support. The SER single-ended (32-bit parallel data and control inputs) pins are 1.8V and 3.3V LVCMOS logic level compatible and is configured through the IOVDD input supply rail. If 1.8V is required, the IOVDD pin must be connected to a 1.8V supply rail. Also when power is applied to the transmitter, IOVDD pin must be applied before or simultaneously with other power supply pins (3.3V). If 1.8V input swing is not required, this pin should be tied to the common 3.3V rail. During normal operation, the voltage level on the IOVDD pins must not change.

PRE-EMPHASIS

The SER LVDS Line Driver features a Pre-Emphasis function used to compensate for extra long or lossy transmission media. The same amount of Pre-Emphasis is applied on all of the enabled differential output channels. Cable drive is enhanced with a user selectable Pre-Emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance will be limited by the loss characteristics and quality of the media.

To enable the Pre-Emphasis function, the “PRE” pin requires one external resistor (Rpre) to VSS (GND) in order to set the pre-emphasized current level. Options include:

1. Normal Output (no Pre-emphasis) – Leave the PRE pin open, include an R pad, do not populate.
2. Enhanced Output (Pre-emphasis enabled) – connect a resistor on the PRE pin to Vss.

Values of the Rpre Resistor should be between 12K Ohm and 100K Ohm. Values less than 6K Ohm should not be used. The amount of Pre-Emphasis for a given media will depend on the transmission distance and Fmax of the application. In general, too much Pre-Emphasis can cause over or undershoot at the receiver input pins. This can result in excessive noise, crosstalk, reduced Fmax, and increased power dissipation. For shorter cables or distances, Pre-Emphasis is typically not be required. Signal quality measurements should be made at the end of the application cable to confirm the proper amount of Pre-Emphasis for the specific application.

The Pre-Emphasis circuit increases the drive current to I = 48 / (R_{PRE}). For example if R_{PRE} = 15 kOhms, then the current is increased by an additional 3.2 mA. To calculate the expected increase in V_{OD}, multiply the increase in current by 50 ohms. So for the case of R_{PRE} = 15 kOhms, the boost to V_{OD} would be 3.2 mA x 50 Ohms = 160 mV. The duration of the current is controlled to one bit by time. If more than one bit value is repeated in the next cycle(s), the Pre-Emphasis current is turned off (back to the normal output current level) for the next bit(s). To boost high frequency data and pre-equalize teh data patternreduce ISI (Inter-Symbol Interference) improving the resulting eye pattern.

V_{OD} SELECT

The SER Line Driver Differential Output Voltage (V_{OD}) magnitude is selectable. Two levels are provided and are selected by the VSEL pin. When this pin is LOW, normal output levels are obtained. For most application set the VSEL pin LOW. When this pin is HIGH, the output current is increased to double the V_{OD} level. Use this setting only for extra long cables or high-loss interconnects.

VOD Control

VSEL Pin Setting	Effect
LOW	Small V_{OD}, typ 440 mV_{P-P}
HIGH	Large V_{OD}, typ 850 mV_{P-P}

SERIAL INTERFACE

The serial links between the DS92LV3241 and the DS92LV3242 are intended for a balanced 100 Ohm interconnects. The links **must** be configured as an AC coupled interface.

The SER and DES support AC-coupled interconnects through an integrated DC balanced encoding/decoding scheme. An external AC coupling capacitors must be placed, in series, in the LVDS signal path. The DES input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal common mode voltage (VCM) to +1.8V.

For the high-speed LVDS transmission, small footprint packages should be used for the AC coupling capacitors. This will help minimize degradation of signal quality due to package parasitics. NPO class 1 or X7R class 2 type capacitors are recommended. 50 WVDC should be the minimum used for best system-level ESD performance. The most common used capacitor value for the interface is 100 nF (0.1 uF) capacitor. One set of capacitors may be used for isolation. Two sets (both ends) may also be used for maximum isolation of both the SER and DES from cable faults.

The DS92LV3241 and the DS92LV3242 differential I/O’s are internally terminated with 100 Ohm resistance between the inverting and non-inverting pins and do not require external termination. The internal resistance value will be between 90 ohm and 130 ohm. The integrated terminations improve signal integrity, reduce stub lengths, and decrease the external component count resulting in space savings.

AT-SPEED BIST FEATURE

The DS92LV3241/ DS92LV3242 serial link is equipped with built-in self-test (BIST) capability to support both system manufacturing and field diagnostics. BIST mode is intended to check the entire high-speed serial interface at full link-speed without the use of specialized and expensive test equipment. This feature provides a simple method for a system host to perform diagnostic testing of both SER and DES. The BIST function is easily configured through the SER BISTEN pin. When the BIST mode is activated, the SER generates a PRBS (pseudo-random bit sequence) pattern (2^7-1). This pattern traverses each lane to the DES input. The DS92LV3242 includes an on-chip PRBS pattern verification circuit that checks the data pattern for bit errors and reports any errors on the data output pins of the DES.

The AT-Speed BIST feature is enabled by setting the BISTEN to High on SER. The BISTEN input must be High or Low for 4 or more TxCLKIN clock cycles in order to activate or deactivate the BIST mode. An input clock signal for the Serializer TxCLKIN must also be applied during the entire BIST operation. Once BIST is enabled, all the Serializer data inputs (TxIN

查询 DS92LV3242 供应商

[31:0]) are ignored and the DES outputs (RxOUT[31:0]) are forced low. Next, the internal test pattern generator for each channel starts transmission of the BIST pattern from SER to DES. The DES BIST mode will be automatically activated by this sequence. A maximum of 128 consecutives clock symbols on DS92LV3242 DES is needed to detect BIST enable function. The BIST is implemented with independent transmit and receive paths for the four serial links. Each channel on the DES will be individually compared against the expected bit sequence of the BIST pattern.

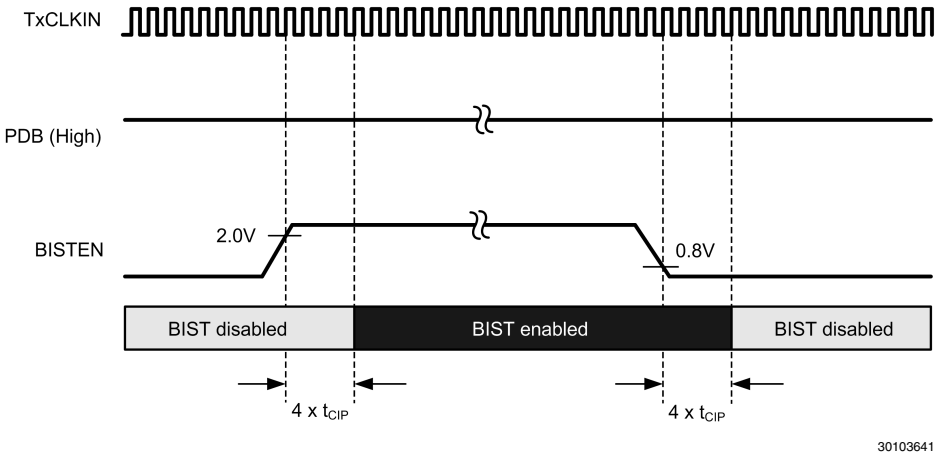


FIGURE 18. BIST Test Enabled/Disabled

Under the BIST mode, the DES parallel outputs on RxOUT [31:0] are multiplexed to represent BIST status indicators. The pass/fail status of the BIST is represented by a Pass flag along with an Error counter. The Pass flag output is designated on DES RxOUT0 for Channel 0, and RxOUT8 for Channel 1. The DES's PLL must first be locked to ensure the Pass status is valid. The output Pass status pin will stay LOW and then transition to High once 44*10^6 symbols are achieved across each of the respective transmission links. The total time duration of the test is defined by the following: 44*10^6 x tCIP . After the Pass output flags reach a HIGH state, it will not drop to LOW even if subsequent bit errors occurred after the BIST duration period. Errors will be reported if the input test pattern comparison does not match. If an error (miss-compare) occurs, the status bit is latched on RxOUT[7:1] for Channel 0, and RxOUT[15:9] for Channel 1; reflecting the number of errors detected. Whenever a data bit contains an error, the Error counter bit output for that corresponding channel goes HIGH. Each counter for the serial link utilizes a 7-bit counter to store the number of errors detected (0 to 127 max).

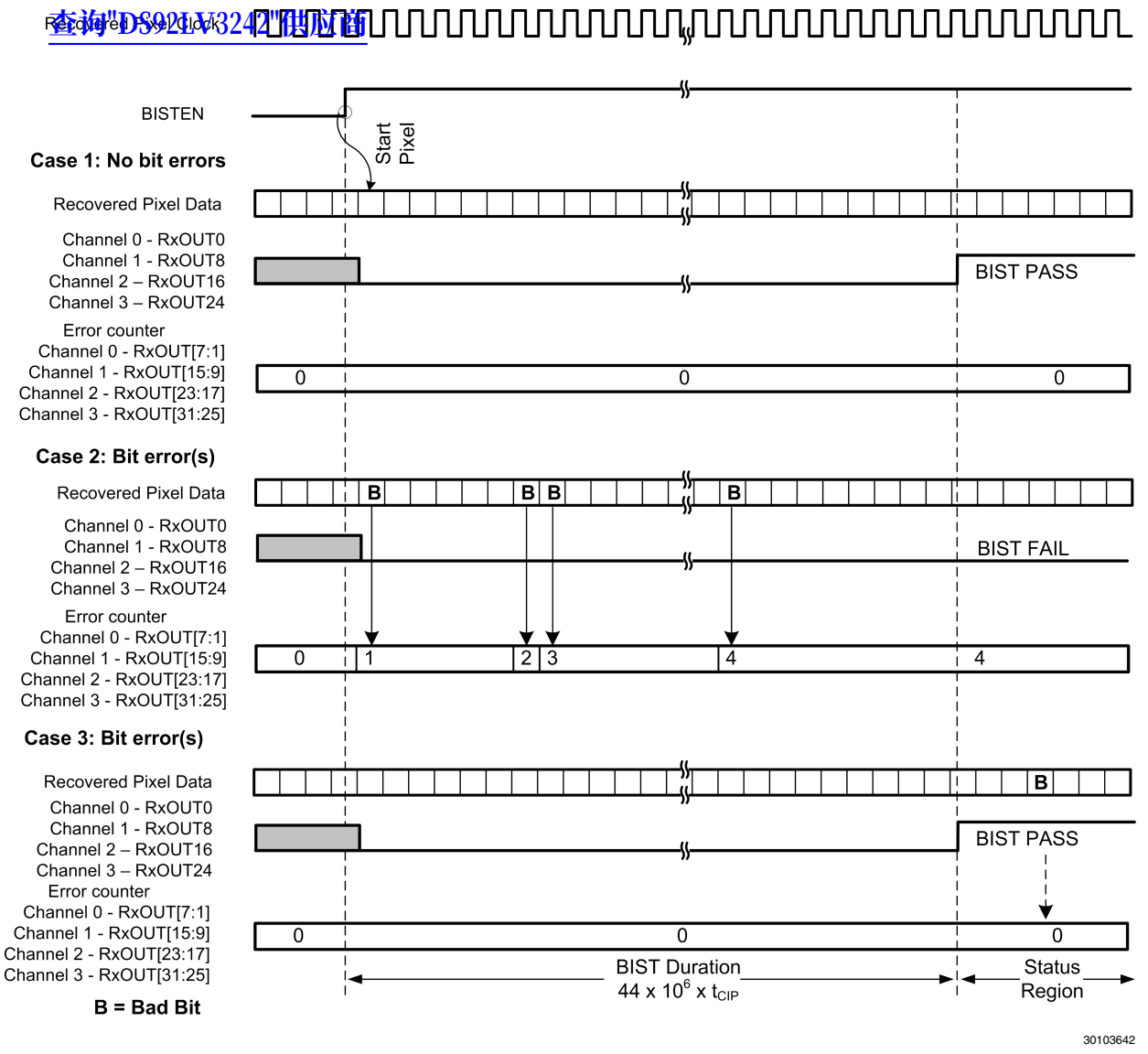


FIGURE 19. BIST Diagram for Different Bit Error Cases

TYPICAL APPLICATION CONNECTION

Figure 20 shows a typical application of the DS92LV3241 Serializer (SER). The differential outputs utilize 100nF coupling capacitors to the serial lines. Bypass capacitors are placed near the power supply pins. A system GPO (General Purpose Output) controls the PDB and BISTEN pins. In this application the R_FB (SER) pin is tied Low to latch data on the falling edge of the TxCLKIN. In this application the link is short, therefore the VSEL pin is tied LOW for the standard output swing level. The Pre-emphasis input utilizes a resistor to ground to set the amount of pre-emphasis desired by the application.

Configuration pins for the typical application are shown for SER:

- PDB – Power Down Control Input – Connect to host or tie HIGH (always ON)
- BISTEN – Mode Input - tie LOW if BIST mode is not used, or connect to host
- VSEL – tie LOW for normal VOD magnitude (application dependant)
- MODE – For clock rates between 20 MHz and 50 MHz tie LOW, for 40 MHz to 85 MHz tie HIGH
- PRE – Leave open if not required (have a R pad option on PCB)
- RSVD1 & RSVD2 – tie LOW

There are eight power pins for the device. These may be bussed together on a common 3.3V plane (3.3V LVCMOS I/O interface). If 1.8V input swing level for parallel data and control pins are required, connect the IOVDD pin to 1.8V. At a minimum, eight 0.1uF capacitors should be used for local bypassing.

查询"DS92LV3242"供应商

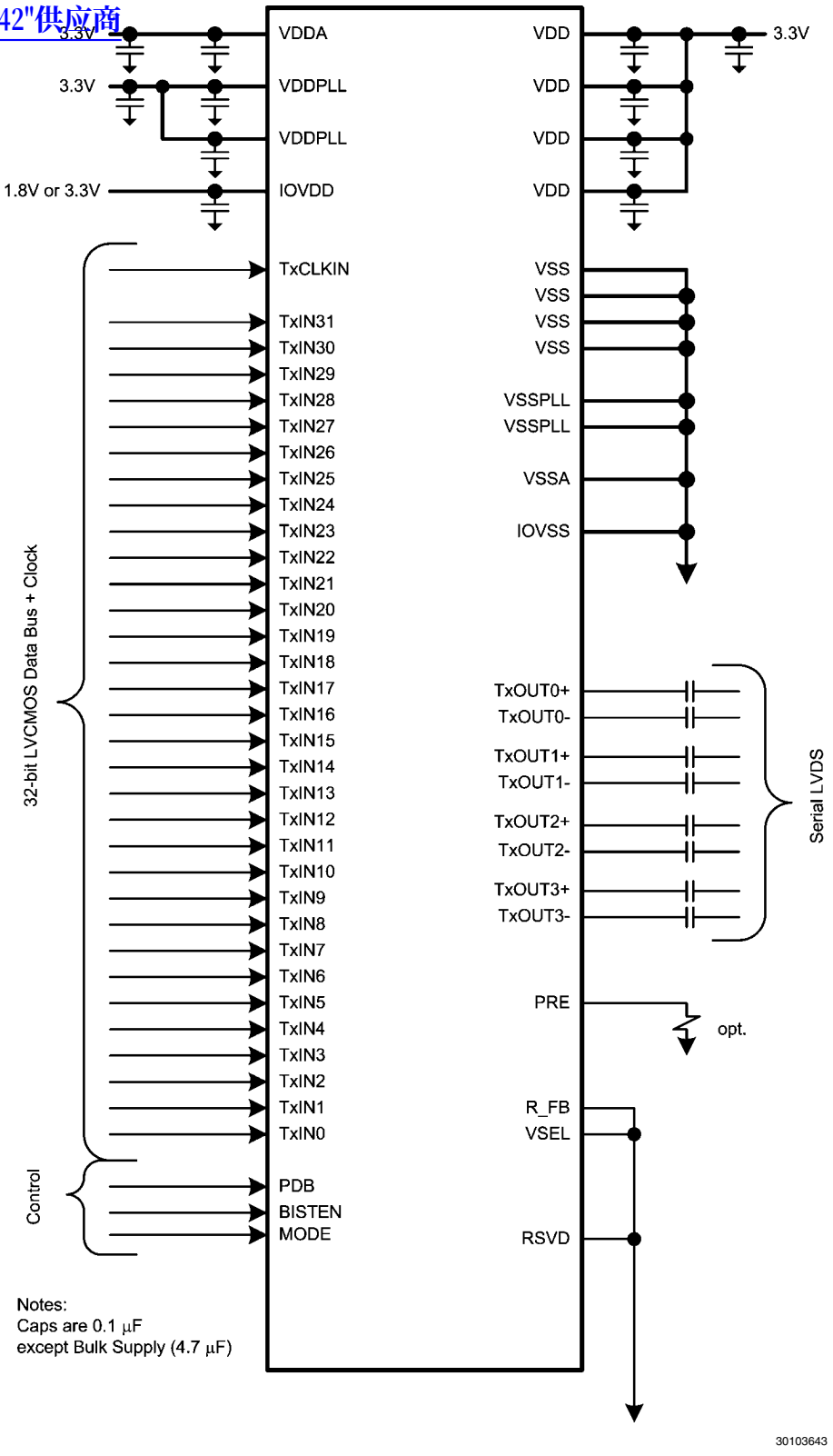


FIGURE 20. DS92LV3241 Typical Connection Diagram

Figure 21 shows a typical application of the DS92LV3242 Deserializer (DES). The differential inputs utilize 100nF coupling capacitors in the serial lines. Bypass capacitors are placed near the power supply pins. A system GPO (General Purpose Output) controls the PDB pin. In this application the R_FB (DES) pin is tied Low to strobe the data on the falling

edge of the RxCLKOUT. The REN signal is not used and is tied High also.

查询"DS92LV3242"供应商

Configuration pins for the typical application are shown for DES:

- PDB – Power Down Control Input – Connect to host or tie HIGH
- REN – tie HIGH if not used (used to MUX two DES to one target device)
- RSVD – tie LOW

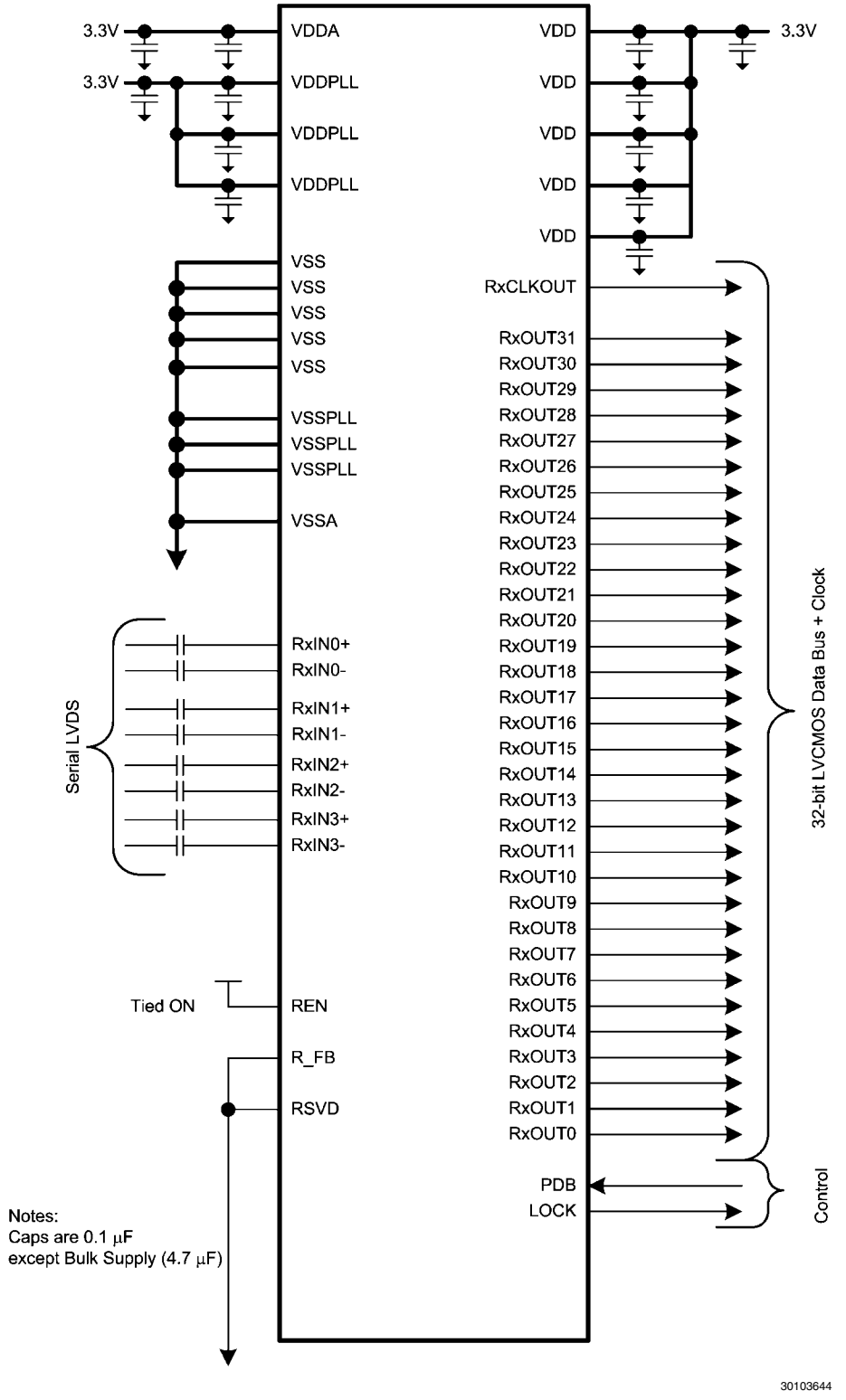


FIGURE 21. DS92LV3242 Typical Connection Diagram

Applications Information

查询"DS92LV3242"供应商

TRANSMISSION MEDIA

The SER and DES are used in AC-coupled point-to-point configurations, through a PCB trace, or through twisted pair cables. Interconnect for LVDS typically has a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. In most applications that involve cables, the transmission distance will be determined on data rates involved, acceptable bit error rate and transmission medium.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS SER/DES devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz range. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

PLUG AND GO

The Serializer and Deserializer devices support hot plugging of the serial interconnect. The automatic receiver lock to random data “plug & go” capability allows the DS92LV3242 to obtain lock to the active data stream during a live insertion event.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

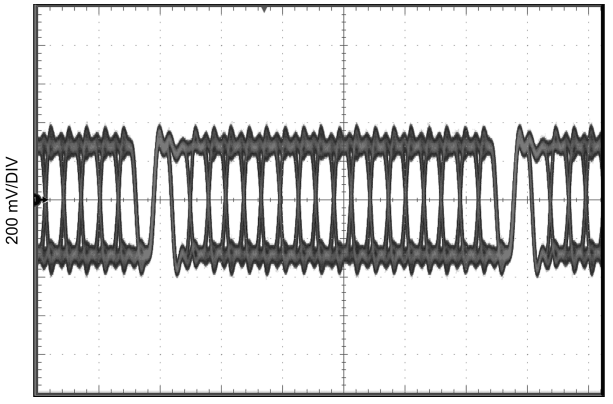
- Use 100 Ohm coupled differential pairs
- Use the S/2S/3S rule in spacings
  —S = space between the pair
  —2S = space between pairs
  —3S = space to LVCMOS signal
- Minimize the number of vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner’s Manual - available in PDF format from the National web site at: **www.national.com/lvds**

查询 DS92LV3242 供应商

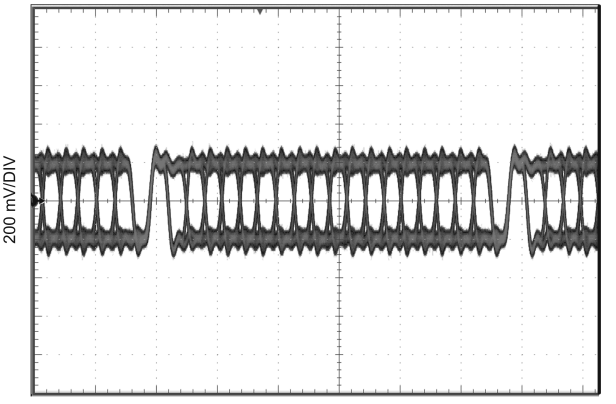
Typical Performance Characteristics

The waveforms below illustrate the typical performance of the DS92LV3241. The SER was given a PCLK and configured as described below each picture. In all of the pictures the SER was configured with BISTEN pin set to logic HIGH. Each waveform was taken by using a high impedance low capacitance differential probe to probe across a 100 ohm differential termination resistor within one inch of TxOUT0+/-.



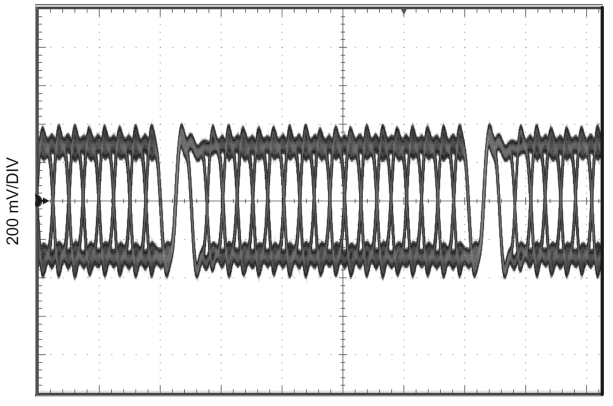
30103652

Serial Output Quad Mode, 85 MHz, VSEL = H, No Pre-Emphasis



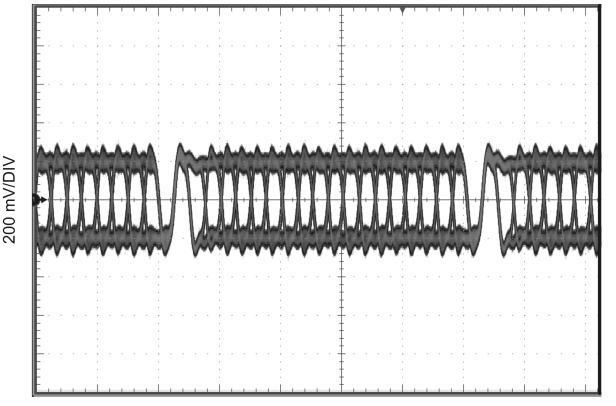
30103653

Serial Output Quad Mode, 85 MHz, VSEL = L, No Pre-Emphasis



30103654

Serial Output Dual Mode, 50 MHz, VSEL = H, No Pre-Emphasis

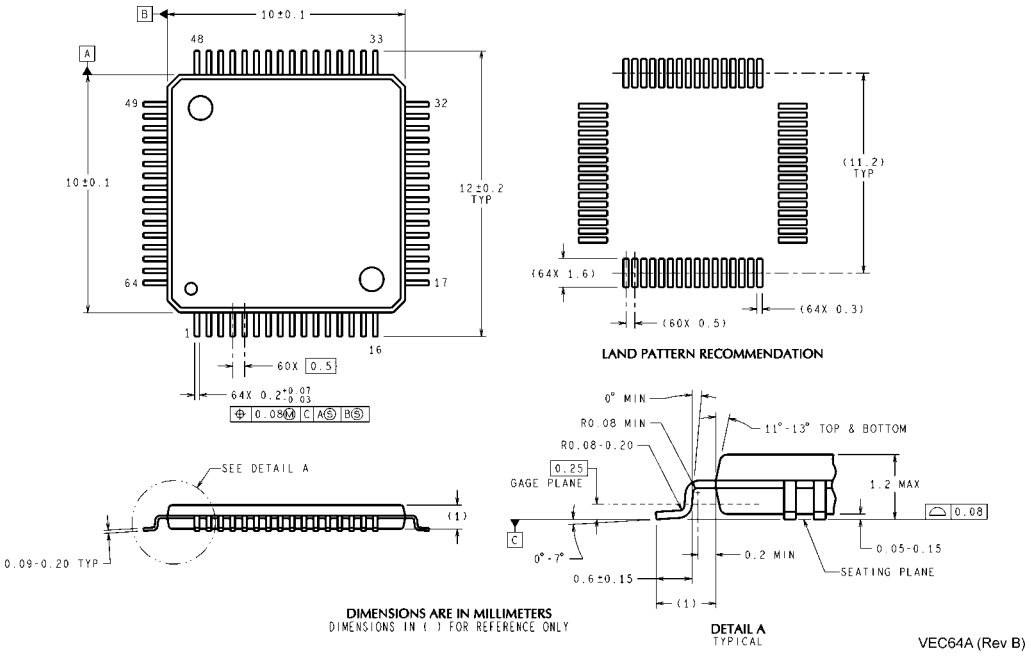


30103655

Serial Output Dual Mode, 50 MHz, VSEL = L, No Pre-Emphasis

Physical Dimensions inches (millimeters) unless otherwise noted

查询"DS92LV3242"供应商



Dimensions show in millimeters only
NS Package Number VEC64A

Ordering Information

NSID	Package Type	Package ID
DS92LV3241TVS	64-Lead TQFP style, 10.0 X 10.0 X 1.0 mm, 0.5 mm pitch	VEC64A
DS92LV3241TVSX	64-Lead TQFP style, 10.0 X 10.0 X 1.0 mm, 0.5 mm pitch	VEC64A
DS92LV3242TVS	64-Lead TQFP style, 10.0 X 10.0 X 1.0 mm, 0.5 mm pitch	VEC64A
DS92LV3242TVSX	64-Lead TQFP style, 10.0 X 10.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel	VEC64A

查询"DS92LV3242"供应商

Notes

查询"DS92LV3242"供应商

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2010 National Semiconductor Corporation

For the most current product information visit us at www.national.com

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com