Clock Generator Specification for AMD64 Processors

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Trademarks

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Revision History

Date	Revision	Changes
September 2003	3.08	Fourth Public release.
September 2003	3.07	Changed the title of the document to “Clock Generator Specification for AMD64 Processors” and changed references throughout the document.
November 2002	3.06	Third Public release.
November 2002	3.05	Added note in Table 2 for resistor strapping recommendation. Made changes in Table 3 for pin descriptions section of FS(2:0) signals.
November 2002	3.04	Changed the title of the document to “Clock Generator Specification for AMD Athlon™ 64 and AMD Opteron™ Processors” and changed references throughout the document.
September 2002	3.03	Second Public release.
September 2002	3.02	Internal revision.
August 2002	3.01	Changed the title of the document to “Clock Generator Specification for AMD Athlon™ and AMD Opteron™ Processors Based on Hammer Technology” and changed references throughout the document.
August 2002	3.00	Initial Public release.

Chapter 1 Description

This specification is intended to provide a definition of the minimum set of requirements for the first AMD64 processors system clock generators.

1.1 Specification Overview

The goal of this specification is

- to provide enough information to enable development of clock generators for the AMD64 processors
- to provide the definition of a minimum feature set for a clock generator that enables initial platform shipments
- to allow clock generator vendors the flexibility to provide product differentiation above and beyond this minimum feature set
- to provide backward compatibility with AMD Athlon™ processor-based platforms

1.2 Pin-Strapped Configuration

Upon power up, the device samples the input states of various configuration input pins to define the correct operating state without the need for software configuration through the I^2C interface. The I^2C interface to internal configuration registers provides a method to optimize the operating state of the clock generator.

***Note**: Changes made through the I^2C interface will override the hardware pin strapped configuration.*

1.3 Processor Frequency Selection and Spread Spectrum Clocking

Processor frequency selection of 100, 133, 166, and 200 MHz are defined from hardware-sampled inputs. Additional frequencies and operating states (combinations of processor frequency and spread spectrum clocking features) can be selected through the I^2C programmable interface. The specified features in this specification provide a minimum set for AMD64 processor-based platforms. Additional features may be provided at the discretion of the clock generator manufacturer.

Spread spectrum modulation (down-spread only) is required for all outputs derived from the internal processor PLL as shown in Figure 1 on page 7. This includes the processor, PCI33 and PCI33_HT66 outputs. The REF, USB, and 24_48 MHz clocks are not affected by spread spectrum control. The spread spectrum requirements include the ability to enable and disable 0.5% down spread clocking. A 0.5% down spread, 33-kHz triangular modulation is required and

other spread amounts less than 0.5% down spread and less than 50 kHz Δf/Δt modulation are left to the clock generator vendor to include as differentiating features.

1.3.1 Reserved Test Mode Operating States

This specification defines two test modes and reserves one other for the purpose of providing required system debug and system test operating modes. The reserved manufacturer test mode is provided for each clock vendor to implement an operating mode specific to their own production test flow needs and is not required for system operation.

1.4 Differential Push-Pull Processor Clock Outputs

This clock generator is specified to provide push-pull driver type differential outputs for the processor clocks (2-pair) instead of the common open drain style used for AMD Athlon processor-based platforms. This provides a more testable product and results in less variation in edge rate and differential skew as seen by the processor. The processor clock termination scheme has been derived such that 15–55 ohm, 3.3-V output drivers can be used for the processor clocks.

1.5 Selectable 33-MHz or 66-MHz Clock Outputs

This clock generator specification defines a number of clock outputs that are selectable between 33 MHz and 66 MHz. This selection provides flexibility across platforms that may implement a combination of 33-MHz PCI resources, 66-MHz PCI resources, and HyperTransport™ technology resources.

Note: *HyperTransport technology is the HyperTransport Technology Consortium's next generation interconnect technology that is designed for use with all AMD64 platforms.*

1.6 PCISTOP33_L Control Signal

This clock generator specification defines one asynchronous PCISTOP33_L signal that provides control for 33-MHz output clocks. Both the PCI33 and PCI33_HT66 clocks, while operating at 33MHz, must stop in response to PCISTOP33_L assertions. While operating at 66 MHz, the PCI33_HT66 outputs are not affected by PCISTOP33_L assertions.

The 33-MHz PCI clock outputs, once stopped, should be in the Low state and started with a full high-pulse width specified. The 33-MHz PCI clock outputs on latency cycles are only one rising PCI clock turned off. Latency is one PCI clock. Section 1.6.1 and Section 1.6.2 on page 7, along with Figure 1 on page 7 gives a description and timing diagram respectively, of the required timing sequence:

1.6.1 Starting the 33-MHz PCI Clocks

The 33MHz PCI clocks must be started using the following sequence of events:

1. On a given PCI clock rising edge, the PCISTOP33_L signal is asserted (first arrow from the left in the timing diagram).

2. On the next rising edge of the PCI clock, the clock synthesis chip samples PCIST0P33_L deasserted (second arrow from the left).

3. The PCI clocks start running with the next rising edge of the PCI clock (third arrow from the left).

1.6.2 Stopping the 33-MHz PCI Clocks

The 33-MHz PCI clocks must be stopped using the following sequence of events:

1. On a rising edge of the PCI clock, the PCISTOP33_L signal is asserted (4th arrow).

2. On the next rising edge of the PCI clock, the clock synthesis chip samples PCISTOP33_L asserted.

3. On the next falling edge of the PCI clock, the PCI clocks go Low and stay Low.

Figure 1 is a picture of the PCISTOP33_L control sequence. All numbered arrow references are counted from left to right.

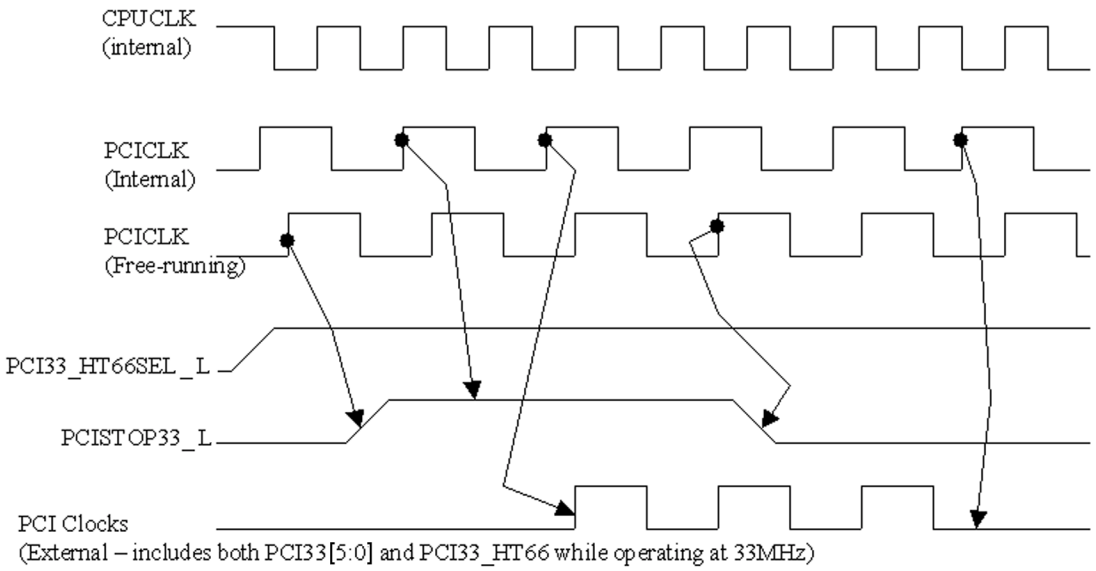

Figure 1. PCISTOP33_L Control Signal

Note: *The fifth arrow, from the left, shows there is no rising edge on the stopped PCI clocks.*

The following notes give additional information on the PCISTOP33_L control sequence.

Notes:

1. *All timing is referenced to internal CPUCLK.*
2. *PCISTOP33_L is an asynchronous input.*
3. *All other clocks continue to run undisturbed.*
4. *PCI33_HT66SEL_L is shown in the High state.*
5. *PCISTOP33_L must meet 10 ns setup/hold times.*

1.7 Input Reference Crystal Definition

The crystal inputs and pin loading should be compatible with 18-pF crystals.

1.8 Internal Input Pullup Resistors

This specification defines internal pullup resistors on most of the control inputs. The internal input pullup resistors allow the input pins to be left unconnected in applications where their function is unnecessary. Additionally, these input pullup resistors provide the required pullup for open drain-type outputs for SMBus. The general range of values is provided for these internal pullups.

1.9 Software Interface and Control

Software interface and control of the clock generator are described in Sections 1.9.1 and 1.9.2.

1.9.1 Hardware Selection with Software Programmable Overrides

Configuration of the features of the clock generator can be completed through hardware pin strapping alone or by hardware pin strapping with optimization of features through programmable registers accessed through the SMBus interface. The values of the programmable registers will override any hardware strapped settings, once the settings are changed.

1.9.2 Configuration Read-Back

The values of the programmable registers can be read back through the SMBus interface to allow the current operating state of the device to be determined.

Chapter 2 Features

This specification describes the main clock generator for AMD64 platforms. Table 1 describes the system clock features.

Table 1. System Clock Features

Features	Frequency	Type	Voltage
Two differential pair processor clocks	200-MHz, 166MHz, 133-MHz, or 100-MHz	Differential push-pull	3.3 V
Six PCI clocks	33-MHz	Push-pull	3.3 V
One free running PCI clock	33-MHz	Push-pull	3.3 V
Three AGP/HT clocks	33-MHz or 66 MHz	Push-pull	3.3 V
USBCLK	48-MHz	Push-pull	3.3 V
FDC clock	24-MHz or 48--MHz	Push-pull	3.3 V
Three Reference clocks	14.318-MHz	Push-pull	3.3 V

Additional features of the system clock are as follows:

- 3.3-V operation
- Two true differential processor clocks pairs (supports both 1P and 2P platforms)
- Seven 3.3-V dedicated 33-MHz PCI clocks, one free-running
- Three 3.3-V selectable 66-MHz or 33 MHz clocks to be used for HyperTransport™ technology reference clocks or PCI 33-MHz clocks
- One 3.3-V 48-MHz output for USB
- One 3.3-V 24-MHz or 48-MHz for SIO
- Three 3.3-V 14.318-MHz reference clocks (one additional to provide reference to external 24.576 MHz generator if needed for AC97 codecs)
- EMI Suppression using spread spectrum technology (down spread only with 33 kHz triangular modulation)
- SMbus interface for configuration register programming and read back (Rev 1.0)
- Power management control inputs
- A 48-pin SSOP

Chapter 3 Frequency Selections

This chapter contains frequency selections for the Clock Generator and they are shown in Table 2.

Table 2. Frequency Selections

Input Configuration						Processor (MHz)	PCI33 (MHz)	PCI33_HT66 (MHz)	24_48 (MHz)	14.318 (MHz)	Comment
FS2	FS1	FS0	PCI33_HT66 SEL_L	PCI STOP33_L	24_48SEL_L						
1	1	1	X	1	X	200	33	33 or 66	24 or 48	14.318	Normal AMD64 Processor Operation
1	1	0	X	1	X	166	33	33 or 66	24 or 48	14.318	Reserved

Notes:

1. *During bypass mode the X1 input pin can be driven with an external clock signal from 10 MHz to 100 MHz. This mode is used in system debug for frequency testing and is planned to be used in the smart burn-in systems for the AMD64 processors used for production burn-in capability.*
2. *These operating modes are reserved for vendor specific test requirements and may be different from vendor to vendor. These modes will not be used in the system.*
3. *In these cases, FS[2:0] is not equal to 000b or 001b.*
4. *It is highly recommended to connect an external pullup resistor and pull down resistor on signals FS[2:0] and 24_48SEL_L to ensure that these signals achieve the desired logic level and to determine the correct frequency selection under various loading and part leakage conditions. The value for the external pull up resistor should be 10 k ohm and the value for the external pull down resistor should be 1K ohm.*

Table 2. Frequency Selections (Continued)

Input Configuration						Processor (MHz)	PCI33 (MHz)	PCI33_HT66 (MHz)	24_48 (MHz)	14.318 (MHz)	Comment
FS2	FS1	FS0	PCI33_HT66 SEL_L	PCI STOP33_L	24_48SEL_L						
1	0	1	X	1	X	133	33	33 or 66	24 or 48	14.318	AMD Athlon™ processor compatible
1[4]	0	0	X	1	X	100	33	33 or 66	24 or 48	14.318	AMD Athlon processor compatible
0	1	1	X	1	X	—	—	—	—	—	Reserved[2]
0	1	0	X	1	X	—	—	—	—	—	Reserved[2]
0	0	1	1	1	X	X1 input (pin3)	=X1 / 6 (pin3)	=X1 / 6 (pin3)	0	0	Bypass mode for bring up and mfgr test[1]
0	0	1	0	1	X	X1 input	=X1 / 6	=X1 / 3	0	0	Bypass mode for bring up and mfgr test[1]

Notes:

1. *During bypass mode the X1 input pin can be driven with an external clock signal from 10 MHz to 100 MHz. This mode is used in system debug for frequency testing and is planned to be used in the smart burn-in systems for the AMD64 processors used for production burn-in capability.*
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Table 2. Frequency Selections (Continued)

Input Configuration						Processor (MHz)	PCI33 (MHz)	PCI33_HT66 (MHz)	24_48 (MHz)	14.318 (MHz)	Comment
FS2	FS1	FS0	PCI33_HT66 SEL_L	PCI STOP33_L	24_48SEL_L						
0	0	0	X	1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Tri-state mode for board level test
X	X	X	0	1	X	100, 133, 166 or 200	33	66	24 or 48	14.318	33 MHz vs. 66 MHz output select[3]
X	X	X	1	1	X	100,133 , 166, or 200	33	33	24 or 48	14.318	33 MHz vs. 66 MHz output select[3]

Notes:

1. *During bypass mode the X1 input pin can be driven with an external clock signal from 10 MHz to 100 MHz. This mode is used in system debug for frequency testing and is planned to be used in the smart burn-in systems for the AMD64 processors used for production burn-in capability.*
2. *These operating modes are reserved for vendor specific test requirements and may be different from vendor to vendor. These modes will not be used in the system.*
3. *In these cases, FS[2:0] is not equal to 000b or 001b.*
4. *It is highly recommended to connect an external pullup resistor and pull down resistor on signals FS[2:0] and 24_48SEL_L to ensure that these signals achieve the desired logic level and to determine the correct frequency selection under various loading and part leakage conditions. The value for the external pull up resistor should be 10 k ohm and the value for the external pull down resistor should be 1K ohm.*

Table 2. Frequency Selections (Continued)

Input Configuration						Processor (MHz)	PCI33 (MHz)	PCI33_HT66 (MHz)	24_48 (MHz)	14.318 (MHz)	Comment
FS2	FS1	FS0	PCI33_HT66 SEL_L	PCI STOP33_L	24_48SEL_L						
X	X	X	X	1	1	100, 133, 166 or 200	33	33 or 66	24	14.318	24 vs. 48 MHz output select[3]
X	X	X	X	1	0	100, 133, 166, or 200	33	33 or 66	48	14.318	24 vs. 48 MHz output select[3]
X	X	X	0	0	X	100, 133, 166, 200	0	66	24 or 48	14.318	PCISTOP vs. 33 MHz and 66 MHz selects[3]

Notes:

1. *During bypass mode the X1 input pin can be driven with an external clock signal from 10 MHz to 100 MHz. This mode is used in system debug for frequency testing and is planned to be used in the smart burn-in systems for the AMD64 processors used for production burn-in capability.*
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Table 2. Frequency Selections (Continued)

Input Configuration						Processor (MHz)	PCI33 (MHz)	PCI33_HT66 (MHz)	24_48 (MHz)	14.318 (MHz)	Comment
FS2	FS1	FS0	PCI33_HT66 SEL_L	PCI STOP33_L	24_48SEL_L						
X	X	X	0	1	X	100, 133, 166, 200	33	66	24 or 48	14.318	PCISTOP vs. 33 MHz and 66 MHz selects[3]
X	X	X	1	0	X	100, 133, 166, 200	0	0	24 or 48	14.318	PCISTOP vs. 33 MHz and 66 MHz selects[3]
X	X	X	1	1	X	100. 133, 166, 200	33	33	24 or 48	14/318	PCISTOP vs. 33 MHz and 66 MHz selects[3]

Notes:

1. *During bypass mode the X1 input pin can be driven with an external clock signal from 10 MHz to 100 MHz. This mode is used in system debug for frequency testing and is planned to be used in the smart burn-in systems for the AMD64 processors used for production burn-in capability.*
2. *These operating modes are reserved for vendor specific test requirements and may be different from vendor to vendor. These modes will not be used in the system.*
3. *In these cases, FS[2:0] is not equal to 000b or 001b.*
4. *It is highly recommended to connect an external pullup resistor and pull down resistor on signals FS[2:0] and 24_48SEL_L to ensure that these signals achieve the desired logic level and to determine the correct frequency selection under various loading and part leakage conditions. The value for the external pull up resistor should be 10 k ohm and the value for the external pull down resistor should be 1K ohm.*

Chapter 4 Logic Block Diagram

This chapter and Figure 2 illustrate the processor clock logic.

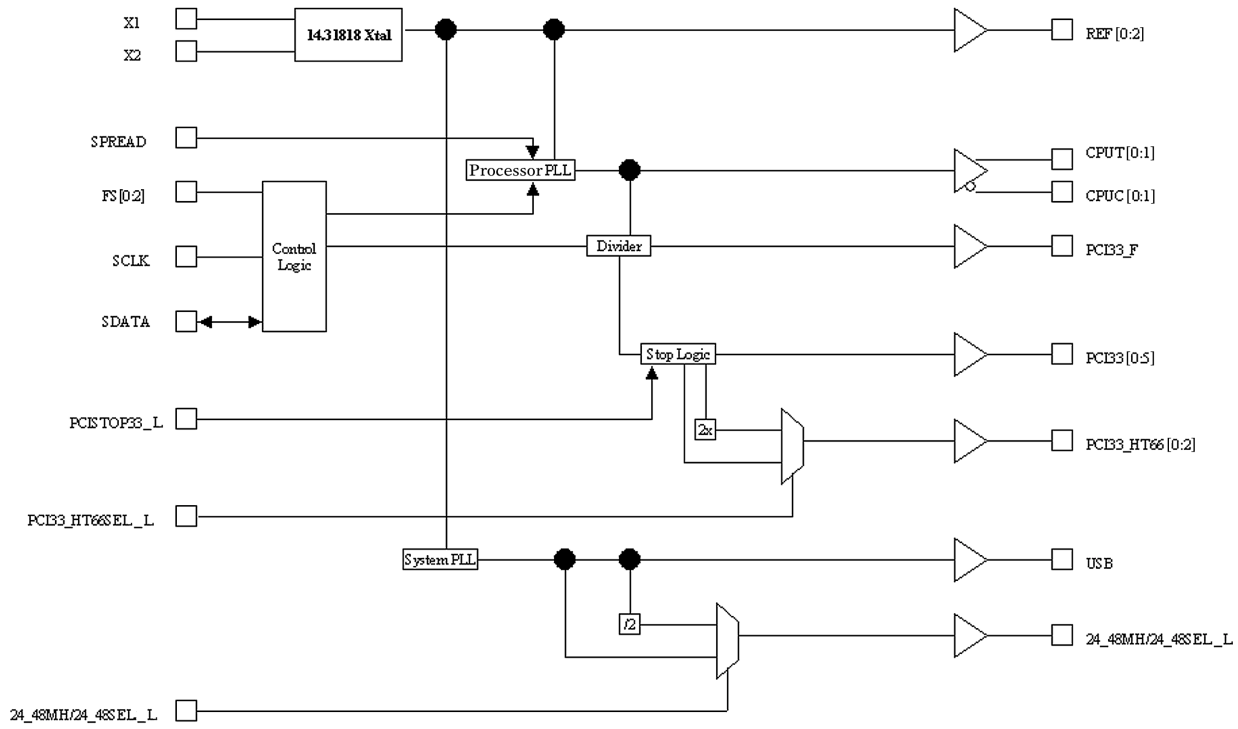

Figure 2. Processor Clock Logic Block Diagram

Chapter 5 Pin Locations and Descriptions

Table 3 contains the pin descriptions for the Clock Generator.

Table 3. Pin Locations and Descriptions

Name	Pin	No. of Pins	Type	Pin Description
X1	3	1	I	**Crystal Connection or External Reference:** Reference crystal input or external reference clock input. This pin should include an internal 36-pF load capacitance to eliminate the need for external load capacitance.
X2	4	1	O	**Crystal Connection:** Reference crystal feedback. This output should include an internal 36-pF load capacitance to eliminate the need for external load capacitance.
CPUT[1:0]	41 37	2	O	**Processor Clock Outputs 1 and 0:** Processor push-pull "True" clock outputs of the differential pair. Requires external termination.
CPUC[1:0]	40 36	2	O	**Processor Clock Outputs 1 and 0:** Processor push-pull "Complimentary" clock outputs of the differential pair. Requires external termination.
PCI33_F	23	1	O	**3.3V Free-Running PCI Clock Output:** The free-running PCI clock pin operates at 33-MHz. The free-running PCI clock is not turned off when PCISTOP33_L is activated Low.
PCI33[5:0]	13 14 17 18 21 22	6	O	**3.3V PCI Clock Outputs:** PCI clocks operate at 33 MHz.
PCI33_HT66[2:0]	7 8 11	3	O	**3.3V PCI 33 MHz or HyperTransport™ Link 66 MHz Outputs:** This group of outputs is selectable between 33 MHz and 66 MHz based upon the state of PCI33_HT66SEL_L. When running 66 MHz, these outputs are for use as reference clocks to HyperTransport technology-based devices.

Table 3. Pin Locations and Descriptions (Continued)

Name	Pin	No. of Pins	Type	Pin Description
PCI33_HT66SEL_L	6	1	I	**PCI33_HT66 MHz Select:** This input selects the output frequency of PCI33_**HT**66 outputs to either 33 MHz or 66 MHz. This input pin is dedicated to avoid corruption of the input state due to PCI add-in cards that may have termination resistors on the input clocks. This input must have a weak (100K) internal pullup resistor. This pin externally strapped low using a 10 K ohm resistor to select if the 66 Mhz outputs are desired. **Low = 66 MHz outputs, High = 33 MHz outputs**
USB	31	1	O	**3.3-V USB Clock Output:** Fixed clock output at 48-MHz.
24_48MHz/24_48SEL_L	28	1	I/O	**3.3-V Super I/O clock output:** The Super I/O clock may be strapped for 24-MHz or 48-MHz. This input must have a weak (100K) internal pullup. This pin will be externally strapped low using a 10 K ohm if the 48 MHz output is desired. **Low = 48 MHz output, high = 24 MHz output**
REF[0:2]/FS[0:2]	1 45 48	3	I/O	**3.3V Reference Clock Outputs:** Fixed clock output at 14.318 MHz . **Frequency Select Inputs:** Power-On strapping to set device operating frequency as described in Table 2 on page 11. These inputs must have weak (100 K) internal pullup resistors. See Notes in Table 2 on page 11 for resistor strapping recommendation.
SPREAD	44	1	I	**Spread Spectrum Clocking Enable:** Power-On strapping that sets spread spectrum clocking as enabled or disabled. This input allows the default spread spectrum-clocking mode to be enabled or disabled upon power up. This input must have a weak (100K) internal pullup resistor. This pin is externally strapped low using a 10 K ohm resistor if spread disabled is desired. **Low=disable, High=enable.** ***Note:*** *all AMD Athlon™ processors and AMD64 processor-based systems are recommended for use with SSC, therefore the default of this pin is enabled and should only be turned off for debug and test purposes.*

Table 3. Pin Locations and Descriptions (Continued)

Name	Pin	No. of Pins	Type	Pin Description
PCISTOP33_L	24	1	I	**Control for PCI33[0:5] and PCI33_HT66[0:2] outputs operating at 33-MHz:** Active-Low control input to halt all 33-MHz PCI clocks except the free-running clock. This input must have a weak internal pullup resistor (100 K). Once this input has been asserted, the PCI33 outputs and PCI33_HT66 outputs operating at 33MHz must stop in the Low state according to the timing diagram outlined in Section 1.6.2 on page 7 and must not violate the output duty cycle requirements until stopped (no glitches or runt cycles). **Low = stop, High = running.**
NC	12	1		Pin reserved for vendor specific features.
SDATA	26	1	I/O	Data pin for I^2C circuitry (SM Bus Rev1.0). This input should have weak internal pullup resistor (100 K). In this case, no external pullup resistors would be required. SDATA is a 5.0-V tolerant I/O. ***Note Option:*** *If CLK vendor only supports 3.3-V tolerant I/O, they must provide an application note in their spec on how to handle a 5V SMBus (i.e., clamp circuit on the motherboard).*
SCLK	25	1	I	Clock pin for I^2C circuitry (SM Bus Rev1.0). This input must have weak internal pullup resistors (100K). In this case, no external pullup resistors would be required. SCLK must be a 3.3-V signal-tolerant I/O but not 5.0-V tolerant..
VDD	2 9 16 19 29 35 38 46	8	P	**Power Connection:** Connected to 3.3 V power supply. Used to supply digital portions of the chip.

Table 3. Pin Locations and Descriptions (Continued)

Name	Pin	No. of Pins	Type	Pin Description
GND	5 10 15 20 27 30 34 39 47	9	G	**Power Connection:** Connected directly to GND on the motherboard. Used to ground digital portions of the chip.
VDDA	43	1	P	**Analog VDD:** Connected to 3.3-V power supply through a filter on the motherboard. Used to supply the main PLL on the chip**.**
GNDA	42	1	G	**Analog GND:** Connected directly to GND on the motherboard. Used to ground the main PLL on the chip.
VDDF	32	1	P	**Analog VDD for 48-MHz PLL:** Connected to 3.3-V power supply through a filter on the motherboard. Used to supply the 48-MHz PLL on the chip.
GNDF	33	1	G	**Analog GND for 48-MHz PLL:** Connected directly to GND on the motherboard. Used to ground the 48-MHz PLL on the chip.

Chapter 6 Package Pinout – 48-Pin SSOP

The package pinout for a 48-pin SSOP package is defined to maximize performance. The package pinout provides grouped VDD and GND pin pairs to maximize mutual coupling and to equalize the distribution losses to each rail as seen at each signal location. The pinout includes dedicated VDDA and GNDA signals to supply the variable PLL and VDDF and GNDF signals to supply the fixed PLL. Figure 3 illustrates the SSOP package pinout.

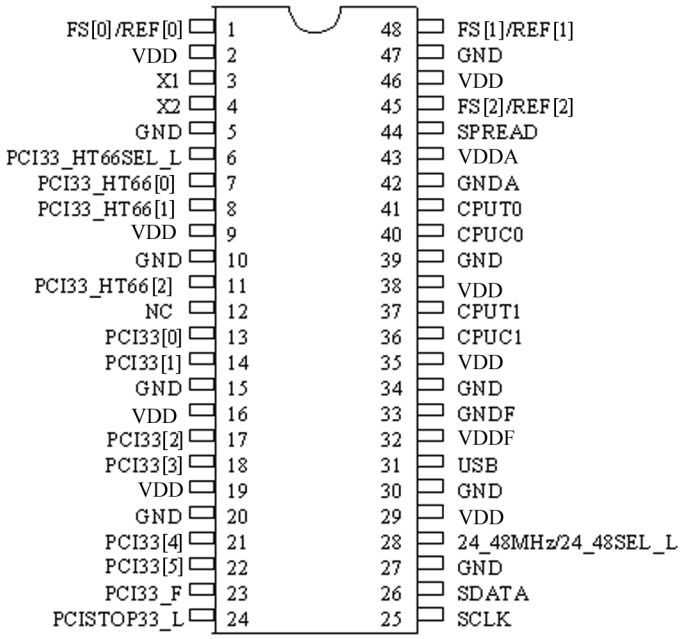

Figure 3. SSOP Package Pinout

Chapter 7 Electrical Specifications

This chapter contains the electrical specifications for the clock generator.

7.1 Absolute Maximum Ratings

The absolute maximum ratings define the maximum non-operating conditions beyond which predictable operation of the device might be impaired. The device should not be subjected to conditions outside these ranges under any circumstances.

Table 4 describes the absolute maximum voltage, temperature, and ESD rating for the part.

Table 4. Absolute Maximum Ratings

Parameter	Description	Rating	Unit
VDD, VDDA, VDDF	Supply Voltage	–0.5 to 3.8	V
V_{IN}	Input Voltage	–0.5 to 3.8	V
T_{STG}	Storage Temp	–65 to +150	°C
ESD $_{PROT}$	Input ESD Protection using Human Body Model	>2	kV

7.2 Operating Conditions

Table 5 describes the normal operating conditions of the part.

Table 5. Operating Conditions

Parameter	Description	Min.	Typical	Max.	Unit
VDD, VDDA, VDDF	Analog and digital supply voltages	3.135		3.465	V
T_A	Operating temperature, ambient	0		70	°C
$F_{(Input)}$	Input frequency (crystal or reference)	10	14.318	16	MHz

7.3 Electrical Characteristics

The electrical characteristics of the device define the electrical parameters and the ranges over which the device must operate. These characteristics are grouped per input or output type. These electrical characteristics must be maintained over the operating conditions shown in Table 5 on page 25.

7.3.1 Logic Inputs

The logic input electrical characteristics are described in Table 6.

The input pins are PCI33_HT66SEL_L, FS[0:2], PCISTOP33_L.

Table 6. Logic Input Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	–	GND-0.3	–	0.8	V
V_{IH}	Input High Voltage	–	2.0	–	VDD+0.3	V
I_{IL}, I_{IH}	Input Low/High Current	0 <Vin< V_{DD}, Input Leakage current	–	–	±50	µA

7.3.2 SDATA, SCLK Input/Output

The SMBus electrical characteristics are described in Table 7.

Table 7. SDATA and SCLK Input Electrical Characteristics *

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	–	GND-0.3	–	0.8	V
V_{IH}	Input High Voltage	–	2.0	–	VDD+0.3	V
I_{IL}, I_{IH}	Input Low/High Current	0 <Vin< VDD, Input Leakage current	–	–	±50	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.75mA	GND-0.3	–	0.4	V
I_{OL}	Output Low Current	V_O= 0.8V	2	–	50	mA
** **Note:** (5-V tolerant) If clock vendor only supports 3.3-V tolerant IO, they must provide an application note in their specification on how to handle a 5-V SMBus (i.e., clamp circuit on the motherboard).*						

7.3.3 X1, X2 Crystal Input/Feedback

The crystal input electrical characteristics are described in Table 8.

Table 8. Crystal Input/Feedback Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
Cinx	Crystal pin load capacitance	–	27	36	45	pF

7.3.4 PCI/ HyperTransport™ Clock Outputs

The following PCI and HyperTransport™ clock output electrical characteristics are described in Table 9.

The PCI and HyperTransport pins are PCI33[0:5], PCI_F , PCI33_HT66[0:2].

Table 9. PCI/HyperTransport™ Clock Output Electrical Characteristics (Lump Capacitance Test Load =30 pF)

	Parameter	Description	Test Conditions	PCI33, PCI33_HT66 = 33MHz			PCI33_HT66 = 66MHz			Unit
				Min	Typ	Max	Min	Typ	Max	
DC	V_{OL}	Output Low Voltage	I_{OL} = 9.0mA	–	–	0.4	–	–	0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -12mA	2.4	–	–	2.4	–	–	V
	I_{OL}	Output Low Current	V_O= 0.8V	10	–	–	10	–	–	mA
	I_{OH}	Output High Current	V_O= 2.0V	–15	–	–	–15	–	–	mA
	f	Frequency, Actual	–	–	33.33	–	–	66.667		MHz
AC	t_R	Output Rise Edge Rate	Measured from 20% to 60%	1	–	4	1	–	4	V/ns
	t_F	Output Fall Edge Rate	Measured from 60% to 20%	1	–	4	1	–	4	V/ns
	t_D	Duty Cycle	Measured on rising and falling edge at 1.5 V	45	–	55	45	–	55	%

Table 9. PCI/HyperTransport™ Clock Output Electrical Characteristics (Lump Capacitance Test Load =30 pF) (Continued)

	Parameter	Description	Test Conditions	PCI33, PCI33_HT66 = 33MHz			PCI33_HT66 = 66MHz			Unit
				Min	Typ	Max	Min	Typ	Max	
AC	t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	0	–	250	0	–	250	ps
	t_{JA}	Jitter, Accumulated	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 µs	-1000	–	1000	-1000	–	1000	ps
	t_{FS}	Frequency Stabilization from Power-up (cold start)	Measured from full supply voltage.	0	–	3	0	–	3	mS
	R_{ON}	Output Impedance	Average value during switching transition. Used for determining series termination value.	12	15	55	12	15	55	Ω

7.3.5 REF[2:0] Clock Outputs

The Reference clock output electrical characteristics are described in Table 10.

Table 10. Reference Clock Output Electrical Characteristics (Lump Capacitance Test Load = 20 pF)

	Parameter	Description	Test Conditions	Min	Typ	Max	Unit
DC	V_{OL}	Output Low Voltage	I_{OL} = 9mA	–	–	0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -12mA	2.4	–	–	V
	I_{OL}	Output Low Current	V_O= 0.8V	16	–	–	mA
	I_{OH}	Output High Current	V_O= 2.0V	–22	–	–	mA
AC	f	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
	t_R	Output Rise Edge Rate	Measured from 20% to 80%	0.5	–	2	V/ns
	t_F	Output Fall Edge Rate	Measured from 80% to 20%	0.5	–	2	V/ns
	t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45	–	55	%
	t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	0	500	1000	ps
	t_{JA}	Jitter, Accumulated	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 µs	–1000	–	1000	ps
	t_{FS}	Frequency Stabilization from Power-up (cold start)	Measured from full supply voltage.	0	–	3	ms
	R_{ON}	Output Impedance	Average value during switching transition. Used for determining series termination value.	20	24	60	Ω

7.3.6 USB, 24_48MHz Clock Outputs

The USB and 24_48MHz clock output electrical characteristics are described in Table 11.

Table 11. 24_48 MHz, USB Clock Output Electrical Characteristics (Lump Capacitance Test Load = 20 pF)

	Parameter	Description	Test Conditions	24_48MHz			USB, 24_48MHz			Unit
				Min	Typ	Max	Min	Typ	Max	
DC	V_{OL}	Output Low Voltage	I_{OL} = 9mA	–		0.4	–		0.4	V
DC	V_{OH}	Output High Voltage	I_{OH} = -12mA	2.4		–	2.4		–	V
DC	I_{OL}	Output Low Current	V_{OL}= 0.8V	16		–	16		–	mA
DC	I_{OH}	Output High Current	V_{OL}= 2.0V	-22		–	–22		–	mA
AC	f	Frequency, Actual	Determined by PLL divider ratio	24.004			48.008			MHz
AC	t_R	Output Rise Edge Rate	Measured from 20% to 80%	0.5		2	0.5		2	V/ns
AC	t_F	Output Fall Edge Rate	Measured from 80% to 20%	0.5		2	0.5		2	V/ns
AC	t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	45		55	%
AC	t_{JC}	Jitter, Cycle-to-Cycle for 24_48MHz clock	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	0	250	500	0	250	500	ps
AC	t_{JC}	Jitter, Cycle-to-Cycle for USB clock (required for USB2.0)	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.				0		200	ps

Table 11. 24_48MHz, USB Clock Output Electrical Characteristics (Lump Capacitance Test Load = 20 pF) (Continued)

	Parameter	Description	Test Conditions	24_48 MHz			USB, 24_48 MHz			Unit
				Min	Typ	Max	Min	Typ	Max	
AC	t_{JA}	Jitter, Accumulated	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 µs	–1000		1000	–1000		1000	ps
	t_{FS}	Frequency Stabilization from Power-up (cold start)	Measured from full supply voltage	0		3	0		3	Ms
	R_{ON}	Output Impedance	Average value during switching transition. Used for determining series termination value.	20	24	60	20	24	60	Ω

7.3.7 CPUT[1:0], CPUC[1:0] Clock Outputs

The processor clock output electrical characteristics are described in Table 12.

Table 12. Processor Clock Output Electrical Characteristics

	Parameter	Description	Test Conditions	Min	Typ	Max	Unit
AC	t_R	Rise Edge Rate	Measured at the AMD64 processors test load. 0V± 400mV (differential measurement)	2	–	10	V/ns
	t_F	Fall Edge Rate	Measured at the AMD64 processors test load 0V ± 400mV (differential measurement)	2	–	10	V/ns
AC	V_{DIFF}	Differential Voltage (Single ended)	Measured at the AMD64 processors test load (single-ended measurement)	0.40	1.25	2.3	V
	ΔV_{DIFF}	Change in V_{DIFF_DC} Magnitude	Measured at the AMD64 processors test load (single-ended measurement)	–150	–	+150	mV
	V_{CM}	Common Mode Voltage (Note 1)	Measured at the AMD64 processors test load (single-ended measurement)	1.05	1.25	1.45	V
	ΔV_{CM}	Change in Common Mode Voltage	Measured at the AMD64 processors test load (single-ended measurement)	–200	–	+200	mV
	t_D	Duty Cycle	Measured at the differential crossing point	45	50	53	%
	t_{JC}	Jitter, Cycle-to-Cycle	Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.	0	100	200	ps

Table 12. Processor Clock Output Electrical Characteristics (Continued)

	Parameter	Description	Test Conditions	Min	Typ	Max	Unit
AC	t_{JA}	Jitter, Accumulated	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50psec, Sample Duration = 10usec	–1000		1000	ps
	t_{FS}	Frequency Stabilization from Power-up (cold start)	Measured from full supply voltage	0		3	mS
	R_{ON}	Output Impedance	Average value during switching transition. Used for determining series termination value. Note that current mode drivers may have a higher output impedance.	15	35	55	Ω

Figure 4 shows the single-ended measurement definitions referenced in Table 12.

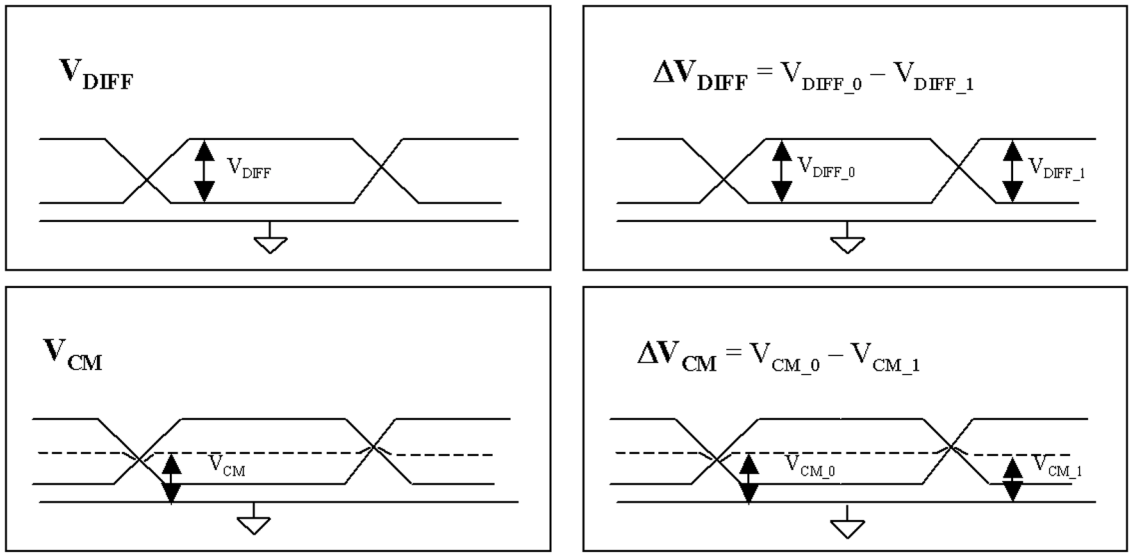

Figure 4. Single-Ended Measurement Definitions

7.3.8 Differential Processor Clock Motherboard Termination Scheme

The processor clock motherboard termination scheme is comprised of 15 ohm series resistor terminations located within 0.5” of clock generator, ~5” 100 ohm differential transmission line, AC coupling caps and 169 ohm differential termination located <0.5” from the processor CPUCLK pins.

The 100 ohm differential transmission lines are generated on the PCB using the stack-up and trace spacing shown in Figure 5. The closest-neighboring signal must be at least 20 mils from the CPUCLK differential pair to reduce motherboard crosstalk effects. The differential pair should be routed with 25 mil length matching between the true and compliment signals. For best signal integrity, these traces should be routed referenced to ground without crossing any plane splits.

A standard 4-layer motherboard stack-up is shown in Figure 5**.**

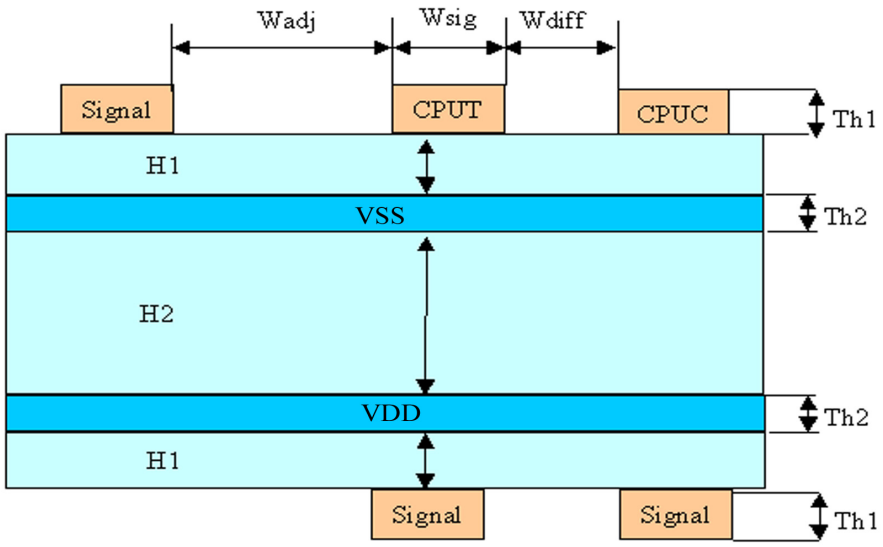

Figure 5. Four-Layer Motherboard Stack-Up and Impedance

The PCB stack-up parameters are outlined in Table 13.

Table 13. Board Stack-Up Parameters

Distance	Size
H1	Dielectric Thickness = 4.7 mils, Dk = Dielectric constant =4.3 for FR-4 board material
H2	Middle Substrate layer ~ 50 mils
Th1	Signal Thickness = 0.5 oz copper (plated) ~2 mils
Th2	Power/Ground Plane Thickness = 1 oz copper (un-plated) ~ 1.4 mils
Wsig	Signal trace width = 5 mils
Wdiff	Spacing to differential Clk = 5 mils
Wadj	Adjacent signal trace spacing = 20 mils

Figure 6 shows the motherboard processor clock termination scheme.

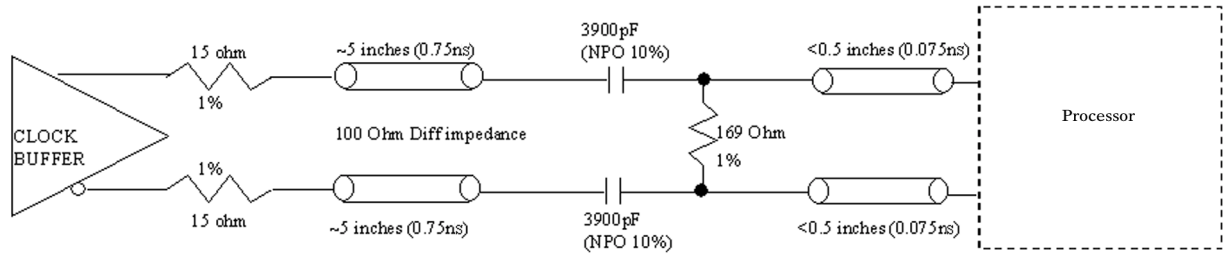

Figure 6. Motherboard Processor Clock Termination Scheme

7.3.9 Differential Processor Clock Input

The processor clock specifications assume the AMD64 processors contains a DC Bias generator circuit to center the receiver inputs after the ac-coupling caps (3900 pF) to VDD/2 where VDD = 2.5 V ± 5%.

Figure 7 on page 36 shows target processor internal bias generation.

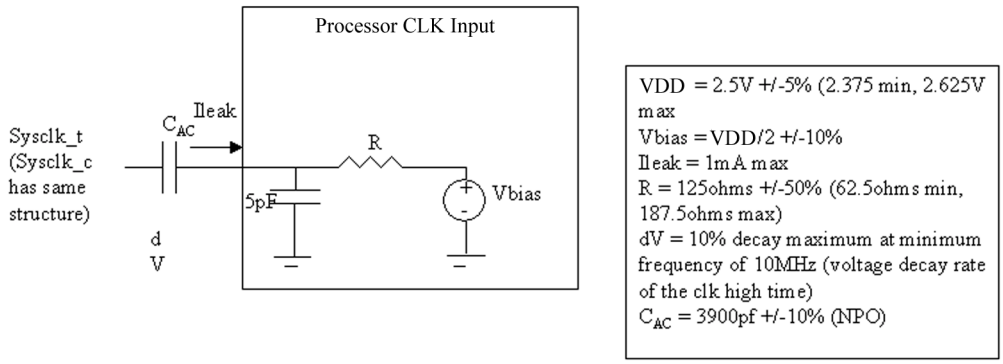

Figure 7. Target Processor Internal Bias Generation

7.3.10 Differential Processor Clock for AMD64 Processors Test Load

The processor clock specification assumes the following test load:

- Fifteen ohm series resistor terminations (used to match the driver impedance with the board impedance) located close to the clk generator
- Five inches of 100-ohm differential transmission line
- AC coupling caps (3900 pF) and 169 ohm differential termination located <0.5” from the processor CPUclk pins
- Trace delay of 180 ps between the AC coupling caps and the processor bias generator—This is to simulate the processor package trace propagation delay. Package trace impedance is 38 ohms single ended and 75 ohms differential.

***Note**: Equivalent package trace on FR-4 PCB is 12 mil trace/30mil space/12mil trace using stackup as shown in Figure 6 on page 35.*

- DC-bias generator circuit referenced to 2.5 V
- Five pF load cap

Figure 8 on page 37 shows the differential processor clock test load for the AMD64 processors.

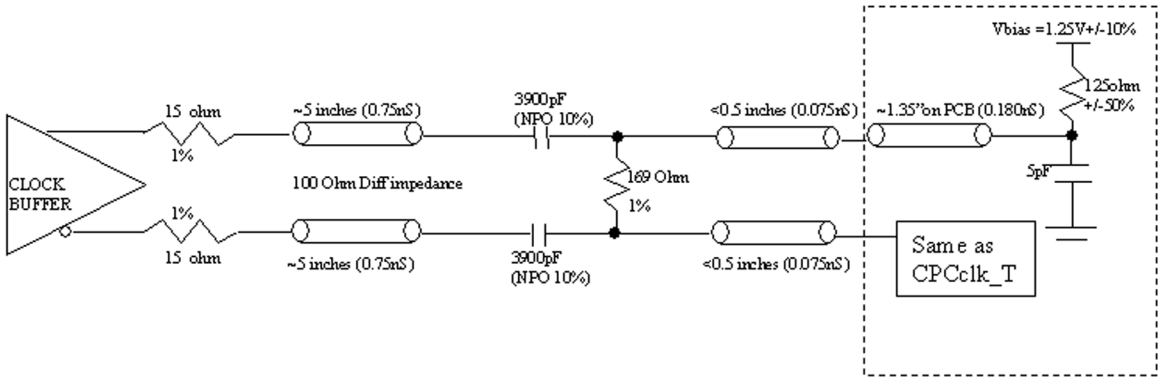

Figure 8. Differential Processor Clock for AMD64 Processors Test Load

7.4 Spread Spectrum

The spread spectrum characteristics are outlined in Table 14.

Table 14. Spread Spectrum Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
f_{SPREAD}	Spread spectrum at 33 kHz sweep rate[1]	–	0.0		–0.5	%

Note:

1. 33-KHz triangular modulation is required along with other spread amounts and modulation algorithms, such as a maximum of 50 kHz Δf/Δt modulation, are left up to the clock generator vendor to include as differentiating features.

7.5 Skew

Skew for AMD64 processor-based systems must be specified in two ways.

Time Independent Skew: The allowable skew between clock outputs that does not vary over time (not dependent upon voltage or temperature changes or co-related with other outputs due to voltage and temperature changes).

Time Variant Skew: The allowable skew between clock outputs that vary over time (with changes in voltage and temperature and that does not effect processor, HT66, or PCI33 outputs equally). The requirement for the time variant specification is derived directly from the HyperTransport technology consortium source point.

Table 15 shows the skew characteristics for the AMD64 processor-based systems.

Table 15. Skew Characteristics

	Parameter	Description	Test Conditions	Skew [5] Window	Unit
Time Independent	$T_{SK\_CPU\_CPU}$	Processor to processor skew, time independent	Measured at crossing points for CPUT rising edges.[1]	250	ps
	$T_{SK\_CPU\_PCI33}$	Processor to PCI skew, time independent	Measured at crossing point for CPUT rising edge and 1.5V for PCI clocks	500 (2000)[3]	ps
	$T_{SK\_PCI33\_PCI33}$	PCI33 to PCI33 clock skew, time independent	Measured between rising at 1.5V	500	ps
	$T_{SK\_PCI33\_HT66}$	PCI33 to HT66 clock skew, time independent	Measured between rising at 1.5V	500	ps
	$T_{SK\_CPU\_HT66}$	Processor to HT66 clock skew, time independent	Measured at crossing point for CPUT rising edge and 1.5 V for HyperTransport™ clocks	500 (2000)[3]	ps
	$T_{SK\_HT66\_HT66}$	HT66 to HT66 clock skew, time independent	Measured between rising edge at 1.5V	500	ps

Notes:

1. *All skews in this skew budget are measured from the first referenced signal to the next (i.e., Tsk_CPU_PCI33 is the skew from the processor crossing point to any PCI33 rising edge @ 1.5V). Therefore, this skew specifies the maximum* skew window *between these two signals to be 500 ps whether the processor crossing leads or lags the PCI clock. This should* not *be interpreted to mean that the PCI33 edge could either be 500 ps before the processor clock to 500 ps after the clock, thus defining a 1000 ps window in which the PCI33 clock edge could fall.*

2. *Time variant and time invariant skews will add in real systems such that the worst-case skew allowable is the sum of the two. All skew measurements should be taken at output pins of the clock generator with SSC on.*

3. *If the Clock Vendor is only interested in supporting AMD64 processor-based systems (i.e., the clock generator will* not *be used in K7 systems), the $T_{SK\ CPU\text{-}PCI33}$ and $T_{SK\ CPU\text{-}HT66}$* Time Independent *skews (as measured under nominal temperature and voltage) can be increased from 500 ps to 2000 ps. This does NOT mean the total combined skew over temp/voltage is equal to 2000 ps + 500 ps=2500 ps. The* Time Variant *skew of the clock generator must still remain <200 ps. The* Time Variant *skew allows for skew changes induced by temperature and/or voltage variations.*

4. *The* Time *Variant specifications are derived from the HyperTransport Electrical Specification. The Tclk2Rclkssc parameter can be ignored when the skew measurements are taken at the output of the clock generator.*

5. *AMD recommends using an averaging function on the oscilloscope while taking skew measurements. This technique has been shown to be effective in reducing jitter accumulation within the skew measurements.*

Table 15. Skew Characteristics (Continued)

	Parameter	Description	Test Conditions	Skew [5] Window	Unit
Time Variant[4]	$T_{SK\_CPU\_CPU}$	Processor to processor skew, time variant	Measured at crossing points for CPUT rising edges.[1]	200[2]	ps
	$T_{SK\_CPU\_PCI33}$	Processor to PCI skew, time variant	Measured at crossing point for CPUT rising edge and 1.5 V for PCI clocks	200[2]	ps
	$T_{SK\_PCI33\_PCI33}$	PCI33 to PCI33 clock skew, time variant	Measured between rising at 1.5 V	200[2]	ps
	$T_{SK\_PCI33\_HT66}$	PCI33 to HT66 clock skew, time variant	Measured between rising at 1.5 V	200[2]	ps
	$T_{SK\_CPU\_HT66}$	Processor to HT66 clock skew, time variant	Measured at crossing point for CPUT rising edge and 1.5 V for HyperTransport™ clocks	200[2]	ps
	$T_{SK\_HT66\_HT66}$	HT66 to HT66 clock skew, time variant	Measured between rising edge at 1.5 V	200[2]	ps

Notes:

1. *All skews in this skew budget are measured from the first referenced signal to the next (i.e., Tsk_CPU_PCI33 is the skew from the processor crossing point to any PCI33 rising edge @ 1.5V). Therefore, this skew specifies the maximum* skew window *between these two signals to be 500 ps whether the processor crossing leads or lags the PCI clock. This should* not *be interpreted to mean that the PCI33 edge could either be 500 ps before the processor clock to 500 ps after the clock, thus defining a 1000 ps window in which the PCI33 clock edge could fall.*
2. *Time variant and time invariant skews will add in real systems such that the worst-case skew allowable is the sum of the two. All skew measurements should be taken at output pins of the clock generator with SSC on.*
3. *If the Clock Vendor is only interested in supporting AMD64 processor-based systems (i.e., the clock generator will* not *be used in K7 systems), the $T_{SK\ CPU\text{-}PCI33}$ and $T_{SK\ CPU\text{-}HT66}$* Time Independent *skews (as measured under nominal temperature and voltage) can be increased from 500 ps to 2000 ps. This does NOT mean the total combined skew over temp/voltage is equal to 2000 ps + 500 ps=2500 ps. The* Time Variant *skew of the clock generator must still remain <200 ps. The* Time Variant *skew allows for skew changes induced by temperature and/or voltage variations.*
4. *The* Time *Variant specifications are derived from the HyperTransport Electrical Specification. The Tclk2Rclkssc parameter can be ignored when the skew measurements are taken at the output of the clock generator.*
5. *AMD recommends using an averaging function on the oscilloscope while taking skew measurements. This technique has been shown to be effective in reducing jitter accumulation within the skew measurements.*

Chapter 8 SMBus Interface

The clock generator features an SMBus 1.0 connection that is designed for use in configuring internal register settings that control particular device functions and read back the current state of the control registers. Upon power-up, the clock generator initializes with default settings/board strappings, therefore the use of the software programming is optional. In order to override the initial settings, Byte0 bit0 must first be activated to allow for software settings. Once this bit is set, the other registers can be programmed accordingly. Once a feature is changed, the value programmed through the SMBus interface will override the initial hardware setting except where noted. To return to the hardware strapped mode of operation, the software reads the strapped pin states in Byte 4 and reprograms the device accordingly. Various clock generator manufacturers may provide additional features as they see fit as long as this basic set of features are included.

8.1 SMBus Protocol

Simplifications to the SMBus 1.1 protocol specification have been made to define a minimum supported feature set. The feature set is defined in this chapter.

8.1.1 Block Write

The byte/count/byte must be evaluated and compared to the number of received bytes to validate a block write transfer. A miscompare must leave the register values unchanged. Other methods of error notification are left to the vendor but none are expressly required.

***Note**: The block write compare is only required for server applications.*

8.1.2 Block Read

The byte count byte is evaluated by the host controller and errors generated if the compare does not match the transferred number of bytes. This error can result from

- Direct comparison of the byte count to transferred bytes
- The protocol error detected from the lack of a NACK condition in the case of an overrun
- The protocol error detected from the presence of a NACK condition when an ACK is expected in the case of an under run

While the SMBus protocol requires host ACK bits to be sent to acknowledge each transferred bytes, an implementation that ignores these ACK bits as a simplification is acceptable.

Clock generators that implement a simplified block read command, wherein the block read command is not required and the R/W bit associated with the device address initiates a block read are allowed in addition to but not as a substitution for the full SMbus block read protocol.

Table 16 shows the I^2C addresses.

Table 16. I^2C Address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	-

Table 17 shows the register settings for frequency and spread spectrum control.

The Write enable and disable bits only take affect once the current block write has completed.

Table 17. Byte0: Frequency and Spread Spectrum Control Register

Bit	Default	Description
7	Inactive=0	Write Disable (write once). A 1 written to this bit, after a 1 has been written to Byte 0 bit 0, will permanently disable modification of all configuration registers until the part has been powered off. Once the clock generator has been Write disabled, the SMBus controller should still accept and acknowledge subsequent write cycles but it should not modify any of the registers.
6	Inactive=0	Spread Spectrum enable (0=disable, 1=enable). This bit provides a software programmable control for spread spectrum clocking. The truth table for SSC is as follows: SPREAD pin, SSE bit, Enabled/Disabled 0, 0, Disabled 0, 1, Enabled 1, 0, Enabled 1, 1, Enabled The readback version of this bit is the hardware strapped value such that the software has the ability to know each state (either by readback or by writing the SSE bit).
5	Inactive=0	FS4 (reserved for mapping to larger FS table through programmable FS bit only)
4	Inactive=0	FS3 (reserved for mapping to larger FS table through programmable FS bit only)
***Note**: FS[2:0] are the only required FS inputs and represent the only required operating states of the device. FS[4:3] are defined and reserved so that implementations that provide a larger FS table with additional operating states are enabled. None of these additional operating states are required by the baseline feature set of the platforms that we envision, however, may serve customer requirements or desires. When Byte 0 is read, the current state of the register should be returned, not FS[2:0] or SPREAD pin states. These pin states are provided in Byte4.*		

Table 17. Byte0: Frequency and Spread Spectrum Control Register (Continued)

Bit	Default	Description
3	Inactive=0	FS2 (corresponds to Table 2, on page 11)
2	Inactive=0	FS1 (corresponds to Table 2, on page 11)
1	Inactive=0	FS0 (corresponds to Table 2, on page 11)
0	Inactive=0	Write Enable. A 1 written to this bit after power up will enable modification of all configuration registers and subsequent zeros written to this bit will disable modification of all configurations except this single bit. Note that when a 1 has been written to Byte0 bit 7 all modification is permanently disabled until the device power cycles. Note also that block write transactions to the interface will complete, however unless the interface has been previously unlocked, the writes will have no effect. The effect of writing this bit does not take effect until the subsequent block write command.
***Note**: FS[2:0] are the only required FS inputs and represent the only required operating states of the device. FS[4:3] are defined and reserved so that implementations that provide a larger FS table with additional operating states are enabled. None of these additional operating states are required by the baseline feature set of the platforms that we envision, however, may serve customer requirements or desires. When Byte 0 is read, the current state of the register should be returned, not FS[2:0] or SPREAD pin states. These pin states are provided in Byte4.*		

The process of changing the FS bits thru software is as follows:

1. Upon powerup, Byte0, bits[5:1], and FS[4:0] are set to the default hardware settings.
2. A 1 is written to Byte0, bit0 to enable software control.
3. Every time Byte0 is written, the FIDs are affected.
4. If a 0 is written to Byte0, bit0 the software control is disabled. Disabling software control does not cause the contents of Byte0 to default back to hardware setting for FS[4:0].

Table 18 outlines the register settings for the PCI clock control.

Table 18. Byte1: PCI Clock Control Register (1=Enabled, 0=Disabled)

Bit	Default	Description
7	Active=1	PCI33_HT66(1) enable (1=Enabled, 0=Disabled)
6	Active=1	PCI33_HT66(0) enable (1=Enabled, 0=Disabled)
5	Active=1	PCI33(5) enable (1=Enabled, 0=Disabled)
4	Active=1	PCI33(4) enable (1=Enabled, 0=Disabled)
3	Active=1	PCI33(3) enable (1=Enabled, 0=Disabled)
2	Active=1	PCI33(2) enable (1=Enabled, 0=Disabled)
1	Active=1	PCI33(1) enable (1=Enabled, 0=Disabled)
0	Active=1	PCI33(0) enable (1=Enabled, 0=Disabled)
***Note**: If a clock is set to free-running in Byte3and Byte 4, it can still be shut off using Byte1 or Byte2.*		

Table 19 outlines the clock register settings available through SMBus.

Table 19. Byte2: PCI Clock, USB, 24_48MHz, REF[2:0] Control Register (1=Enabled, 0=Disabled)

Bit	Default	Description
7	Active=1	CPUT/C(1) shutdown. This bit can be used to disable the CPUT/C(1) clock pair. During shutdown, CPUT = L and CPUC = H.
6	Active=1	CPUT/C(0) shutdown. This bit can be used to disable the CPUT/C(0) clock pair. During shutdown, CPUT = L and CPUC = H.
5	Active=1	REF(2) enable (1=Enabled, 0=Disabled)
4	Active=1	REF(1) enable (1=Enabled, 0=Disabled)
3	Active=1	REF(0) enable (1=Enabled, 0=Disabled)
2	Active=1	24_48MHz enable (1=Enabled, 0=Disabled)
1	Active=1	USB enable (1=Enabled, 0=Disabled)
0	Active=1	PCI33_HT66(2) enable (1=Enabled, 0=Disabled)

The individual clock output enable/disable controls shown in Table 19 are intended to allow unused clock outputs to be disabled to reduce electrical interference and electromagnetic radiation. They are not intended to provide any dynamic control or power reduction features. Also, if a clock is set to free running, it can still be shut off using Byte1 or Byte2.

Table 20 outlines the register control for PCI free running clocks.

Note: *1=Free running, 0=Controlled by PCISTOP.*

Table 20. Byte3: PCI Clock Free Running Select Control Register

Bit	Default	Description
7	Inactive=0	Reserved for vendor specific functions
6	Inactive=0	Reserved for vendor specific functions
5	Inactive=0	PCI(5) free-running enable *
4	Inactive=0	PCI(4) free-running enable *
3	Inactive=0	PCI(3) free-running enable *
2	Inactive=0	PCI(2) free-running enable *
1	Inactive=0	PCI(1) free-running enable *
0	Inactive=0	PCI(0) free-running enable *
NOTE: ** The individual free-running enable/disable controls are intended to allow individual clock outputs to be made free running. A clock output that has its free-running bit enabled will not be turned off with the assertion of either PCISTOP33_L or PCISTOP66_L.*		

Table 21 outlines some additional register settings for the clock control through SMBus.

Table 21. Byte4: Pin Latched/Real Time State (and One Free Running Control)

Bit	Default	Description
7	Active=1	PCI33_F output enable. This bit can be optionally used to disable the PCI33_F output.
6	Active=1	SPREAD pin state
5	Active=1	24_48SEL_L pin power up latched state
4	Active=1	PCI33_HT66SEL_L pin state
3	Active=1	FS(2) power-up latched pin state
2	Active=1	FS(1) power-up latched pin state
1	Active=1	FS(0) power-up latched pin state
0	InActive=0	Reserved for vendor specific functions

Bits one through six of this register are intended to provide the original latch input pin state or the current real time input pin state to software. These values can be used to return the clock generator to its hardware configured operating state.

Table 22 outlines the register settings for clock vendor ID.

Table 22. Byte5: Clock Vendor ID

Bit	Default	Description
7	Varies	Vendor ID, 001= reserved, 111=reserved
6		Vendor ID
5		Vendor ID
4		Device Revision ID
3		Device Revision ID
2		Device Revision ID
1		Device Revision ID
0		Device Revision ID

The 3-bit Vendor ID and 5-bit Device revision ID are intended to provide software with enough information about the clock generator present in the system as to decide the correct configuration. Vendor ID is assigned by AMD. The Device Revision ID is left to the clock generator vendor to assign. The combination of the two provides a unique ID for software.

Table 23. Byte6: Reserved for Byte Count

Bit	Default	Description
7		Reserved for device specific read byte count=MSB
6		Reserved
5		Reserved
4		Reserved
3		Reserved
2		Reserved
1		Reserved
0		Reserved

This register contains the number of bytes that the clock generator returns when issued a block read command. It is defined and reserved such that additional bytes can be added as the clock generator vendor sees fit. This register should contain the total number of bytes returned by a block read command including vendor specific bytes above 6. Should a clock vendor wish to provide test/debug mode registers above byte 6, this value can remain defaulted to 6 and later updated through an SMBus write to allow access to these test/debug registers.

ATPG Function—This feature is only used during processor burn-in and is an optional feature for the clock vendor to implement.

Two SMBus register bits are required to implement this feature:

- **ATPG Mode Bit**—Enables/Disables ATPG mode
- **ATPG Pulse Bit—Triggers a single CPUclk pulse when set**

Assuming that the clock synthesizer is operating either in Normal mode or PLL bypass mode, the following sequence can be followed to generate an ATPG pulse.

- Set the Write Enable Bit (Byte/Bit 0) to program the Clock Synthesizer registers using the SM Bus.
- Use the ATPG Mode Bit in the clock synthesizer configuration space to enable/disable the ATPG mode. When this bit is set, the ATPG mode is enabled and the differential processor clock outputs are pulled in differential low state (CPUT = 0 and CPUC = 1). The ATPG mode also requires the USBclk (48MHz) to run as usual. All other clocks (PCI, Ref, PCI33_66, SuperIO are not used by the ATPG mode therefore can either be left running or shut off.
- Use the ATPG pulse bit in the clock synthesizer program space to generate the ATPG pulse. When the ATPG pulse bit is set, a differential ATPG pulse is generated on the differential processor clock pins. The pulse width of the ATPG pulse is one processor clock period. The processor clock period in the ATPG mode is same as the one in Normal mode or PLL bypass mode.

- Clear the ATPG pulse bit, since the clock synthesizer only recognizes 0 to 1 transition of the ATPG pulse bit for next ATPG pulse generation.
- Use the ATPG pulse bit to generate the next ATPG pulse (set to 1).
- If the ATPG pulse bit is not set and the ATPG mode bit is cleared, then the synthesizer should work in normal or PLL bypass mode.