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100790

9–Bit Transceiver

FEATURES

- **Typical propagation delay from input to output: 1.3ns**
- **Typical supply current ($-I_{EE}$): 240mA**
- **3–state outputs eliminate bus impedance discontinuities and wire–OR problems**
- **9–bit data width provides optimum handling of parity bit**
- **Drives 25Ω loads**
- **4,000 Volt ESD protection for all pins**
- **Controlled edge rates for quieter bus operation**

DESCRIPTION

The 100790 is a nine–bit, noninverting transceiver. All data lines (A_n and B_n) are bidirectional with three–state capability. The Direction Control, DIR, selects the data flow path (A_n to B_n or B_n to A_n). The Output Enable, $\overline{OE}$, determines whether the data lines are active or in a high impedance state. A High on $\overline{OE}$ will turn off the output emitter follower of every data line. As a result, each data line approaches the termination voltage (–2.0V) and takes on a high impedance state.

Each data line can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V). Integrated pull–down resistors are provided for all data lines.

All unused inputs can be left open due to integrated pull–down resistors.

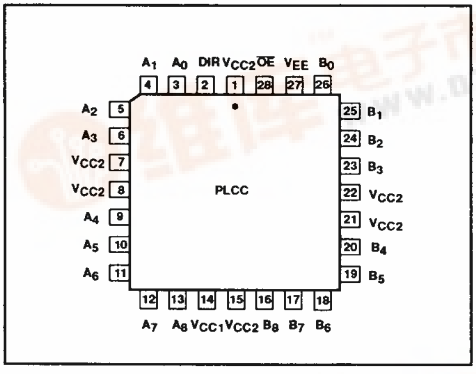
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28–Pin PLCC	100790A

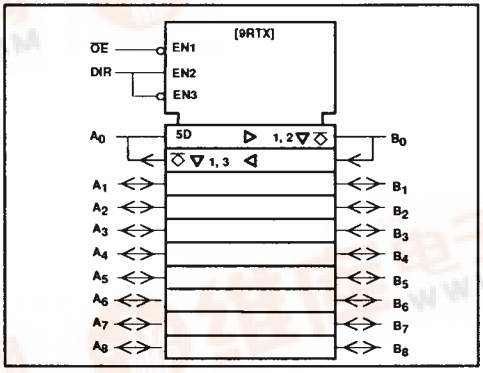
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_8$	A bidirectional data lines
$B_0 - B_8$	B bidirectional data lines
$\overline{OE}$	Output enable input
DIR	Direction control input

PIN CONFIGURATION

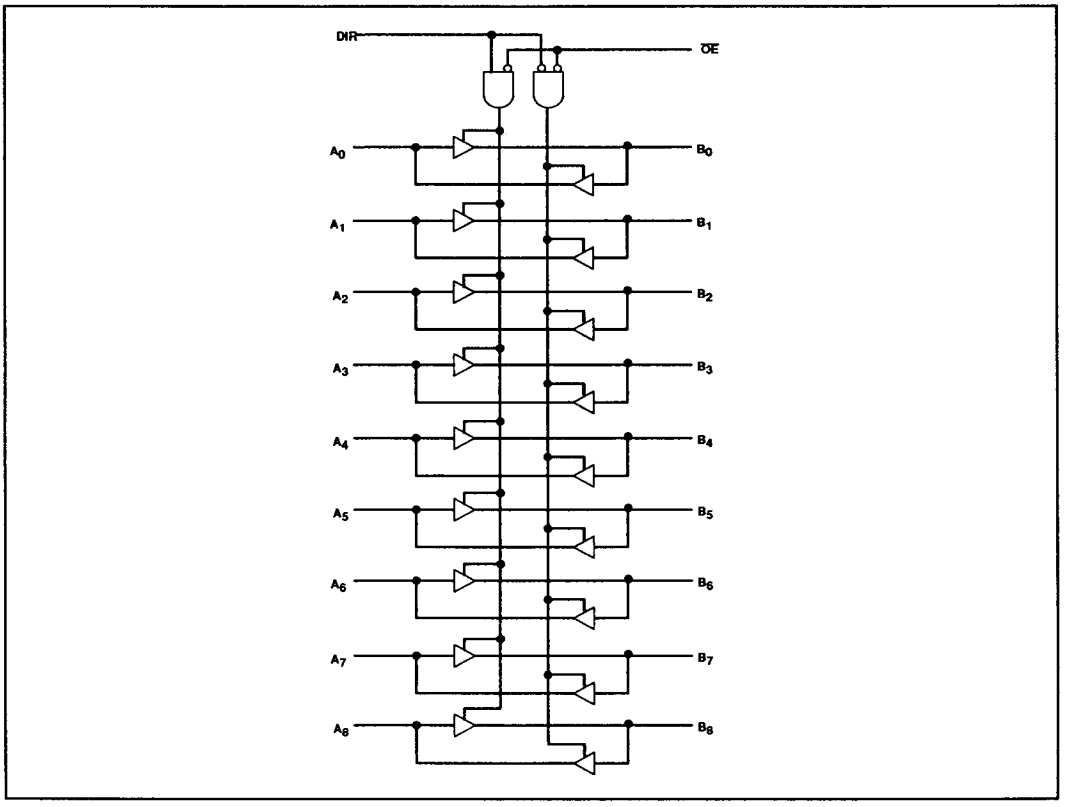


IEC/IEEE SYMBOL



Transceiver 100790

LOGIC DIAGRAM



FUNCTION TABLE

CONTROL		DATA		OPERATING MODE
$\overline{OE}$	DIR	A_n	B_n	
L	L	L	L	Data flows from B_n to A_n
L	L	H	H	
L	H	L	L	Data flows from A_n to B_n
L	H	H	H	
H	X	Z	Z	All A_n and B_n in high impedance state

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance state

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+70°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–100	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+70	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

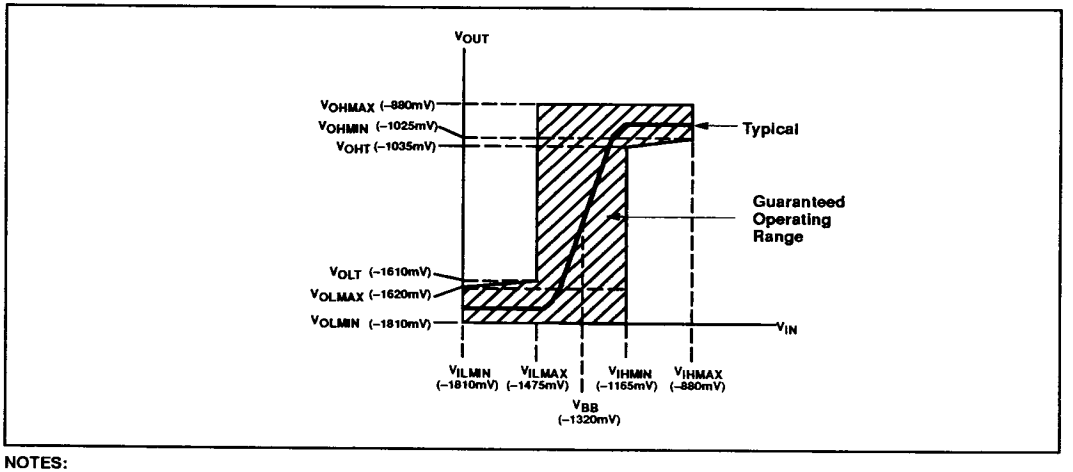
$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +70°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 25Ω to –2.0V ± 0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{OZ}	Off–state output current[5]		$\overline{OE}$ at V_{IHMAX}. Apply –2.1V to output under test. Apply V_{IHMAX} to the corresponding input.					120	µA
I_{IH}	High level input current[5]	A_n, B_n	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}. $\overline{OE}$ at V_{IHMAX}.					100	µA
		$\overline{OE}$, DIR	One control line under test at V_{IHMAX}, other control line at V_{ILMIN}. All A_n and B_n open.					100	µA
I_{IL}	Low level input current[5]	A_n, B_n	One input under test at V_{ILMIN}, other inputs at V_{IHMAX}. $\overline{OE}$ at V_{IHMAX}.			10			µA
		$\overline{OE}$, DIR	One control line under test at V_{ILMIN}, other control line at V_{IHMAX}. All A_n and B_n open.			10			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			100	240	280	mA

NOTES:

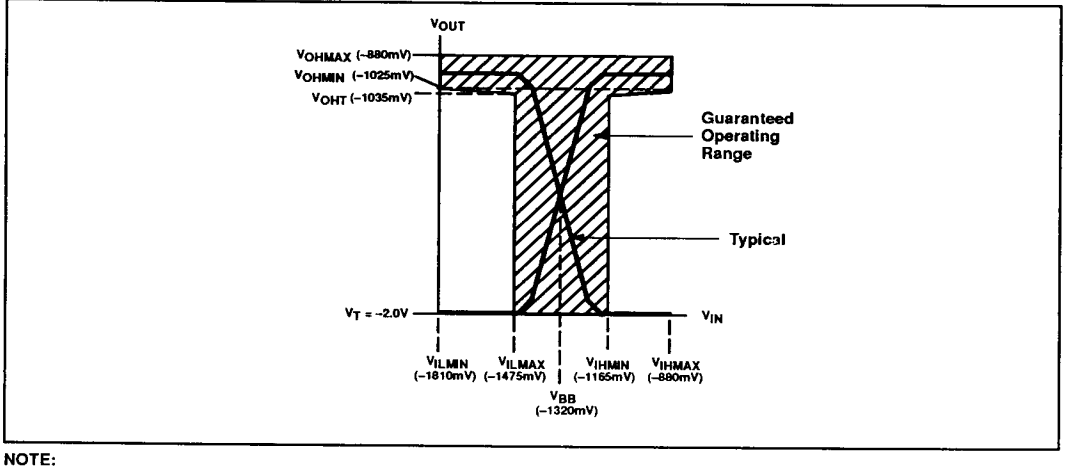
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapter 10, Section 4.
5. For bidirectional lines, this parameter includes currents due to output leakage and input pull–down resistors.

TRANSFER CHARACTERISTIC FOR DATA FLOW



NOTES:
1. If V_{IN} is applied to A_n, then V_{OUT} is measured at B_n.
2. If V_{IN} is applied to B_n, then V_{OUT} is measured at A_n.

TRANSFER CHARACTERISTIC FOR ENABLING AND DISABLING THE OUTPUTS



NOTE:
V_{IN} is applied to DIR or $\overline{OE}$; V_{OUT} is measured at A_n or B_n.

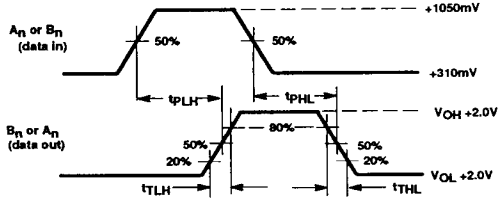
AC ELECTRICAL CHARACTERISTICS

PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.7V$ to $-4.2V$

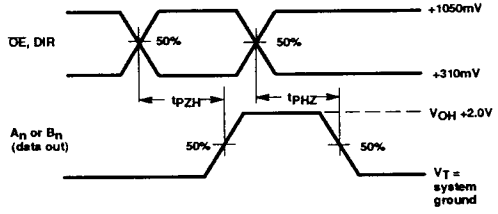
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +70°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 1	0.5	2.0	0.5	2.0	0.5	2.0	ns
t_{PZH}	Output enable time DIR, $\overline{OE}$ to A_n, B_n	Waveform 2	2.0	4.0	2.0	4.0	2.0	4.0	ns
t_{PHZ}	Output disable time DIR, $\overline{OE}$ to A_n, B_n	Waveform 2	0.7	2.2	0.7	2.2	0.7	2.2	ns
t_{TLH} t_{THL}	Transition time for A_n, B_n	Waveform 1	0.4	1.85	0.4	1.85	0.4	1.85	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



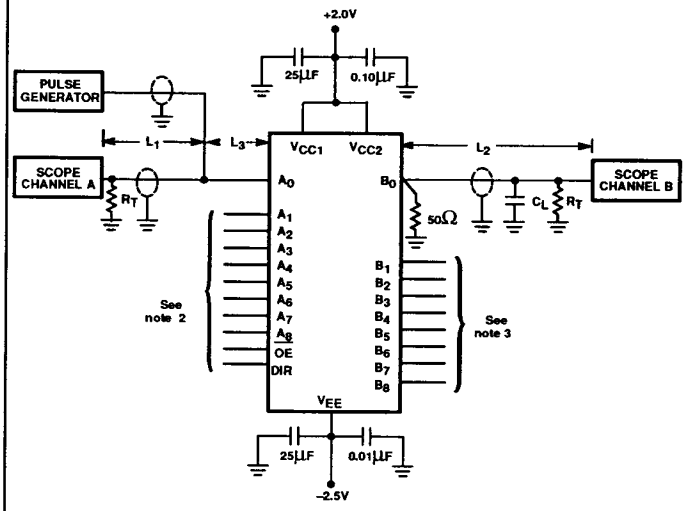
Waveform 1. Propagation Delays and Transition Times



Waveform 2. Output Enable and Disable Time

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

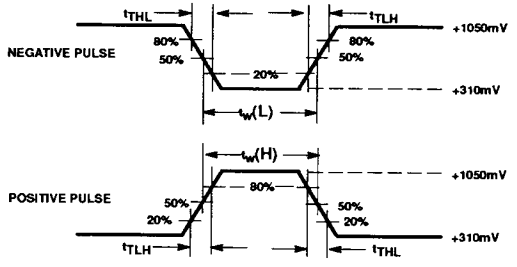
AC TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$,
$V_{EE} = -2.8V$ to $-2.2V$, $V_T = 0V$ (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	740mV$_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.