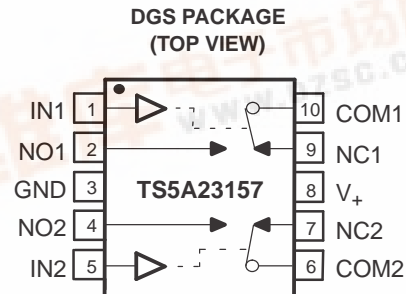


FEATURES

- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Specified Break-Before-Make Switching
- Low ON-State Resistance (15 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.8-V to 5.5-V Single-Supply Operation

APPLICATIONS

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits



DESCRIPTION

The TS5A23157 is a dual, single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

ORDERING INFORMATION

T _A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	VSSOP (MSOP-10) – DGS	Tape and reel	TS5A23157TDGSRQ1	JBR

FUNCTION TABLE

INPUT IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

SUMMARY OF CHARACTERISTICS

Configuration	2:1 Multiplexer/ Demultiplexer (2 × SPDT)
Number of channels	2
r _{on}	15 Ω
Δr _{on}	0.15 Ω
r _{on(flat)}	4 Ω
t _{ON} /t _{OFF}	8.7 ns/6.8 ns
t _{BBM}	0.5 ns
Charge injection	7 pC
Bandwidth	220 MHz
OFF isolation	–65 dB at 10 MHz
Crosstalk	–66 dB at 10 MHz
Total harmonic distortion	0.01%
I _{COM(off)} /I _{NC(off)}	±1 μA
Package option	10-pin DGS



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TS5A23157-Q1

DUAL 15- Ω SPDT ANALOG SWITCH

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V ₊	Supply voltage range ⁽²⁾		-0.5	6.5	V
V _{NC} V _{NO} V _{COM}	Analog voltage range ⁽²⁾⁽³⁾⁽⁴⁾		-0.5	V ₊ + 0.5	V
I _{I/O}	Analog port diode current	V _{NC} , V _{NO} , V _{COM} < 0 or V _{NC} , V _{NO} , V _{COM} > V ₊		±50	mA
I _{NC} I _{NO} I _{COM}	On-state switch current	V _{NC} , V _{NO} , V _{COM} = 0 to V ₊		±50	mA
V _{IN}	Digital input voltage range ⁽²⁾⁽³⁾		-0.5	6.5	V
I _{IK}	Digital input clamp current	V _{IN} < 0		-50	mA
	Continuous current through V ₊ or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽⁵⁾			165.36	°C/W
T _{stg}	Storage temperature range		-65	150	°C
ESD	Electrostatic discharge rating	Human-body model		2	kV
		Charged-device model		1	kV
		Machine model		200	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 5.5 V maximum.

(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NO} , V _{NC}					0		V ₊	V
ON-state resistance	r _{on}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −30 mA,	Switch ON, See Figure 6	Full	4.5 V			15	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 3.15 V, I _{COM} = −30 mA,	Switch ON, See Figure 6	25°C	4.5 V	0.15			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −30 mA,	Switch ON, See Figure 6	25°C	4.5 V	4			Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = 0 to V ₊ ,	Switch OFF, See Figure 7	25°C	5.5 V	−1	0.05	1	μA
				Full		−1	1		
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0 to V ₊ , V _{COM} = Open,	Switch ON, See Figure 7	25°C	5.5 V	−0.1		0.1	μA
				Full		−1	1		
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0 to V ₊ ,	Switch ON, See Figure 7	25°C	5.5 V	−0.1		0.1	μA
				Full		−1	1		
Digital Inputs (IN1, IN2) ⁽²⁾									
Input logic high	V _{IH}			Full		V ₊ × 0.7			V
Input logic low	V _{IL}			Full		V ₊ × 0.3			V
Input leakage current	I _{IH} , I _{IL}	V _{IN} = 5.5 V or 0		25°C	5.5 V	−1	0.05	1	μA
				Full		−1	1		

(1) $T_A = 25^\circ\text{C}$

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TS5A23157-Q1

DUAL 15-Ω SPDT ANALOG SWITCH

SCS232-T05/2003 查询"TS5A23157-Q1"供应商

Electrical Characteristics for 5-V Supply (continued)

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	4.5 V to 5.5 V	1.2		8.7	ns
Turn-off time	t _{OFF}	V _{NC} = GND and V _{NO} = V ₊ , or V _{NC} = V ₊ and V _{NO} = GND,	R _L = 500 Ω, C _L = 50 pF, See Figure 9	Full	4.5 V to 5.5 V	0.5		6.8	ns
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 10	25°C	4.5 V to 5.5 V	0.5			ns
Charge injection	Q _C	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	See Figure 14	25°C	5 V		7		pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND,	Switch OFF, See Figure 8	25°C	5 V		5.5		pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND,	Switch ON, See Figure 8	25°C	5 V		17.5		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND,	Switch ON, See Figure 8	25°C	5 V		17.5		pF
Digital input capacitance	C _{IN}	V _{IN} = V ₊ or GND,	See Figure 8	25°C	5 V		2.8		pF
Bandwidth	BW	R _L = 50 Ω,	Switch ON, See Figure 11	25°C	4.5 V		220		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 12	25°C	4.5 V		−65		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 13	25°C	4.5 V		−66		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 15	25°C	4.5 V		0.01		%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	25°C	5.5 V			1	μA
				Full				10	
Change in supply current	ΔI ₊	V _{IN} = V ₊ − 0.6 V		Full	5.5 V			500	μA

Electrical Characteristics for 3.3-V Supply

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -24\text{ mA}$, Switch ON, See Figure 6	Full	3 V			23	Ω
ON-state resistance match between channels	Δr_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 2.1\text{ V}$, $I_{\text{COM}} = -24\text{ mA}$, Switch ON, See Figure 6	25°C	3 V		0.2		Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -24\text{ mA}$, Switch ON, See Figure 6	25°C	3 V		9		Ω
NC, NO OFF leakage current	$I_{\text{NC(OFF)}}, I_{\text{NO(OFF)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = 0 \text{ to } V_+$, Switch OFF, See Figure 7	25°C Full	3.6 V	-1	0.05	1	μA
NC, NO ON leakage current	$I_{\text{NC(ON)}}, I_{\text{NO(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = \text{Open}$, Switch ON, See Figure 7	25°C Full	3.6 V	-0.1		0.1	μA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}$, $V_{\text{COM}} = 0 \text{ to } V_+$, Switch ON, See Figure 7	25°C Full	3.6 V	-0.1		0.1	μA
Digital Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		$V_+ \times 0.7$			V
Input logic low	V_{IL}		Full		$V_+ \times 0.3$			V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{IN}} = 5.5\text{ V or }0$	25°C Full	3.6 V	-1	0.05	1	μA
Dynamic								
Turn-on time	t_{ON}	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$, or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$, $R_L = 500\text{ } \Omega$, $C_L = 50\text{ pF}$, See Figure 9	Full	3 V to 3.6 V	2.0		10.6	ns
Turn-off time	t_{OFF}	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$, or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$, $R_L = 500\text{ } \Omega$, $C_L = 50\text{ pF}$, See Figure 9	Full	3 V to 3.6 V	1.0		8.3	ns
Break-before-make time	t_{BBM}	$V_{\text{NC}} = V_{\text{NO}} = V_+/2$, $R_L = 50\text{ } \Omega$, $C_L = 35\text{ pF}$, See Figure 10	25°C	3 V to 3.6 V	0.5			ns
Charge injection	Q_C	$R_L = 50\text{ } \Omega$, $C_L = 0.1\text{ nF}$, See Figure 14	25°C	3.3 V		3		pC
Bandwidth	BW	$R_L = 50\text{ } \Omega$, Switch ON, See Figure 11	25°C	3 V		220		MHz
OFF isolation	O_{ISO}	$R_L = 50\text{ } \Omega$, $f = 10\text{ MHz}$, Switch OFF, See Figure 12	25°C	3 V		-65		dB
Crosstalk	X_{TALK}	$R_L = 50\text{ } \Omega$, $f = 10\text{ MHz}$, Switch ON, See Figure 13	25°C	3 V		-66		dB
Total harmonic distortion	THD	$R_L = 600\text{ } \Omega$, $C_L = 50\text{ pF}$, $f = 600\text{ Hz to }20\text{ kHz}$, See Figure 15	25°C	3 V		0.015		%
Supply								
Positive supply current	I_+	$V_{\text{IN}} = V_+ \text{ or GND}$, Switch ON or OFF	25°C Full	3.6 V			1 10	μA
Change in supply current	ΔI_+	$V_{\text{IN}} = V_+ - 0.6\text{ V}$	Full	3.6 V			500	μA

(1) $T_A = 25^\circ\text{C}$

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TS5A23157-Q1

DUAL 15-Ω SPDT ANALOG SWITCH

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Electrical Characteristics for 2.5-V Supply

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -8 \text{ mA}$, Switch ON, See Figure 6	Full	2.3 V			50	Ω
ON-state resistance match between channels	Δr_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.6 \text{ V}$, $I_{\text{COM}} = -8 \text{ mA}$, Switch ON, See Figure 6	25°C	2.3 V		0.5		Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -8 \text{ mA}$, Switch ON, See Figure 6	25°C	2.3 V		27		Ω
NC, NO OFF leakage current	$I_{\text{NC(OFF)}}, I_{\text{NO(OFF)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = 0 \text{ to } V_+$, Switch OFF, See Figure 7	25°C Full	2.7 V	-1	0.05	1	μA
NC, NO ON leakage current	$I_{\text{NC(ON)}}, I_{\text{NO(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = \text{Open}$, Switch ON, See Figure 7	25°C Full	2.7 V	-0.1		0.1	μA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}$, $V_{\text{COM}} = 0 \text{ to } V_+$, Switch ON, See Figure 7	25°C Full	2.7 V	-0.1		0.1	μA
Digital Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		$V_+ \times 0.7$			V
Input logic low	V_{IL}		Full		$V_+ \times 0.3$			V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{IN}} = 5.5 \text{ V or } 0$	25°C Full	2.7 V	-1	0.05	1	μA
Dynamic								
Turn-on time	t_{ON}	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$, or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$, $R_L = 500 \text{ } \Omega$, $C_L = 50 \text{ pF}$, See Figure 9	Full	2.3 V to 2.7 V	2.5		17	ns
Turn-off time	t_{OFF}	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$, or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$, $R_L = 500 \text{ } \Omega$, $C_L = 50 \text{ pF}$, See Figure 9	Full	2.3 V to 2.7 V	1.5		10.5	ns
Break-before-make time	t_{BBM}	$V_{\text{NC}} = V_{\text{NO}} = V_+/2$, $R_L = 50 \text{ } \Omega$, $C_L = 35 \text{ pF}$, See Figure 10	25°C	2.3 V to 2.7 V	0.5			ns
Bandwidth	BW	$R_L = 50 \text{ } \Omega$, Switch ON, See Figure 11	25°C	2.3 V		220		MHz
OFF isolation	O_{ISO}	$R_L = 50 \text{ } \Omega$, $f = 10 \text{ MHz}$, Switch OFF, See Figure 12	25°C	2.3 V		-65		dB
Crosstalk	X_{TALK}	$R_L = 50 \text{ } \Omega$, $f = 10 \text{ MHz}$, Switch ON, See Figure 13	25°C	2.3 V		-66		dB
Total harmonic distortion	THD	$R_L = 600 \text{ } \Omega$, $C_L = 50 \text{ pF}$, $f = 600 \text{ Hz to } 20 \text{ kHz}$, See Figure 15	25°C	2.3 V		0.025		%
Supply								
Positive supply current	I_+	$V_{\text{IN}} = V_+ \text{ or GND}$, Switch ON or OFF	25°C Full	2.7 V			1 10	μA
Change in supply current	ΔI_+	$V_{\text{IN}} = V_+ - 0.6 \text{ V}$	Full	2.7 V			500	μA

(1) $T_A = 25^\circ\text{C}$

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply

 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$				0		V_+	V
ON-state resistance	r_{on}	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -4 \text{ mA}$, Switch ON, See Figure 6	Full	1.65 V			160	Ω
ON-state resistance match between channels	Δr_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.15 \text{ V}$, $I_{\text{COM}} = -4 \text{ mA}$, Switch ON, See Figure 6	25°C	1.65 V		1		Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq V_{\text{NO}} \text{ or } V_{\text{NC}} \leq V_+$, $I_{\text{COM}} = -4 \text{ mA}$, Switch ON, See Figure 6	25°C	1.65 V		110		Ω
NC, NO OFF leakage current	$I_{\text{NC(OFF)}}, I_{\text{NO(OFF)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = 0 \text{ to } V_+$, Switch OFF, See Figure 7	25°C Full	1.95 V	-1	0.05	1	μA
NC, NO ON leakage current	$I_{\text{NC(ON)}}, I_{\text{NO(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0 \text{ to } V_+$, $V_{\text{COM}} = \text{Open}$, Switch ON, See Figure 7	25°C Full	1.95 V	-0.1		0.1	μA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}$, $V_{\text{COM}} = 0 \text{ to } V_+$, Switch ON, See Figure 7	25°C Full	1.95 V	-0.1		0.1	μA
Digital Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		$V_+ \times 0.75$			V
Input logic low	V_{IL}		Full		$V_+ \times 0.25$			V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{IN}} = 5.5 \text{ V or } 0$	25°C Full	1.95 V	-1	0.05	1	μA
Dynamic								
Turn-on time	t_{ON}	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$, or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$, $R_L = 500 \text{ } \Omega$, $C_L = 50 \text{ pF}$, See Figure 9	Full	1.65 V to 1.95 V	5.5		27	ns
Turn-off time	t_{OFF}	$V_{\text{NC}} = \text{GND and } V_{\text{NO}} = V_+$, or $V_{\text{NC}} = V_+ \text{ and } V_{\text{NO}} = \text{GND}$, $R_L = 500 \text{ } \Omega$, $C_L = 50 \text{ pF}$, See Figure 9	Full	1.65 V to 1.95 V	2		16	ns
Break-before-make time	t_{BBM}	$V_{\text{NC}} = V_{\text{NO}} = V_+/2$, $R_L = 50 \text{ } \Omega$, $C_L = 35 \text{ pF}$, See Figure 10	25°C	1.65 V to 1.95 V	0.5			ns
Bandwidth	BW	$R_L = 50 \text{ } \Omega$, Switch ON, See Figure 11	25°C	1.8 V		220		MHz
OFF isolation	O_{ISO}	$R_L = 50 \text{ } \Omega$, $f = 10 \text{ MHz}$, Switch OFF, See Figure 12	25°C	1.8 V		-60		dB
Crosstalk	X_{TALK}	$R_L = 50 \text{ } \Omega$, $f = 10 \text{ MHz}$, Switch ON, See Figure 13	25°C	1.8 V		-66		dB
Total harmonic distortion	THD	$R_L = 600 \text{ } \Omega$, $C_L = 50 \text{ pF}$, $f = 600 \text{ Hz to } 20 \text{ kHz}$, See Figure 15	25°C	1.8 V		0.015		%
Supply								
Positive supply current	I_+	$V_{\text{IN}} = V_+ \text{ or GND}$, Switch ON or OFF	25°C Full	1.95 V			1 10	μA
Change in supply current	ΔI_+	$V_{\text{IN}} = V_+ - 0.6 \text{ V}$	Full	1.95 V			500	μA

(1) $T_A = 25^\circ\text{C}$

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TYPICAL CHARACTERISTICS

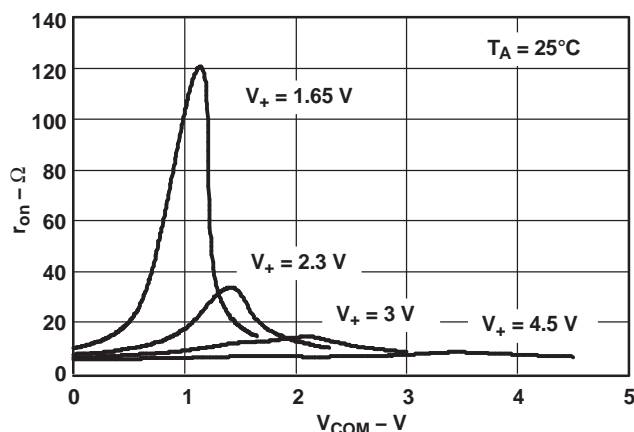


Figure 1. r_{on} vs V_{COM}

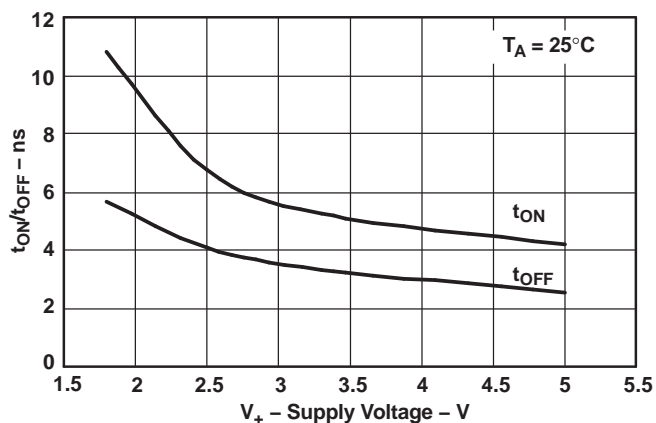


Figure 2. t_{ON} and t_{OFF} vs V_+

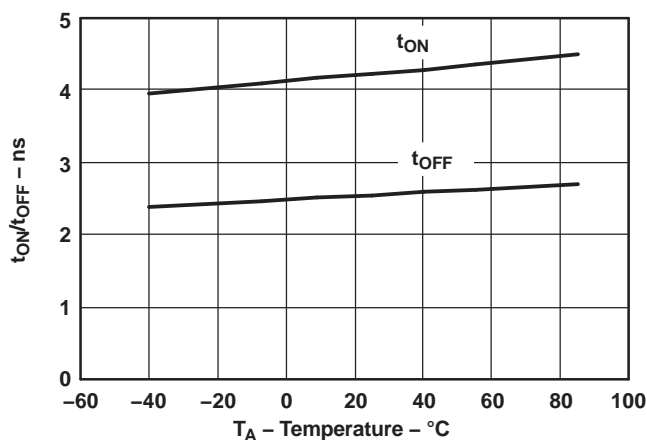


Figure 3. t_{ON} and t_{OFF} vs Temperature
($V_+ = 5$ V)

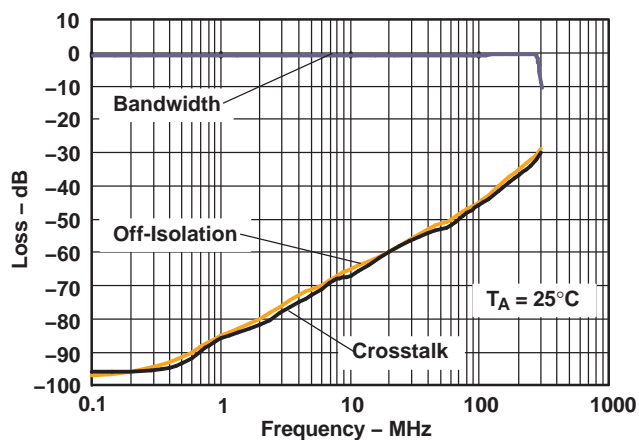


Figure 4. Frequency Response ($V_+ = 3$ V)

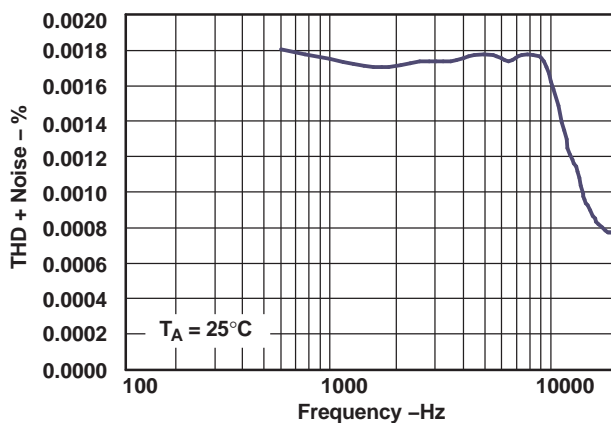


Figure 5. Total Harmonic Distortion (THD)
vs Frequency ($V_+ = 3$ V)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	IN1	Digital control to connect COM to NO or NC
2	NO1	Normally open
3	GND	Digital ground
4	NO2	Normally open
5	IN2	Digital control to connect COM to NO or NC
6	COM2	Common
7	NC2	Normally closed
8	V ₊	Power supply
9	NC1	Normally closed
10	COM1	Common

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NC}	Voltage at NC
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr _{on}	Difference of r _{on} between channels
r _{on(flat)}	Difference between the maximum and minimum value of r _{on} in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (NO to COM or NC to COM) in the ON state and the output (NC or NO) being open
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Minimum input voltage for logic low for the control input (IN)
V _{IN}	Voltage at IN
I _{IH} , I _{IL}	Leakage current measured at IN
t _{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning ON.
t _{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM/NC/NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulombs (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q _C = C _L × ΔV _O , C _L is the load capacitance and ΔV _O is the change in analog output voltage.
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NC to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NC to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C _{IN}	Capacitance of IN

TS5A23157-Q1

DUAL 15-Ω SPDT ANALOG SWITCH

SCS252-JULY 2003 [查看"TS5A23157-Q1"供应商](#)

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state. OFF isolation, $O_{ISO} = 20 \text{ LOG } (V_{NC}/V_{COM})$ dB, V_{COM} is the input and V_{NC} is the output.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured at a specific frequency and in dB. Crosstalk, $X_{TALK} = 20 \text{ log } (V_{NC1}/V_{NO1})$, V_{NO1} is the input and V_{NC1} is the output.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is -3 dB below the dc gain. Gain is measured from the equation, $20 \text{ log } (V_{NC}/V_{COM})$ dB, where V_{NC} is the output and V_{COM} is the input.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

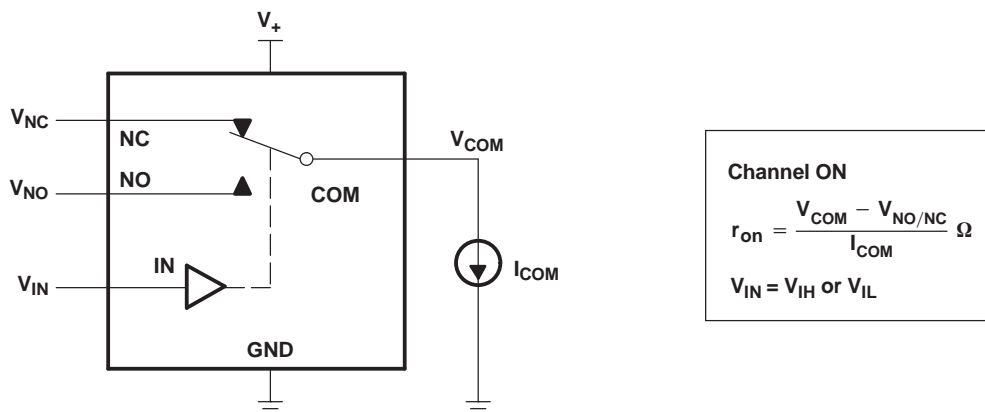


Figure 6. ON-State Resistance (R_{on})

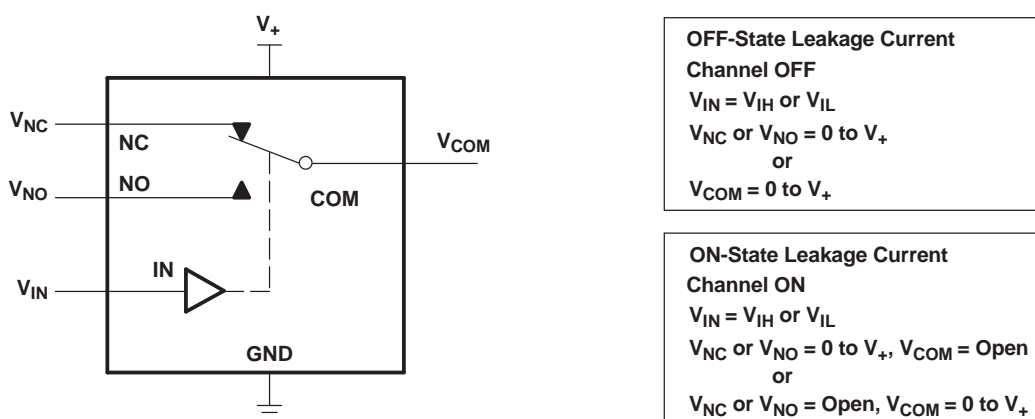


Figure 7. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

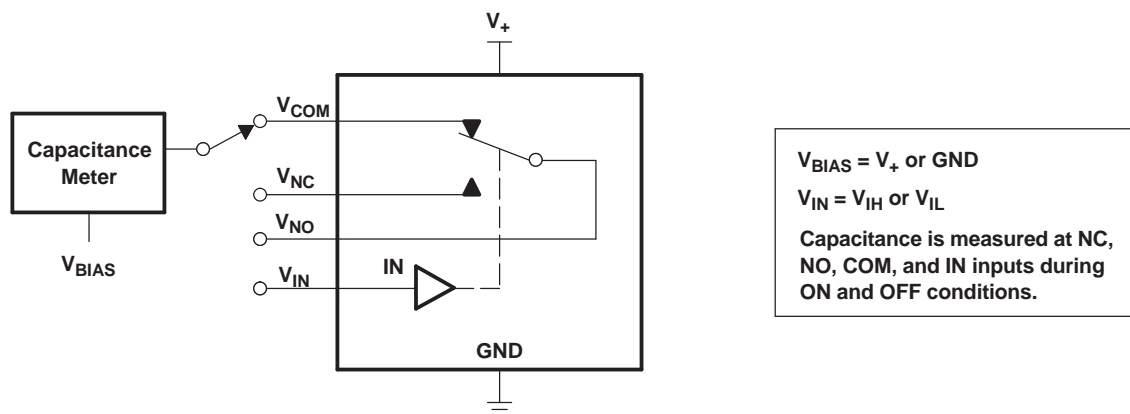


Figure 8. Capacitance (C_{IN} , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

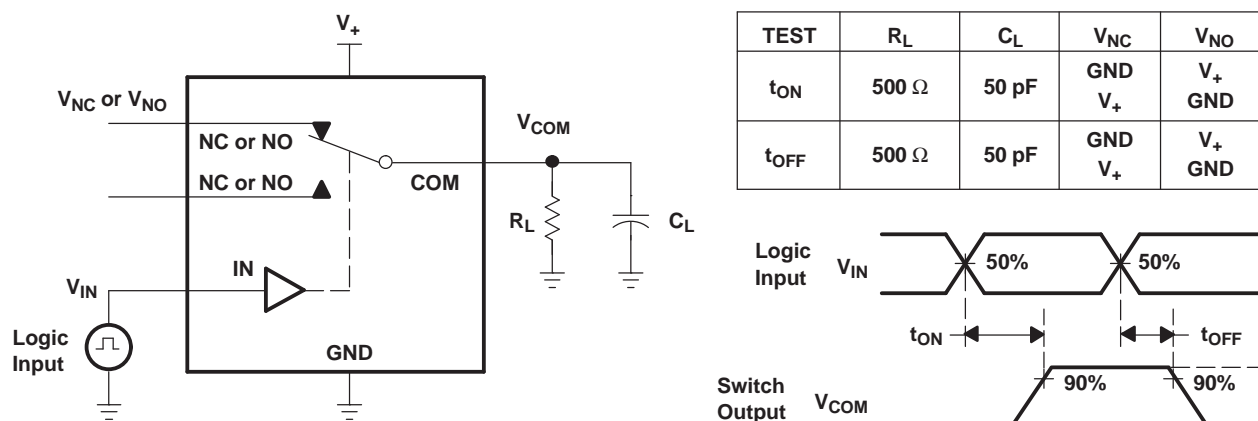


Figure 9. Turn-On Time (t_{ON}) and Turn-Off Time (t_{OFF})

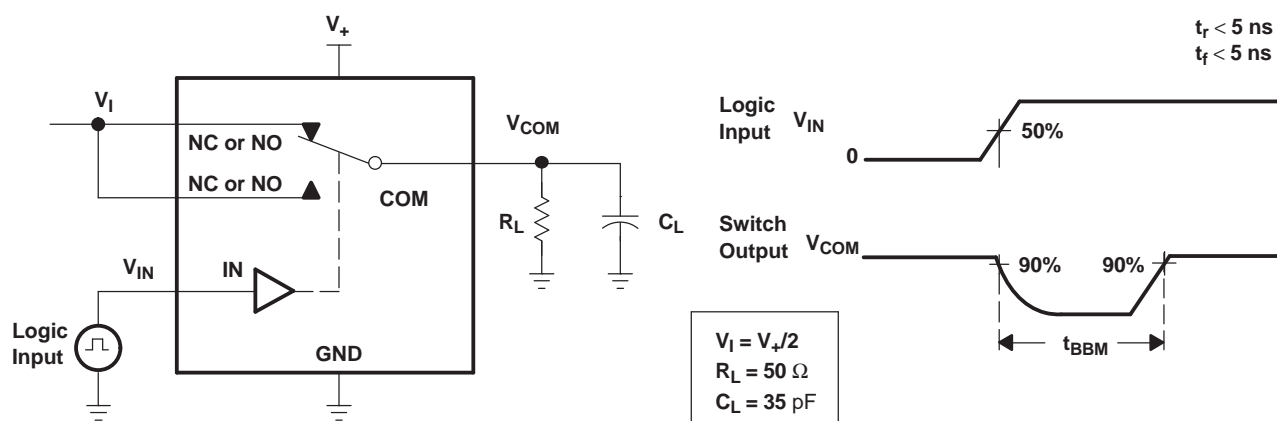


Figure 10. Break-Before-Make Time (t_{BBM})

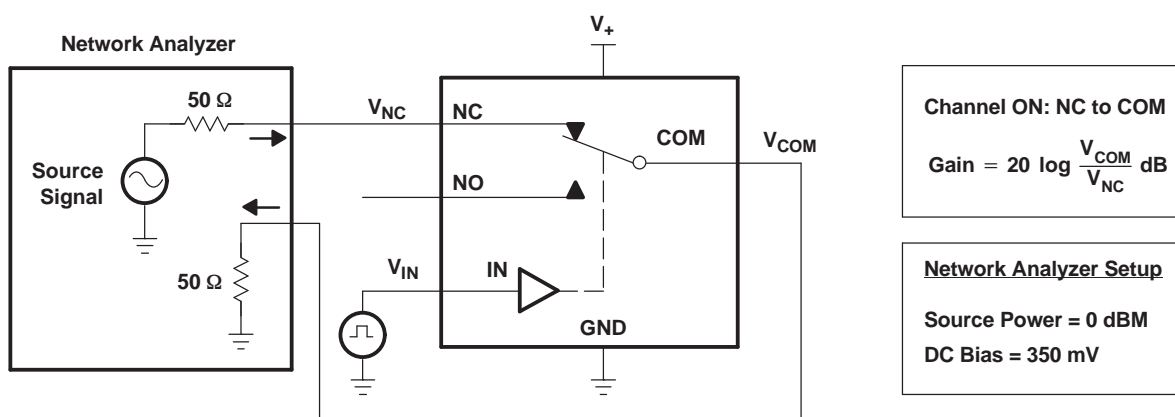


Figure 11. Frequency Response (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

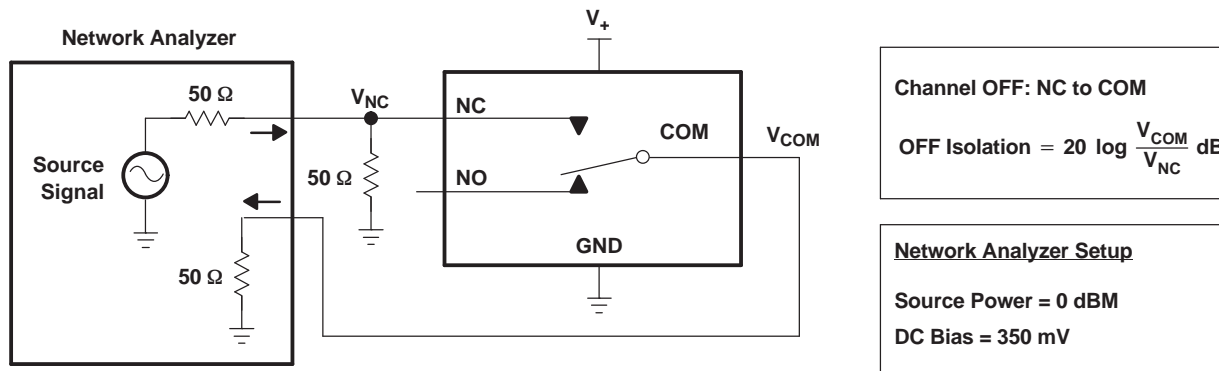


Figure 12. OFF Isolation (O_{Iso})

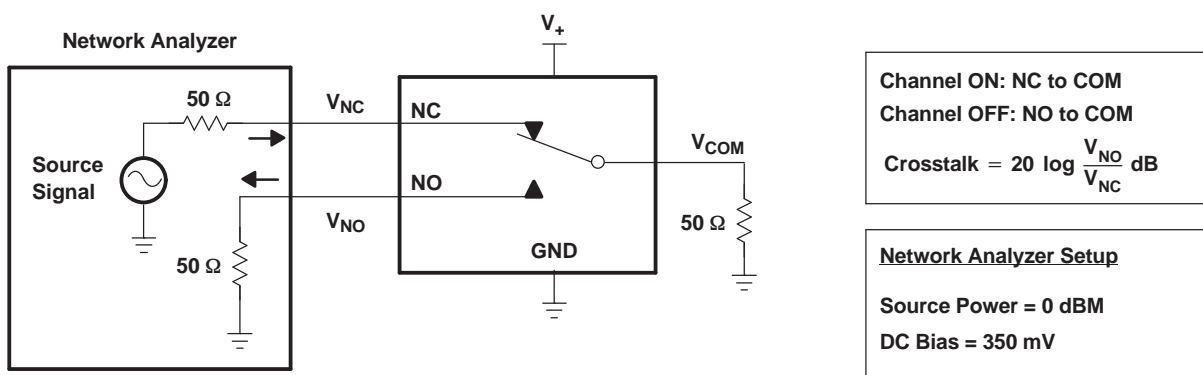


Figure 13. Crosstalk (X_{TALK})

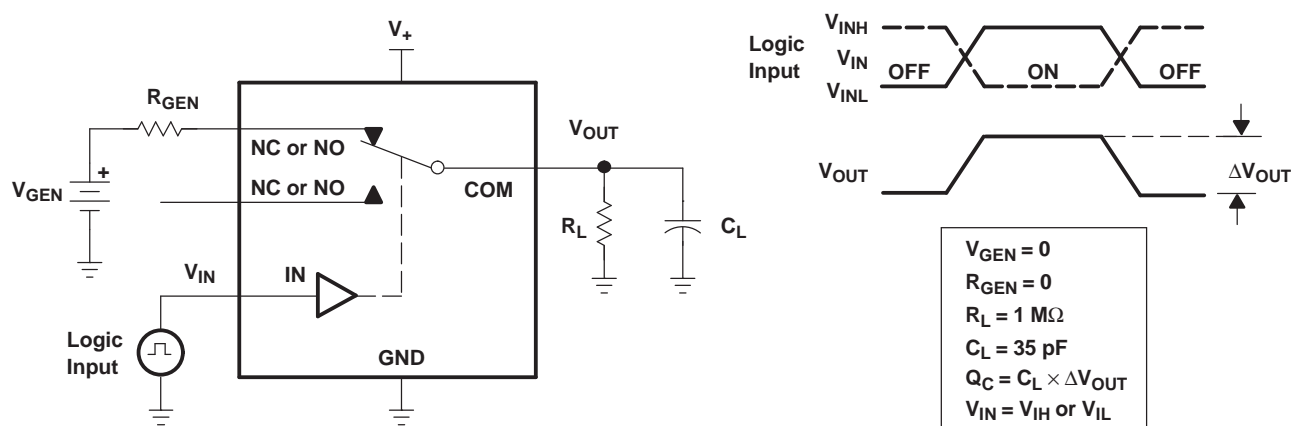


Figure 14. Charge Injection (Q_C)

PARAMETER MEASUREMENT INFORMATION (continued)

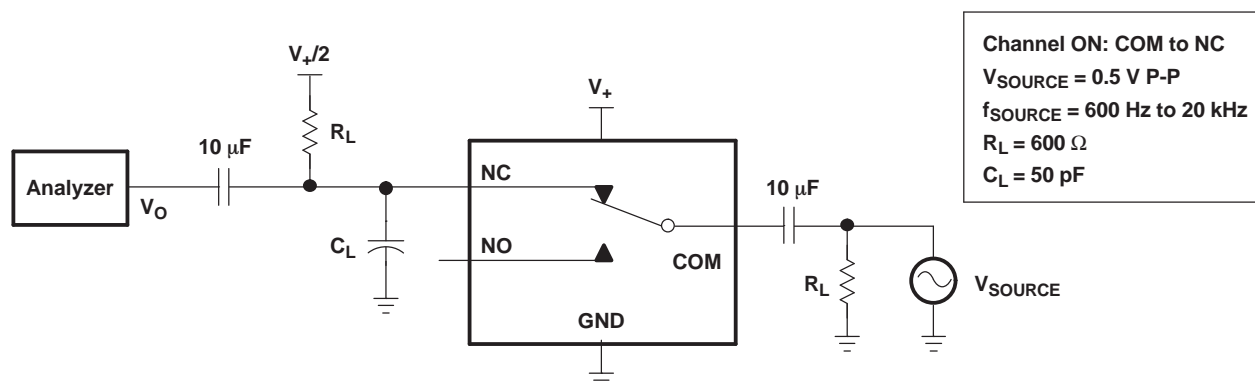


Figure 15. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TS5A23157TDGSRQ1	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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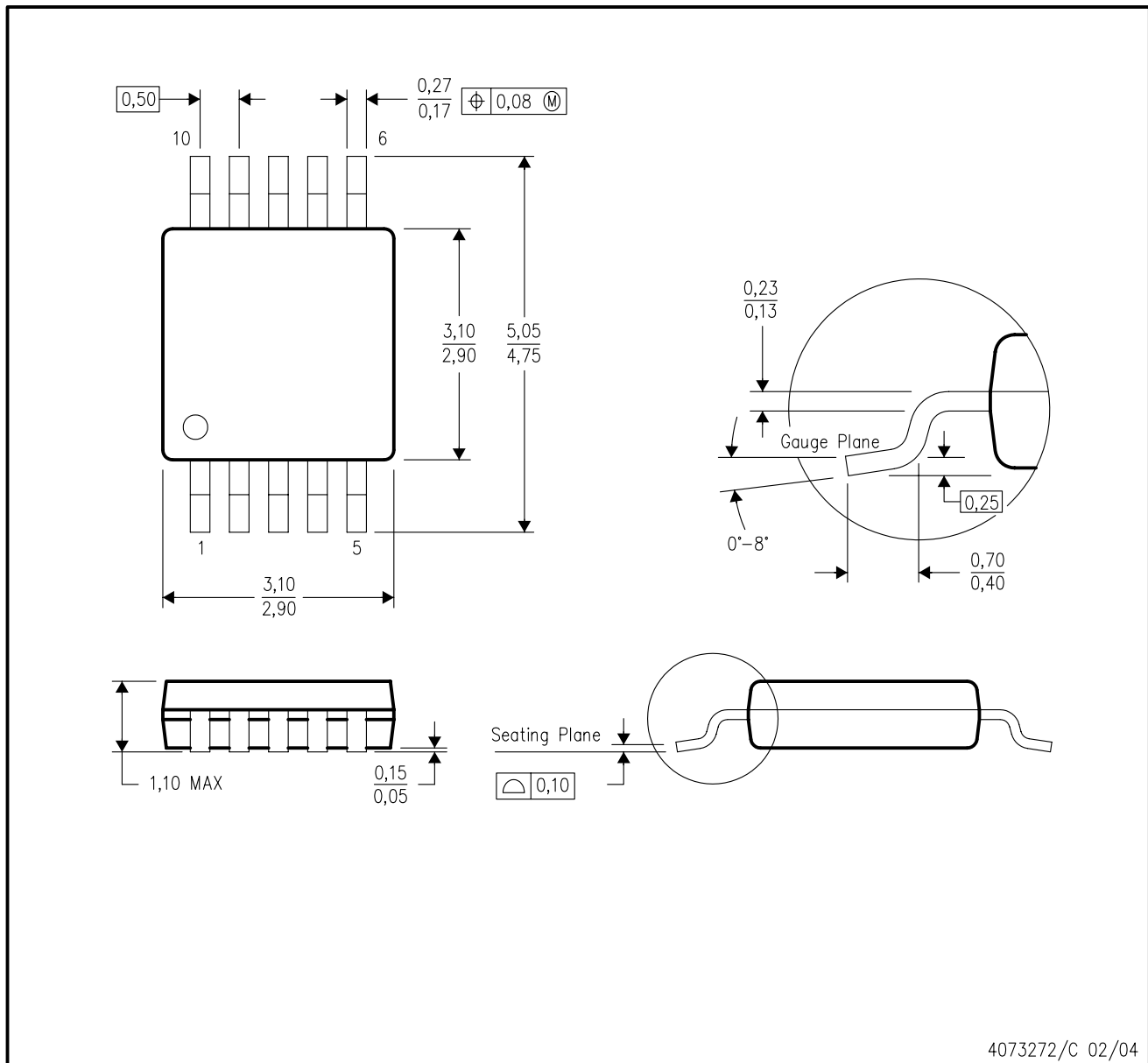
- Catalog: [TS5A23157](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

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