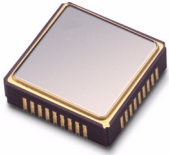




**GENERAL DESCRIPTION**

The M1025/26 is a VCSO (Voltage Controlled SAW Oscillator) based clock jitter attenuator PLL designed for clock jitter attenuation and frequency translation. The device is ideal for generating the transmit reference clock for optical network systems supporting up to 2.5Gb data rates. It can serve to jitter attenuate a stratum reference clock or a recovered clock in loop timing mode. The M1025/26 module includes a proprietary SAW (surface acoustic wave) delay line as part of the VCSO. This results in a high frequency, high-Q, low phase noise oscillator that assures low intrinsic output jitter.



**PIN ASSIGNMENT (9 x 9 mm SMT)**

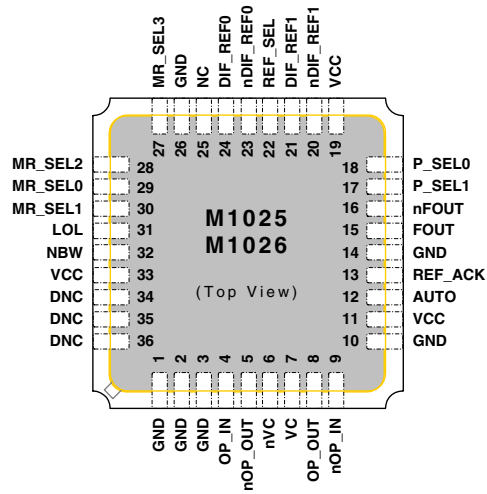


Figure 1: Pin Assignment

**FEATURES**

- ◆ Integrated SAW delay line; low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz)
- ◆ Output frequencies of 62.5 to 175 MHz (Specify VCSO output frequency at time of order)
- ◆ LVPECL clock output (CML and LVDS options available)
- ◆ Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTTL
- ◆ Loss of Lock (LOL) output pin; Narrow Bandwidth control input (NBW pin)
- ◆ AutoSwitch (AUTO pin) - automatic (non-revertive) reference clock reselection upon clock failure
- ◆ Acknowledge pin (REF\_ACK pin) indicates the actively selected reference input
- ◆ Hitless Switching (HS) options with or without Phase Build-out (PBO) to enable SONET (GR-253) /SDH (G.813) MTIE and TDEV compliance during reselection
- ◆ Pin-selectable feedback and reference divider ratios
- ◆ Single 3.3V power supply
- ◆ Small 9 x 9 mm SMT (surface mount) package

**Example I/O Clock Frequency Combinations Using M1025-11-155.5200 or M1026-11-155.5200**

Input Reference Clock (MHz)		PLL Ratio (Pin Selectable)		Output Clock (MHz) (Pin Selectable)
(M1025)	(M1026)	(M1025)	(M1026)	
19.44 or 38.88		8 or 4		155.52
	77.76	2		or
	155.52	1		77.76
	622.08	0.25		

Table 1: Example I/O Clock Frequency Combinations

**SIMPLIFIED BLOCK DIAGRAM**

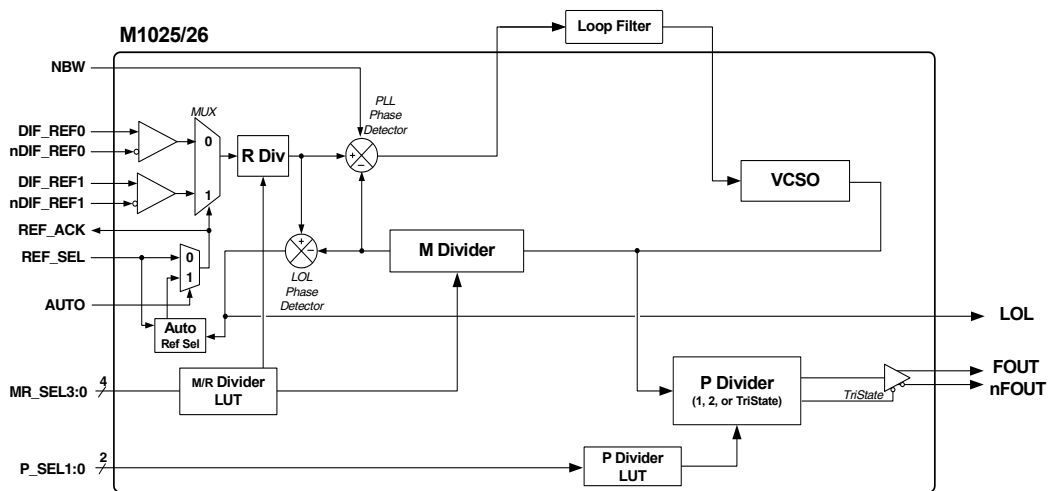


Figure 2: Simplified Block Diagram



## PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 9.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12	AUTO	Input	Internal pull-down resistor <sup>1</sup>	Automatic/manual reselection mode for clock input: Logic 1 automatic reselection upon clock failure (non-revertive) Logic 0 manual selection only (using REF_SEL)
13	REF_ACK	Output		Reference Acknowledgement pin for input mux state; outputs the currently selected reference input pair: Logic 1 indicates nDIF_REF1, DIF_REF1 Logic 0 indicates nDIF_REF0, DIF_REF0
15 16	FOUT nFOUT	Output	No internal terminator	Clock output pair. Differential LVPECL (CML, LVDS available).
17 18	P_SEL1 P_SEL0		Internal pull-down resistor <sup>1</sup>	Post-PLL, P divider selection. LVCMOS/LVTTL. See Table 5, P Divider Look-Up Table (LUT), on pg. 4.
20	nDIF_REF1	Input	Biased to $V_{cc}/2$ <sup>2</sup>	Reference clock input pair 1. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
21	DIF_REF1		Internal pull-down resistor <sup>1</sup>	
22	REF_SEL	Input	Internal pull-down resistor <sup>1</sup>	Reference clock input selection. LVCMOS/LVTTL: Logic 1 selects DIF_REF1, nDIF_REF1. Logic 0 selects DIF_REF0, nDIF_REF0.
23	nDIF_REF0	Input	Biased to $V_{cc}/2$ <sup>2</sup>	Reference clock input pair 0. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
24	DIF_REF0		Internal pull-down resistor <sup>1</sup>	
25	NC			No internal connection.
27 28 29 30	MR_SEL3 MR_SEL2 MR_SEL0 MR_SEL1	Input	Internal pull-down resistor <sup>1</sup>	M and R divider value selection. LVCMOS/ LVTTL. See Tables 3 and 4, M and R Divider Look-Up Tables (LUT) on pg. 3.
31	LOL	Output		Loss of Lock indicator output. Asserted when internal PLL is not tracking the input reference for frequency and phase. <sup>3</sup> Logic 1 indicates loss of lock. Logic 0 indicates locked condition.
32	NBW	Input	Internal pull-UP resistor <sup>1</sup>	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, $R_{IN} = 2100k\Omega$ Logic 0 - Wide bandwidth, $R_{IN} = 100k\Omega$
34, 35, 36	DNC		Do Not Connect.	

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-UP resistors, see **DC Characteristics** on pg. 11.

Note 2: Biased to  $V_{cc}/2$ , with  $50k\Omega$  to  $V_{cc}$  and  $50k\Omega$  to ground. See **Differential Inputs Biased to  $V_{CC}/2$**  on pg. 11.

Note 3: See **LVCMOS Output** in DC Characteristics on pg. 11.

## DETAILED BLOCK DIAGRAM

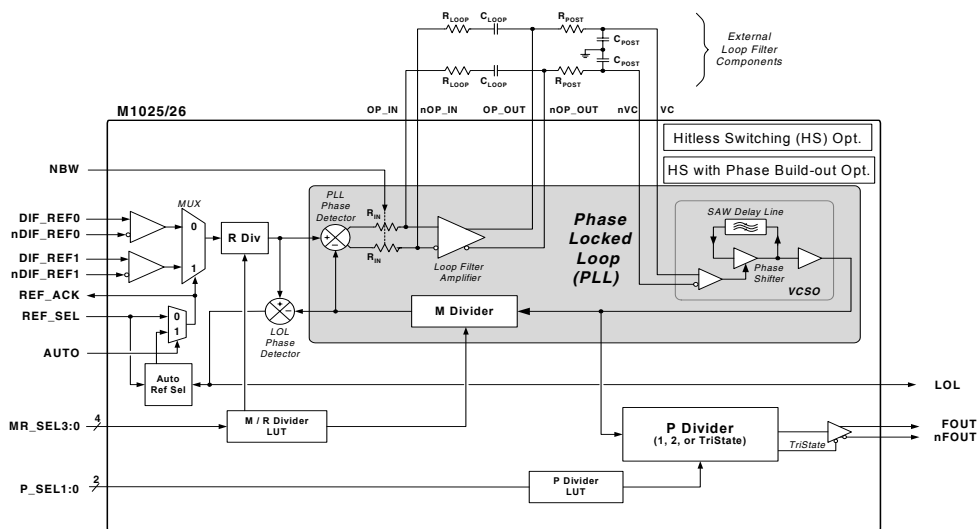


Figure 3: Detailed Block Diagram

## DIVIDER SELECTION TABLES

### M and R Divider Look-Up Tables (LUT)

The MR\_SEL3:0 pins select the feedback and reference divider values M and R to enable adjustment of loop bandwidth and jitter tolerance. The look-up tables vary by device variant. M1025 and M1026 are defined in Tables 3 and 4 respectively.

Tables 3 and 4 provide example  $F_{in}$  and phase detector frequencies with 155.52MHz VCSO devices (M1025-11-155.5200 and M1026-11-155.5200). See "Ordering Information" on pg. 14.

M1025 M/R Divider LUT

MR_SEL3:0	M Div	R Div	Total PLL Ratio	$F_{in}$ for 155.52MHz VCSO (MHz)	Phase Det. Freq. for 155.52MHz VCSO (MHz)
0 0 0 0	8	1	8	19.44	19.44
0 0 0 1	32	4	8	19.44	4.86
0 0 1 0	128	16	8	19.44	1.215
0 0 1 1	512	64	8	19.44	0.30375
0 1 0 0	2	1	2	77.76	77.76
0 1 0 1	8	4	2	77.76	19.44
0 1 1 0	32	16	2	77.76	4.86
0 1 1 1	128	64	2	77.76	1.215
1 0 0 0	1	1	1	155.52	155.52
1 0 0 1	4	4	1	155.52	38.88
1 0 1 0	16	16	1	155.52	9.72
1 0 1 1	64	64	1	155.52	2.43
1 1 0 0	Test Mode <sup>1</sup>	N/A	N/A	N/A	N/A
1 1 0 1	1	4	0.25	622.08	155.52
1 1 1 0	4	16	0.25	622.08	38.88
1 1 1 1	16	64	0.25	622.08	9.72

Table 3: M1025 M/R Divider LUT

Note 1: Factory test mode; do not use.

M1026 M/R Divider LUT

MR_SEL3:0	M Div	R Div	Total PLL Ratio	$F_{in}$ for 155.52MHz VCSO (MHz)	Phase Det. Freq. for 155.52MHz VCSO (MHz)
0 0 0 0	4	1	4	38.88	38.88
0 0 0 1	16	4	4	38.88	9.72
0 0 1 0	64	16	4	38.88	2.43
0 0 1 1	256	64	4	38.88	0.6075
0 1 0 0	2	1	2	77.76	77.76
0 1 0 1	8	4	2	77.76	19.44
0 1 1 0	32	16	2	77.76	4.86
0 1 1 1	128	64	2	77.76	1.215
1 0 0 0	1	1	1	155.52	155.52
1 0 0 1	4	4	1	155.52	38.88
1 0 1 0	16	16	1	155.52	9.72
1 0 1 1	64	64	1	155.52	2.43
1 1 0 0	Test Mode <sup>1</sup>	N/A	N/A	N/A	N/A
1 1 0 1	1	4	0.25	622.08	155.52
1 1 1 0	4	16	0.25	622.08	38.88
1 1 1 1	16	64	0.25	622.08	9.72

Table 4: M1026 M/R Divider LUT

Note 1: Factory test mode; do not use.



### General Guidelines for M and R Divider Selection

General guidelines for M/R divider selection (see following pages for more detail):

- A lower phase detector frequency should be used for loop timing applications to assure PLL tracking, especially during GR-253 jitter tolerance testing. The recommended maximum phase detector frequency for loop timing mode is 19.44MHz. The LOL pin should not be used during loop timing mode.
- When LOL is to be used for system health monitoring, the phase detector frequency should be 5MHz or greater. Low phase detector frequencies make LOL overly sensitive, and higher phase detector frequencies make LOL less sensitive.
- The preceding guideline also applies when using the AutoSwitch Mode, since AutoSwitch uses the LOL output for clock fault detection.

### P Divider Look-Up Table (LUT)

The P\_SEL1 and P\_SEL0 pins select the post-PLL divider value P. The output frequency of the SAW can be divided by 1 or 2 or the output can be TriStated as specified in Table 5.

P_SEL1:0	P Value	M1025-155.5200 or M1026-155.5200 Output Frequency (MHz)
0 0	2	77.76
0 1	1	155.52
1 0	2	77.76
1 1	TriState	N/A

Table 5: P Divider Look-Up Table (LUT)

## FUNCTIONAL DESCRIPTION

The M1025/26 is a PLL (Phase Locked Loop) based clock generator that generates an output clock synchronized to one of two selectable input reference clocks. An internal high "Q" SAW delay line provides low jitter signal performance.

A pin-selected look-up table is used to select the PLL feedback divider (M Div) and reference divider (R Div) as shown in Tables 3 and 4 on pg. 3. These look-up tables provide flexibility in both the overall frequency multiplication ratio (total PLL ratio) and phase detector frequency.

The M1025/26 includes a Loss of Lock (LOL) indicator, which provides status information to system management software. A Narrow Bandwidth (NBW) control pin is provided as an additional mechanism for adjusting PLL loop bandwidth without affecting the phase detector frequency.

An automatic input reselection feature, or "AutoSwitch" is also included in the M1025/26. When the AutoSwitch mode is enabled, the device will automatically switch to the other reference clock input when the currently selected reference clock fails. Reference selection is non-revertive, meaning that only one reference reselection will be made each time that AutoSwitch is re-enabled.

In addition to the AutoSwitch feature, Hitless Switching and Phase Build-out options can be ordered with the device. The Hitless Switching and Phase Build-out options help assure SONET/SDH MTIE and TDEV compliance during either a manual or automatic input reference reselection.

### Input Reference Clocks

Two clock reference inputs and a selection mux are provided. Either reference clock input can accept a differential clock signal (such as LVPECL or LVDS) or a single-ended clock input (LVCMOS or LVTTTL on the non-inverting input).

*A single-ended reference clock on the unselected reference input can cause an increase in output clock jitter. For this reason, differential reference inputs are preferred; interference from a differential input on the non-selected input is minimal.*

Implementation of single-ended input has been facilitated by biasing nDIF\_REF0 and nDEF\_REF1 to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. Figure 4 shows the input clock structure and how it is used with either LVCMOS / LVTTTL inputs or a DC- coupled LVPECL clock.

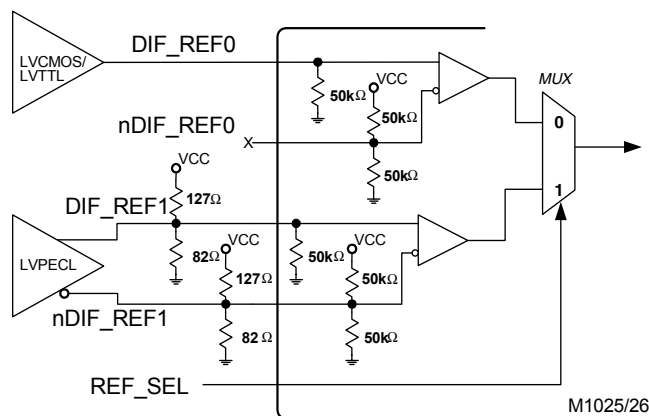


Figure 4: Input Reference Clocks

### Differential LVPECL Inputs

Differential LVPECL inputs are connected to both reference input pins in the usual manner. The external load termination resistors shown in Figure 4 (the 127Ω and 82Ω resistors) will work for both AC and DC coupled LVPECL reference clock lines. These provide the 50Ω load termination and the VTT bias voltage.

### Single-ended Inputs

Single-ended inputs (LVCMOS or LVTTTL) are connected to the non-inverting reference input pin (DIF\_REF0 or DIF\_REF1). The inverting reference input pin (nDIF\_REF0 or nDIF\_REF1) must be left unconnected.

*In single-ended operation, when the unused inverting input pin (nDIF\_REF0 or nDEF\_REF1) is left floating (not connected), the input will self-bias at VCC/2.*

### PLL Operation

The M1025/26 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The “M” divider divides the VCSO output frequency, feeding the result into the plus input of the phase detector. The output of the “R” divider is fed into the minus input of the phase detector. The phase detector compares its two inputs. The phase detector output, filtered externally, causes the VCSO to increase or decrease in speed as needed to phase- and frequency-lock the VCSO to the reference input.

*The value of the M divider directly affects closed loop bandwidth.*

The relationship between the nominal VCSO center frequency (Fvcso), the M divider, the R divider, and the input reference frequency (Fin) is:

$$F_{vcso} = F_{in} \times \frac{M}{R}$$

For the available M divider and R divider look-up table combinations, Tables 3 and 4 on pg. 3 list the Total PLL Ratio as well as Fin when using the M1025-11-155.5200 or the M1026-11-155.5200. (“Ordering Information”, pg. 14.)

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

### Post-PLL Divider

The M1025/26 features a post-PLL (P) divider. By using the P Divider, the device’s output frequency (Fout) can be the VCSO center frequency (Fvcso) or 1/2 Fvcso.

The P\_SEL pin selects the value for the P divider: logic 1 sets P to 2, logic 0 sets P to 1. (See Table 5 on pg. 4.)

When the P divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$F_{out} = \frac{F_{vcso}}{P} = F_{in} \times \frac{M}{R \times P}$$

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.



### TriState

The TriState feature puts the LVPECL output driver into a high impedance state, effectively disconnecting the driver from the FOUT and nFOUT pins of the device. A logic 0 is then present on the clock net. The impedance of the clock net is then set to  $50\Omega$  by the external circuit resistors. (This is in distinction to a CMOS output in TriState, in which case the net goes to a high impedance and the logic value floats.) The  $50\Omega$  impedance level of the LVPECL TriState allows manufacturing In-circuit Test to drive the clock net with an external  $50\Omega$  generator to validate the integrity of clock net and the clock load.

*Any unused output (single-ended or differential) should be left unconnected (floating) in system application. This minimizes output switching current and therefore minimizes noise modulation of the VCSO.*

### Loss of Lock Indicator (LOL) Output Pin

Under normal device operation, when the PLL is locked, the LOL Phase Detector drives LOL to logic 0. Under circumstances when the VCSO cannot lock to the input (as measured by a greater than 4 ns discrepancy between the feedback and reference clock rising edges at the LOL Phase Detector) the LOL output goes to logic 1. The LOL pin will return back to logic 0 when the phase detector error is less than 2 ns. The loss of lock indicator is a low current LVCMOS output.

### Guidelines Using LOL

As described, the LOL pin indicates when the PLL is out-of-lock with the input reference. The LOL condition is also used by the AutoSwitch circuit to detect a lost reference, as described in following sections. LOL is also used by the Hitless Switching and Phase Build-out functions (optional device features).

To ensure reliable operation of LOL and guard against false out-of-lock indications, the following conditions should be met:

- The phase detector frequency should be no less than 5MHz, and preferably it should be 10MHz or greater. Phase detector frequency is defined by  $F_{in} / R$ . A higher phase detector frequency will result in lower phase error and less chance of false triggering the LOL phase detector. Refer to Tables 3 and 4 on pg. 3 for phase detector frequency when using the M1025-11-155.5200 or the M1026-11-155.5200.
- The input reference should have an intrinsic jitter of less than 1 ns pk-pk. If reference jitter is greater than 1 ns pk-pk, the LOL circuit might falsely trigger. Due to this limitation, the LOL circuit should not be used in loop timing mode, nor should it be used with a noisy reference clock. Likewise, the AutoSwitch, Hitless Switching, or Phase Build-out features should not be used in loop timing mode or with a noisy reference clock, since these features depend on LOL.

### Reference Acknowledgement (REF\_ACK) Output

The REF\_ACK (reference acknowledgement) pin outputs the value of the reference clock input that is routed to the phase detector. Logic 1 indicates input pair 1 (nDIF\_REF1, DIF\_REF1); logic 0 indicates input pair 0 (nDIF\_REF0, DIF\_REF0). The REF\_ACK indicator is an LVCMOS output.



### AutoSwitch (AUTO) Reference Clock Reselection

This device offers an automatic reference clock reselection feature for switching input reference clocks upon a reference clock failure. With the AUTO input pin set to high and the LOL output low, the device is placed into automatic reselection (AutoSwitch) mode. Once in AutoSwitch mode, when LOL then goes high (due to a reference clock fault), the input clock reference is automatically reselected internally, as indicated by the state change of the REF\_ACK output. Automatic clock reselection is made only once (it is non-revertive). Re-arming of automatic mode requires placing the device into manual selection (Manual Select) mode (AUTO pin low) before returning to AutoSwitch mode (AUTO pin high).

#### Using the AutoSwitch Feature

*See also Table 6, Example AutoSwitch Sequence.*

In application, the system is powered up with the device in Manual Select mode (AUTO pin is set low), allowing sufficient time for the reference clock and device PLL to settle. The REF\_SEL input selects the reference clock to be used in Manual Select mode and the initial reference clock used in AutoSwitch mode. The REF\_SEL input state must be maintained when switching to AutoSwitch mode (AUTO pin high) and must still be maintained until a reference fault occurs.

Once a reference fault occurs, the LOL output goes high and the input reference is automatically reselected. The

REF\_ACK output always indicates the reference selection status and the LOL output always indicates the PLL lock status.

A successful automatic reselection is indicated by a change of state of the REF\_ACK output and a momentary level high of the LOL output (minimum high time is 10 ns).

*If an automatic reselection is made to a non-valid reference clock (one to which the PLL cannot lock), the REF\_ACK output will change state but the LOL output will remain high.*

No further automatic reselection is made; only one reselection is made each time the AutoSwitch mode is armed. AutoSwitch mode is re-armed by placing the device into Manual Select mode (AUTO pin low) and then into AutoSwitch mode again (AUTO pin high).

Following an automatic reselection and prior to selecting Manual Select mode (AUTO pin low), the REF\_SEL pin has no control of reference selection. To prevent an unintentional reference reselection, AutoSwitch mode must not be re-enabled until the desired state of the REF\_SEL pin is set and the LOL output is low. It is recommended to delay the re-arming of AutoSwitch mode, following an automatic reselection, to ensure the PLL is fully locked on the new reference. In most system configurations, where loop bandwidth is in the range of 100-1000 Hz and damping factor below 10, a delay of 500 ms should be sufficient. Until the PLL is fully locked intermittent LOL pulses may occur.

#### Example AutoSwitch Sequence

0 = Low; 1 = High. Example with REF\_SEL initially set to 0 (i.e., DIF\_REF0 selected)

REF_SEL Input	Selected Clock Input	REF_ACK Output	AUTO Input	LOL Output	Conditions
<b>Initialization</b>					
0	DIF_REF0	0	0	1	Device power-up. Manual Select mode. DIF_REF0 input selected reference, not yet locked to.
0	DIF_REF0	0	0	-0-	LOL to 0: Device locked to reference (may get intermittent LOL pulses until fully locked).
0	DIF_REF0	0	-1-	0	AUTO set to 1: Device placed in AutoSwitch mode (with DIF_REF0 as initial reference clock).
<b>Operation &amp; Activation</b>					
0	DIF_REF0	0	1	0	Normal operation with AutoSwitch mode armed, with DIF_REF0 as initial reference clock.
0	DIF_REF0	0	1	-1-	LOL to 1: Clock fault on DIF_REF0, loss of lock indicated by LOL pin, ...
0	-DIF_REF1-	-1-	1	1	... and immediate automatic reselection to DIF_REF1 (indicated by REF_ACK pin).
0	DIF_REF1	1	1	-0-	LOL to 0: Device locks to DIF_REF1 (assuming valid clock on DIF_REF1).
<b>Re-initialization</b>					
-1-	DIF_REF1	1	1	0	REF_SEL set to 1: Prepares for Manual Selection of DIF_REF1 before then re-arming AutoSwitch.
1	DIF_REF1	1	-0-	0	AUTO set to 0: Manual Select mode entered briefly, manually selecting DIF_REF1 as reference.
1	DIF_REF1	1	-1-	0	AUTO set to 1: Device is placed in AutoSwitch mode (delay recommended to ensure device fully locked), re-initializing AutoSwitch with DIF_REF1 now specified as the initial reference clock.

Table 6: Example AutoSwitch Sequence

### Optional Hitless Switching and Phase Build-out

The M1025/26 is available with a Hitless Switching feature that is enabled during device manufacturing. In addition, a Phase Build-out feature is also offered. These features are offered as device options and are specified by device order code. Refer to “Ordering Information” on pg. 14.

The Hitless Switching feature (with or without Phase Build-out) is designed for applications where switching occurs between two stable system reference clocks. It should not be used in loop timing applications, or when reference clock jitter is greater than 1 ns pk-pk. Hitless Switching is triggered by the LOL circuit, which is activated by a 4 ns phase transient. This magnitude of phase transient can be generated by the CDR (Clock & Data Recovery unit) in loop timing mode, especially during a system jitter tolerance test. It can also be generated by some types of Stratum clock DLLs (digital PLL), especially those that do not include a post de-jitter APLL (analog PLL).

When the Hitless Switching feature is enabled, it is always triggered by LOL, whether in AutoSwitch mode (AUTO pin high) or Select mode (AUTO pin low). For example, in Manual mode, the Hitless Switching feature operates when LOL goes high even if there is no reselection of the input mux. This enables the use of an upstream clock mux (such as on the host card), while still providing MTIE compliance when readjusting to the resultant phase change.

When the M1025/26 is operating in wide bandwidth mode (NBW=0), the optional Hitless Switching function puts the device into narrow bandwidth mode when activated. This allows the PLL to lock the new input clock phase gradually. With proper configuration of the external loop filter, the output clock complies with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The optional proprietary Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock. The PBO function selects a new VCSO clock edge for the PLL Phase Detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

The Hitless Switching and Phase Build-out functions are triggered by the LOL circuit. For proper operation, a low phase detector frequency must be avoided. See “Guidelines Using LOL” on pg. 6 for information regarding the phase detector frequency.

### HS/PBO Triggers

The HS function (or the combined HS/PBO function) is armed after the device locks to the input clock reference. Once armed, HS is triggered by the occurrence of a Loss of Lock condition. This would typically occur as a consequence of a clock reference failure, a clock failure upstream to the M1025/26, or a M1025/26 clock reference mux reselection.

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*When pin AUTO = 1 (automatic reference reselection mode) HS is used in conjunction with input reselection. When AUTO = 0 (manual mode), HS will still occur upon an input phase transient, however the clock input is not reselected (this enables hitless switching when using an external MUX for clock selection).*

---

### HS/PBO Operation

Once triggered, the following HS/PBO sequence occurs:

1. The HS function disables the PLL Phase Detector and puts the device into NBW (narrow bandwidth) mode. The internal resistor  $R_{in}$  is changed to 2100k $\Omega$ . See the Narrow Bandwidth (NBW) Control Pin on pg. 8.
2. If included, the PBO function adds to (builds out) the phase in the clock feedback path (in VCSO clock cycle increments) to align the feedback clock with the (new) reference clock input phase.
3. The PLL Phase Detector is enabled, allowing the PLL to re-lock.
4. Once the PLL Phase Detector feedback and input clocks are locked to within 2 ns for eight consecutive cycles, a timer (WBW timer) for resuming wide bandwidth (in 175 ns) is started.
5. When the WBW timer times out, the device reverts to wide loop bandwidth mode (*i.e.*,  $R_{in}$  is returned to 100k $\Omega$ ) and the HS/PBO function is re-armed.

### Narrow Bandwidth (NBW) Control Pin

A Narrow Loop Bandwidth control pin (NBW pin) is included to adjust the PLL loop bandwidth. In wide bandwidth mode (NBW=0), the internal resistor  $R_{in}$  is 100k $\Omega$ . With the NBW pin asserted, the internal resistor  $R_{in}$  is changed to 2100k $\Omega$ . This lowers the loop bandwidth by a factor of about 21 (approximately 2100 / 100) and lowers the damping factor by a factor of about 4.6 (the square root of 21), assuming the same loop filter components.



### External Loop Filter

To provide stable PLL operation, the M1025/26 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

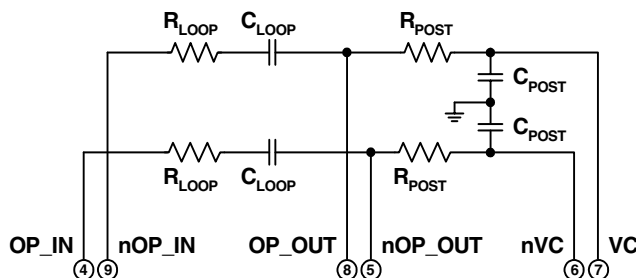


Figure 5: External Loop Filter

See Table 7, Example External Loop Filter Component Values, below.

PLL Bandwidth is affected by loop filter component values, the “M” value, and the “PLL Loop Constants” listed in AC Characteristics on pg. 12.

The MR\_SEL3:0 settings can be used to actively change PLL loop bandwidth in a given application. See “M and R Divider Look-Up Tables (LUT)” on pg. 3.

### Example External Loop Filter Component Values<sup>1</sup> for M1025-yz-155.5200 and M1026-yz-155.5200

VCSO Parameters:  $K_{VCO} = 200\text{kHz/V}$ ,  $R_{IN} = 100\text{k}\Omega$  (pin NBW = 0), VCSO Bandwidth = 700kHz.

$F_{REF}$ (MHz)	Device Configuration					Example External Loop Filter Comp. Values				Nominal Performance Using These Values		
	$F_{VCSO}$ (MHz)	MR_SEL3:0	MDiv	NBW		$R_{LOOP}$	$C_{LOOP}$	$R_{POST}$	$C_{POST}$	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
19.44 <sup>2</sup>	155.52	0 0 0 0	8	0		6.8k $\Omega$	10 $\mu$ F	82k $\Omega$	1000pF	315Hz	5.4	0.068
38.88 <sup>3</sup>	155.52	0 0 0 1	16	0		12k $\Omega$	10 $\mu$ F	82k $\Omega$	1000pF	270Hz	6.7	0.044
77.76 <sup>4</sup>	155.52	0 1 0 1	8	0		6.8k $\Omega$	10 $\mu$ F	82k $\Omega$	1000pF	315Hz	5.4	0.068
77.76 <sup>5</sup>	155.52	0 1 1 0	32	0		22k $\Omega$	4.7 $\mu$ F	82k $\Omega$	1000pF	250Hz	6.0	0.05
155.52 <sup>4</sup>	155.52	1 0 1 0	16	0		12k $\Omega$	10 $\mu$ F	82k $\Omega$	1000pF	270Hz	6.7	0.044
155.52 <sup>5</sup>	155.52	1 0 1 1	64	0		47k $\Omega$	2.2 $\mu$ F	82k $\Omega$	1000pF	266Hz	6.2	0.05

Table 7: Example External Loop Filter Component Values

Note 1:  $K_{VCO}$ , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to [www.icst.com](http://www.icst.com).

Note 2: This row is for the M1025 only.

Note 3: This row is for the M1026 only.

Note 4: Optimal for system clock filtering.

Note 5: Optimal for loop timing mode (LOL, AutoSwitch, or Hitless Switching should not be used).

### PLL Simulator Tool Available

A free PC software utility is available on the ICS website ([www.icst.com](http://www.icst.com)). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

For guidance on device or loop filter implementation, contact CMBU (Commercial Business Unit) Product Applications at (508) 852-5400.



## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Symbol	Parameter	Rating	Unit
V <sub>I</sub>	Inputs	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>O</sub>	Outputs	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>CC</sub>	Power Supply Voltage	4.6	V
T <sub>S</sub>	Storage Temperature	-45 to +100	°C

Table 8: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Positive Supply Voltage	3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Operating Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	°C

Table 9: Recommended Conditions of Operation



## ELECTRICAL SPECIFICATIONS

### DC Characteristics

Unless stated otherwise,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$  (commercial),  $T_A = -40^\circ C$  to  $+85^\circ C$  (industrial),  $F_{VCSO} = F_{OUT} = 150-175MHz$ , LVPECL outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V	
	$I_{CC}$	Power Supply Current			175	225	mA	
All Differential Inputs	$V_{P-P}$	Peak to Peak Input Voltage		0.15			V	
	$V_{CMR}$	Common Mode Input	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.5		$V_{CC} - .85$	V	
	$C_{IN}$	Input Capacitance				4	pF	
Differential Inputs with Pull-down	$I_{IH}$	Input High Current (Pull-down)				150	$\mu A$	$V_{CC} = V_{IN} = 3.456V$
	$I_{IL}$	Input Low Current (Pull-down)	DIF_REF0, DIF_REF1	-5			$\mu A$	
	$R_{pulldown}$	Internal Pull-down Resistance			50		k $\Omega$	
Differential Inputs Biased to VCC/2	$I_{IH}$	Input High Current (Biased)				150	$\mu A$	$V_{IN} = 0$ to $3.456V$
	$I_{IL}$	Input Low Current (Biased)	nDIF_REF0, nDIF_REF1	-150			$\mu A$	
	$R_{bias}$	Biased to Vcc/2			See Figure 4			
All LVCMOS / LVTTTL Inputs	$V_{IH}$	Input High Voltage	AUTO, REF_SEL, MR_SEL3, MR_SEL2, MR_SEL1, MR_SEL0, P_SEL1, P_SEL0, NBW	2		$V_{CC} + 0.3$	V	
	$V_{IL}$	Input Low Voltage		-0.3		0.8	V	
	$C_{IN}$	Input Capacitance				4	pF	
LVCMOS / LVTTTL Inputs with Pull-down	$I_{IH}$	Input High Current (Pull-down)	AUTO, REF_SEL, MR_SEL3, MR_SEL2, MR_SEL1, MR_SEL0, P_SEL1, P_SEL0			150	$\mu A$	$V_{CC} = V_{IN} = 3.456V$
	$I_{IL}$	Input Low Current (Pull-down)		-5			$\mu A$	
	$R_{pulldown}$	Internal Pull-down Resistance			50		k $\Omega$	
LVCMOS / LVTTTL Inputs with Pull-UP	$I_{IH}$	Input High Current (Pull-UP)				5	$\mu A$	$V_{CC} = 3.456V$ $V_{IN} = 0V$
	$I_{IL}$	Input Low Current (Pull-UP)	NBW	-150			$\mu A$	
	$R_{pullup}$	Internal Pull-UP Resistance			50		k $\Omega$	
Differential Outputs	$V_{OH}$	Output High Voltage		$V_{CC} - 1.4$		$V_{CC} - 1.0$	V	
	$V_{OL}$	Output Low Voltage	FOUT, nFOUT	$V_{CC} - 2.0$		$V_{CC} - 1.7$	V	
	$V_{P-P}$	Peak to Peak Output Voltage <sup>1</sup>		0.4		0.85	V	
LVCMOS Output	$V_{OH}$	Output High Voltage	LOL, REF_ACK	2.4		$V_{CC}$	V	$I_{OH} = 1mA$
	$V_{OL}$	Output Low Voltage		GND		0.4	V	$I_{OL} = 1mA$

Note 1: Single-ended measurement. See Figure 6, Output Rise and Fall Time, on pg. 12.

Table 10: DC Characteristics



## ELECTRICAL SPECIFICATIONS (CONTINUED)

### AC Characteristics

Unless stated otherwise,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$  (commercial),  $T_A = -40^\circ C$  to  $+85^\circ C$  (industrial),  $F_{VCSO} = F_{OUT} = 150\text{-}175\text{MHz}$ , LVPECL outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
$F_{IN}$	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	15		700	MHz	
$F_{OUT}$	Output Frequency	FOUT, nFOUT	62.5		175	MHz	
APR	Absolute Pull-Range of VCSO	Commercial	$\pm 120$	$\pm 200$		ppm	
		Industrial	$\pm 50$	$\pm 150$		ppm	
$K_{VCO}$	VCO Gain			200		kHz/V	
PLL Loop Constants <sup>1</sup>	$R_{IN}$	Wide Bandwidth		100		k $\Omega$	
		Narrow Bandwidth		2100		k $\Omega$	
$BW_{VCSO}$	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	$\Phi_n$	Single Side Band Phase Noise @ 155.52MHz	1kHz Offset	-83		dBc/Hz	$F_{in}=19.44$ or $38.88$ MHz Tot. PLL ratio = 8 or 4. See pg. 3
		10kHz Offset	-113		dBc/Hz		
		100kHz Offset	-136		dBc/Hz		
$J(t)$	Jitter (rms) @ 155.52MHz	12kHz to 20MHz		0.4	0.6	ps	
odc	Output Duty Cycle <sup>2</sup>		45	50	55	%	
$t_R$	Output Rise Time <sup>2</sup> for FOUT, nFOUT		350	450	550	ps	20% to 80%
$t_F$	Output Fall Time <sup>2</sup> for FOUT, nFOUT		350	450	550	ps	20% to 80%

Table 11: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 7, Example External Loop Filter Component Values, on pg. 9.

Note 2: See Parameter Measurement Information on pg. 12.

## PARAMETER MEASUREMENT INFORMATION

### Output Rise and Fall Time

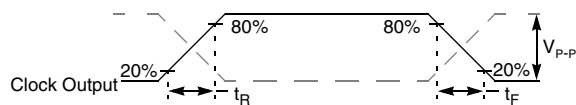


Figure 6: Output Rise and Fall Time

### Output Duty Cycle

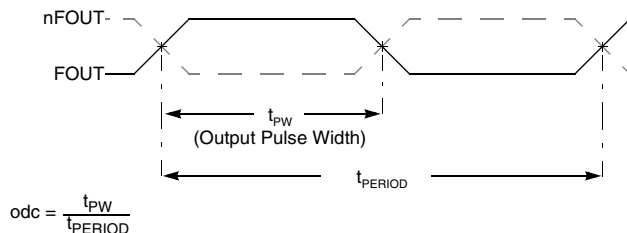
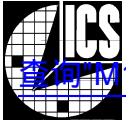
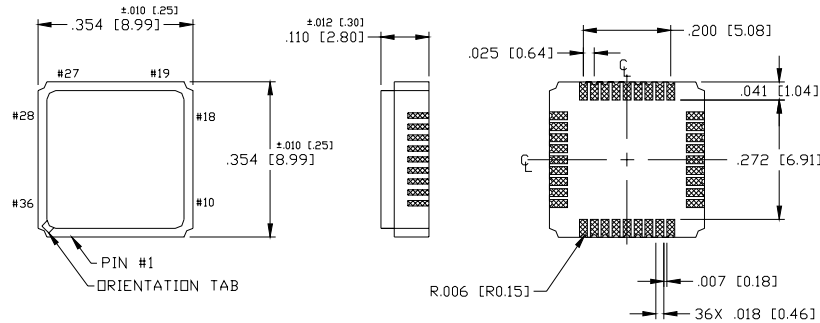


Figure 7: Output Duty Cycle



**DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER**

**Mechanical Dimensions:**



Refer to the SAW PLL application notes web page at [www.icst.com/products/appnotes/SawPLLAppNotes.htm](http://www.icst.com/products/appnotes/SawPLLAppNotes.htm) for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE  $\pm .005$  [0.13]

**Figure 8: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier**





**ORDERING INFORMATION**

**Part Numbering Scheme**

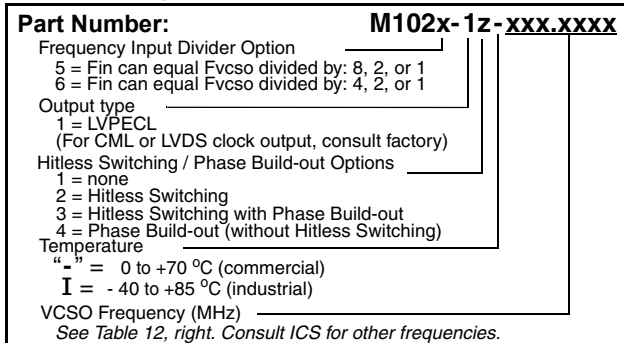


Figure 9: Part Numbering Scheme

Consult ICS for the availability of other VCSO frequencies.

Note \*: Fout can equal Fvcs0 divided by: 1 or 2

**Standard VCSO Output Frequencies (MHz)\***

125.0000	167.3280
155.5200	167.3316
156.2500	167.7097
156.8324	168.0400
161.1328	172.6423
166.6286	173.3708
167.2820	

Table 12: Standard VCSO Output Frequencies (MHz)

**Example Part Numbers**

VCSO Frequency (MHz)	Temperature	Order Part Number (Examples)
155.52	commercial	<b>M1025-11-155.5200</b> or <b>M1026-11-155.5200</b>
	industrial	<b>M1025-11I155.5200</b> or <b>M1026-11I155.5200</b>
156.25	commercial	<b>M1025-11-156.2500</b> or <b>M1026-11-156.2500</b>
	industrial	<b>M1025-11I156.2500</b> or <b>M1026-11I156.2500</b>

Table 13: Example Part Numbers

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