

Product Specification

PE4232

Product Description

The PE4232 is a high-isolation Switch designed for CATV applications, covering a broad frequency range from near DC up to 1300 MHz. This single-supply SPST switch offers a single-pin CMOS control interface with industry leading CTB performance. It also provides low insertion loss, high isolation and extremely low bias requirements while operating on a single 3-volt supply. In a typical CATV application, the PE4232 provides for a cost effective and manufacturable solution vs. mechanical relays.

The PE4232 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

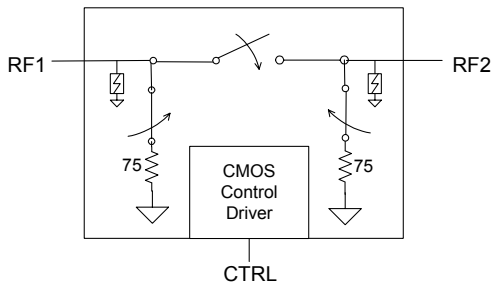


Table 1. Electrical Specifications @ +25 °C ($Z_S = Z_L = 75 \Omega$)

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency ¹		DC		1300	MHz
Operating Power	On / Off			30/24	dBm
Insertion Loss	DC – 50 MHz 1000 MHz		0.5 0.75	0.65 1.0	dB
Isolation	DC – 50 MHz 1000 MHz	75 50	90 53		dB
Return Loss	5 - 1000 MHz	14	20		dB
Input 1 dB Compression ^{2,4}	1000 MHz	30	33		dBm
CTB / CSO	77 & 110 channels; PO = 44 dBmV		-100		dBc
Input IP2 ²	1000 MHz	80			dBm
Input IP3 ²	1000 MHz	50			dBm
Video Feedthrough ³				15	mV _{pp}
Switching Time			2		μs

Notes: 1. Device linearity will begin to degrade below 1 MHz.

2. Measured in a 50 Ω system.

3. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.

4. Note Absolute Maximum ratings in Table 3.

SPST CATV UltraCMOS™ Switch

Features

- Non-reflective 75 Ω switch
- Integrated 0.25 watt terminations
- CTB performance of 100 dBc
- High isolation: 90 dB at 5 MHz, 53 dB at 1000 MHz
- Low insertion loss: 0.5 dB at 5 MHz, 0.75 dB at 1000 MHz
- High input IP2: 80 dBm
- CMOS/TTL single-pin control
- Single +3-volt supply operation
- Extremely low bias: 33 μ A @ 3 V

Figure 2. Package Type

6-lead DFN



Figure 3. Pin Configuration

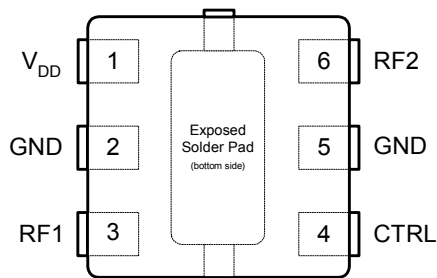


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V _{DD}	Nominal 3 V supply connection.
2	GND	Ground connection. ²
3	RF1	RF port. ¹
4	CTRL	CMOS or TTL logic level: High = RF1 to RF2 signal path Low = RF1 isolated from RF2
5	GND	Ground connection. ²
6	RF2	RF port. ¹

Notes: 1. Both RF pins must be held at 0 V_{DC} or require external DC blocking capacitors
2. The exposed pad must be soldered to the ground plane for proper switch performance.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on CTRL input	-0.3	5.5	V
T _{ST}	Storage temperature	-65	150	°C
T _{OP}	Operating temperature	-40	85	°C
P _{IN}	Input power (50 Ω), CTRL=1/CTRL=0		33/24	dBm
V _{ESD}	ESD voltage (Human Body Model)		200	V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Unit
V _{DD} Power Supply	2.7	3.0	3.3	V
I _{DD} Power Supply Current (V _{DD} = 3V, V _{CTRL} = 3V)		33	40	μA
Control Voltage High	0.7xV _{DD}		5	V
Control Voltage Low	0		0.3xV _{DD}	V

Table 5. Control Logic Truth Table

Control Voltage (CTRL)	Signal Path (RF1 to RF2)
High ¹	ON
Low	OFF

Notes: 1. CTRL accepts both CMOS and TTL voltage levels.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Description

The PE4232 high isolation SPST CATV Switch is designed to support CATV applications such as premise disconnect of a CATV signal path. This function is typically performed by bulky and expensive mechanical switches. The high isolation characteristics, high compression point, and integrated 75-ohm terminations make the PE4232 an ideal, cost effective and manufacturable product of choice.

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Typical Performance Data @ 25°C (Unless Otherwise Noted)
(75-ohm impedance except as indicated)

Figure 4.
T = -40 °C to 85 °C

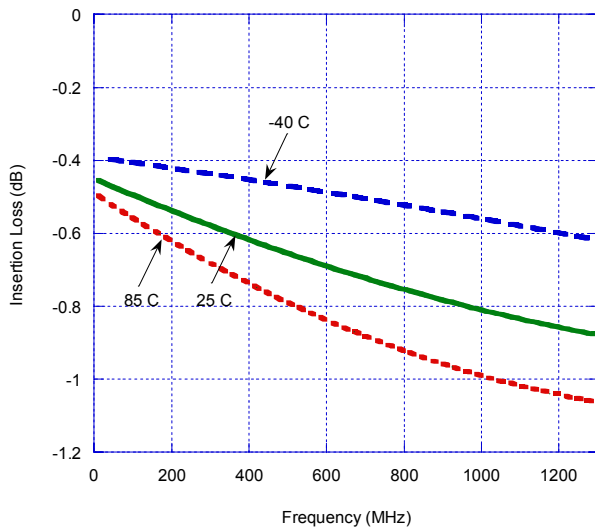


Figure 5. Input 1 dB Compression Point & IIP3
(50-ohm system impedance)

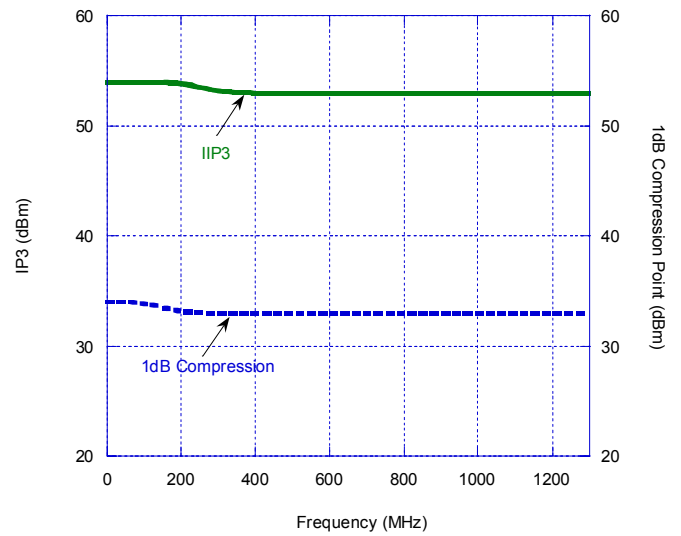
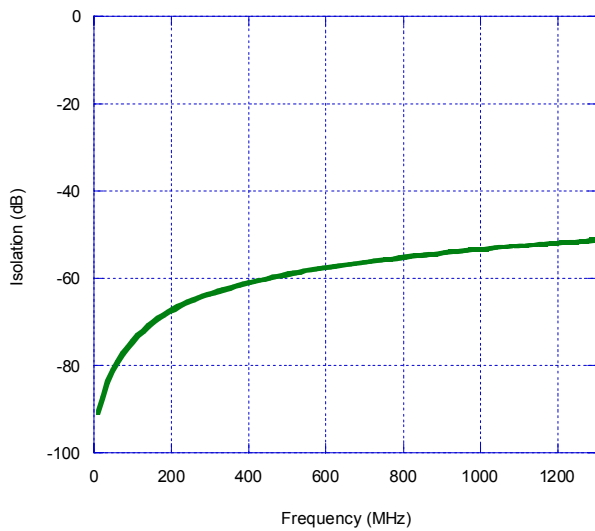


Figure 6. Isolation



Typical Performance Data @ 25 °C
(75-ohm impedance)

Figure 7. RF1 Return Loss (Switch = ON)

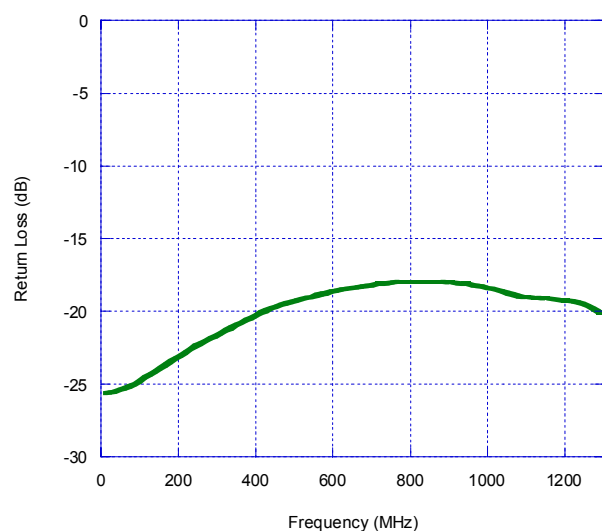


Figure 8. RF1 Return Loss (Switch = OFF)

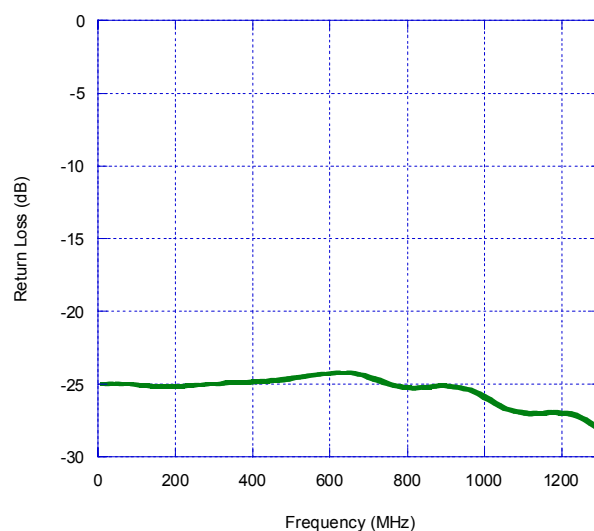


Figure 9. RF2 Return Loss (Switch = ON)

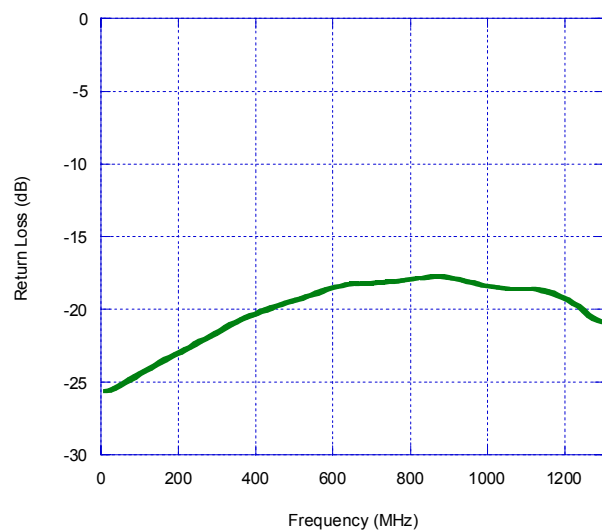
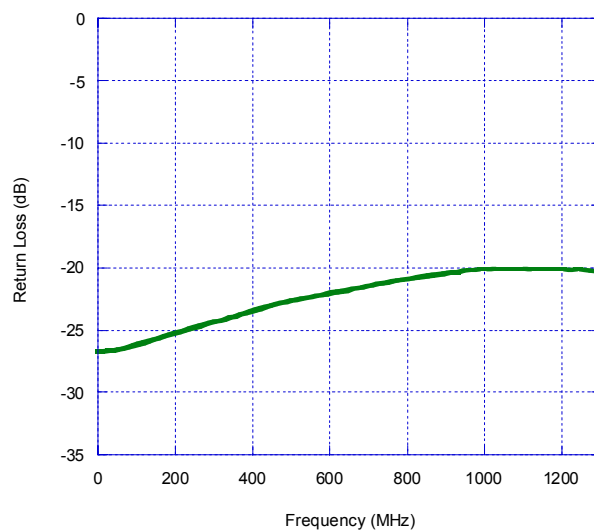


Figure 10. RF2 Return Loss (Switch = OFF)



Evaluation Kit

The SPST Switch Evaluation Kit board was designed to ease customer evaluation of the PE4232 SPST switch. The RF1 port is connected through a 75 Ω transmission line to the top left BNC connector, J1. The RF2 port is connected through a 75 Ω transmission line to the BNC connector on the top right side of the board, J2. A through transmission line connects BNC connectors J3 and J4. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide model with trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ϵ_R of 4.3. Note that the predominate mode for these transmission lines is coplanar waveguide with a ground plane.

J5 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J5-3) is connected to the device V_{DD} input. The fourth pin to the right (J5-7) is connected to the device CTRL input. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 11. Evaluation Board Layouts

Peregrine Specification 101/0079

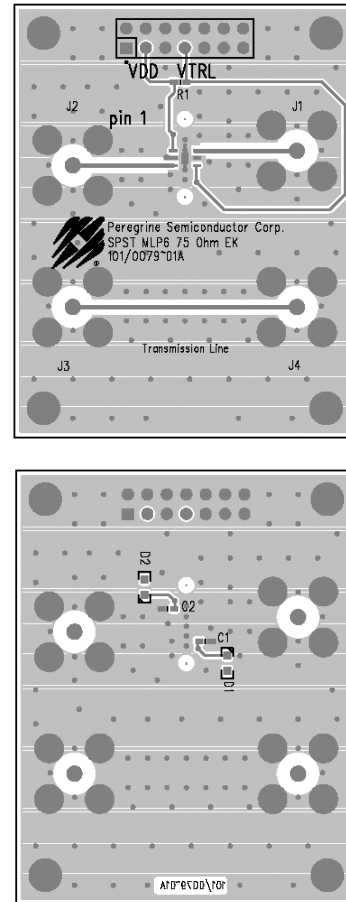


Figure 12. Evaluation Board Schematic

Peregrine Specification 102/0081

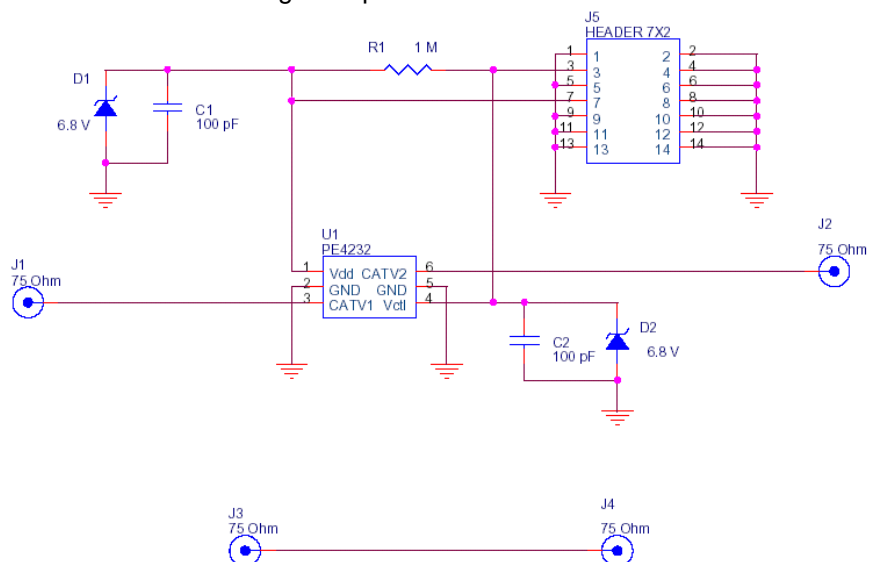
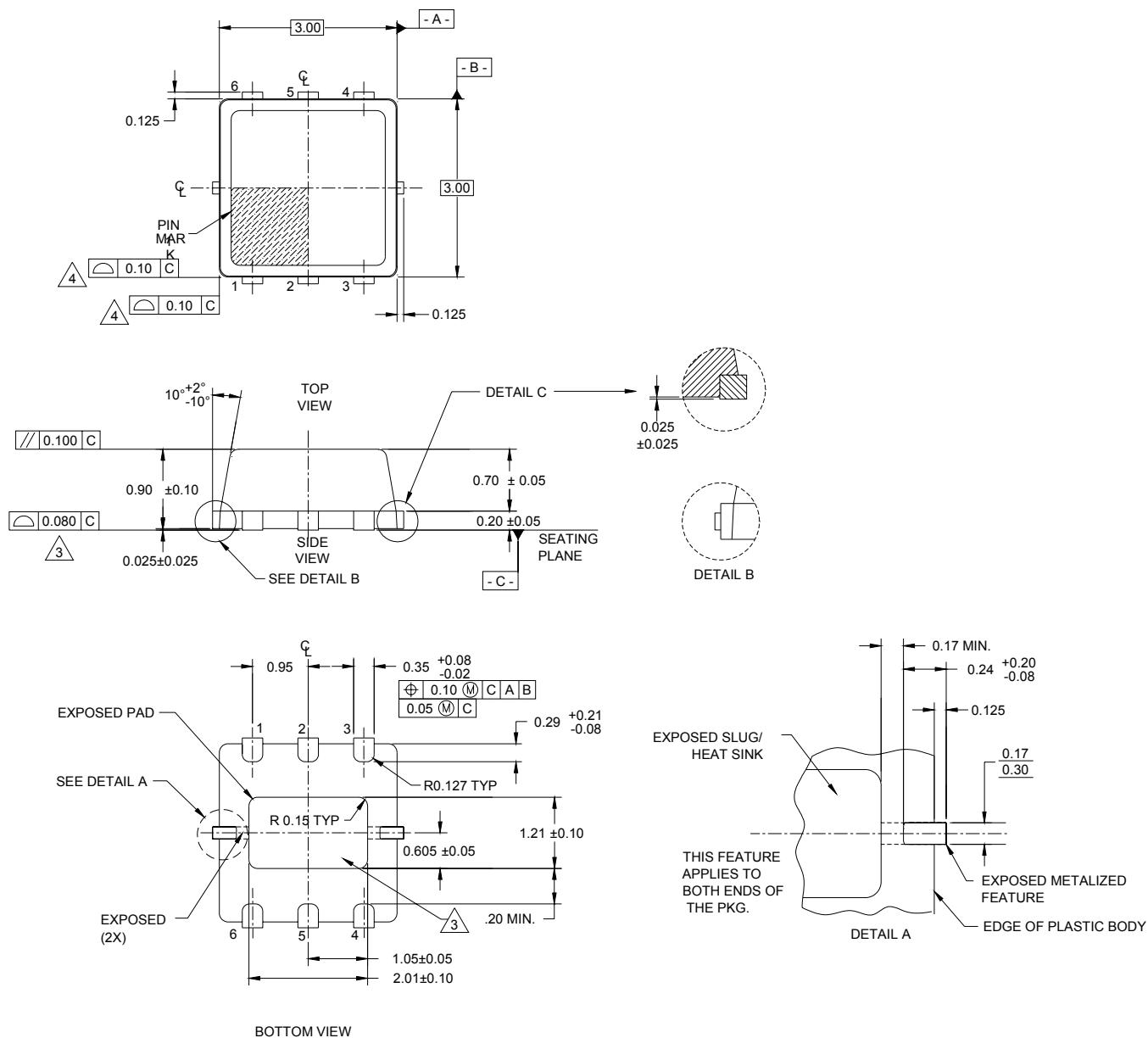


Figure 13. Package Drawing

6-lead DFN



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