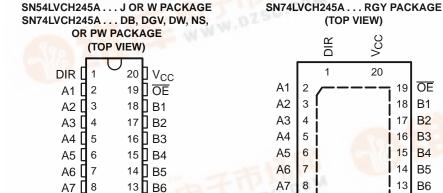


旬**ツミヤツ/ダイタº♡**CH245A-SP"供应商

FEATURES

- Inputs Accept Voltages to 5.5 V
- Max t_{nd} of 6.3 ns at 3.3 V
- Typical Volp (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With $3.3-V V_{CC}$

- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

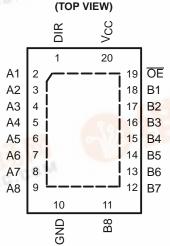


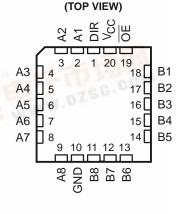
12

B7 11 **B8**

Α8 9

GND





SN54LVCH245A...FK PACKAGE

DESCRIPTION/ORDERING INFORMATION

The SN54LVCH245A octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation, SN74LVCH245A octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

These devices are fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by OE or DIR. WWW.DZSC.COM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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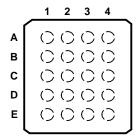


ORDERING INFORMATION

T _A	PACKAG	E ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Reel of 1000	SN74LVCH245ARGYR	LCH245A
	SOIC - DW	Tube of 25	SN74LVCH245ADW	LVCH245A
	301C - DVV	Reel of 2000	SN74LVCH245ADWR	LVCH245A
–40°C to 85°C	SOP - NS	Reel of 2000	SN74LVCH245ANSR	LVCH245A
	SSOP - DB	Reel of 2000	SN74LVCH245ADBR	LCH245A
		Tube of 70	SN74LVCH245APW	
	TSSOP - PW	Reel of 2000	SN74LVCH245APWR	LCH245A
		Reel of 250	SN74LVCH245APWT	
	TVSOP - DGV	Reel of 2000	SN74LVCH245ADGVR	LCH245A
	VFBGA – GQN	Dool of 1000	SN74LVCH245AGQNR	I CLIDAEA
	VFBGA – ZQN (Pb-free)	Reel of 1000	SN74LVCH245AZQNR	LCH245A
	CDIP – J	Tube of 20	SNJ54LVCH245AJ	SNJ54LVCH245AJ
–55°C to 125°C	CFP – W	Tube of 85	SNJ54LVCH245AW	SNJ54LVCH245AW
	LCCC – FK	Tube of 55	SNJ54LVCH245AFK	SNJ54LVCH245AFK

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GQN OR ZQN PACKAGE (TOP VIEW)



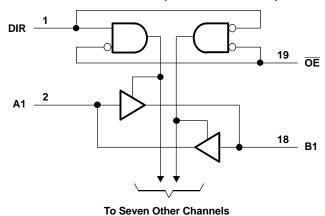
TERMINAL ASSIGNMENTS

	1	2	3	4
Α	A1	DIR	V _{CC}	<u>OE</u>
В	А3	B2	A2	B1
С	A5	A4	B4	В3
D	A7	В6	A6	B5
E	GND	A8	B8	B7

FUNCTION TABLE

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_{I}	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the	high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the	high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current				
	Continuous current through V _{CC} or GND		±100	mA	
		DB package (4)		70	
		DGV package ⁽⁴⁾		92	
		DW package ⁽⁴⁾		58	
θ_{JA}	Package thermal impedance	GQN/ZQN package ⁽⁴⁾		78	°C/W
		NS package ⁽⁴⁾		60	
		PW package ⁽⁴⁾		83	
		RGY package ⁽⁵⁾		37	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

⁽⁵⁾ The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LVCH245A, SN74LVCH245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS





Recommended Operating Conditions⁽¹⁾

			SN54LVC	H245A	SN74LV	SN74LVCH245A		
			MIN	MAX	MIN	MAX	UNIT	
V	Cumply voltage	Operating	2	3.6	1.65	3.6	V	
V_{CC}	Supply voltage	Data retention only	1.5		1.5		V	
		V _{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		2			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$				$0.35 \times V_{CC}$		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$				0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		8.0		0.8		
V _I	Input voltage		0	5.5	0	5.5	V	
\/	Output welfere	High or low state	0	V _{CC}	0	V _{CC}	V	
Vo	Output voltage	3-state	0	5.5	0	5.5	V	
		V _{CC} = 1.65 V				-4		
	High lovel output ourrent	$V_{CC} = 2.3 \text{ V}$				-8	mA	
I _{OH}	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12		-12	IIIA	
		V _{CC} = 3 V		-24		-24		
		V _{CC} = 1.65 V				4		
	Low lovel output current	$V_{CC} = 2.3 \text{ V}$				8	mA	
I _{OL}	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12		12	12	
		V _{CC} = 3 V		24		24		
Δt/Δν	Input transition rise or fall rate			10		10	ns/V	
T _A	Operating free-air temperature		-55	125	-40	85	°C	

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST SOMBITIONS	.,	SN54L	VCH245	iΑ	SN74	LVCH24	5A		
Ρ/	ARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	UNIT	
			1.65 V to 3.6 V				V _{CC} - 0.2				
		I _{OH} = -100 μA	2.7 V to 3.6 V	V _{CC} – 0.2							
V _{OH}		I _{OH} = -4 mA	1.65 V				1.2			V	
VOH		I _{OH} = -8 mA	2.3 V				1.7			·	
		10 4	2.7 V	2.2			2.2				
		$I_{OH} = -12 \text{ mA}$	3 V	2.4			2.4				
		I _{OH} = -24 mA	3 V	2.2			2.2				
		1. 100 1	1.65 V to 3.6 V						0.2		
		$I_{OL} = 100 \mu\text{A}$	2.7 V to 3.6 V			0.2					
.,		I _{OL} = 4 mA	1.65 V						0.45	.,	
V_{OL}		I _{OL} = 8 mA	2.3 V						0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4			0.4		
		I _{OL} = 24 mA	3 V			0.55			0.55		
I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5			±5	μΑ	
I _{off}		V_I or $V_O = 5.5 \text{ V}$	0						±10	μΑ	
		V _I = 0.58 V	4.05.1/				25				
		V _I = 1.07 V	1.65 V				-25				
		V _I = 0.7 V	0.01/				45				
I _{I(hold)}		V _I = 1.7 V	2.3 V				-45			μΑ	
,		V _I = 0.8 V	0.17	75			75				
		V _I = 2 V	3 V	-75			-75				
		V _I = 0 to 3.6 V ⁽²⁾	3.6 V			±500			±500		
$I_{OZ}^{(3)}$		$V_{O} = 0 \text{ V or } (V_{CC} \text{ to 5.5 V})$	2.3 V to 3.6 V			±15			±5	μΑ	
		$V_I = V_{CC}$ or GND	261/			10			10	^	
I _{CC}		$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(4)}$ $I_{\text{O}} = 0$	3.6 V			10			10	μΑ	
ΔI_{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500			500	μΑ	
Ci	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		4	12		4		pF	
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V		5.5	12		5.5		pF	

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. This is the bus-hold maximum dynamic current required to switch the input from one state to another.

For the total leakage current in an I/O port, please consult the $I_{I(hold)}$ specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions $V_I = 0$ V or $V_I = V_{CC}$ to 5.5 V. The bus-hold current, at input voltage greater than V_{CC} , is negligible.

This applies in the disabled state only.

SN54LVCH245A, SN74LVCH245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54L			
PARAMETER	FROM (INPUT)	TO (OUTPUT) $V_{CC} = 2.7 \text{ V}$		V _{CC} = 3 ± 0.3	V_{CC} = 3.3 V \pm 0.3 V	
			MIN MAX	MIN	MAX	
t _{pd}	A or B	B or A	8	1	7	ns
t _{en}	ŌE	A or B	9.5	1	8.5	ns
t _{dis}	ŌĒ	A or B	8.5	1	7.5	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN74LVCH245A								
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V \pm 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	(1)	(1)	(1)	(1)		7.3	1.5	6.3	ns
t _{en}	ŌĒ	A or B	(1)	(1)	(1)	(1)		9.5	1.5	8.5	ns
t _{dis}	ŌĒ	A or B	(1)	(1)	(1)	(1)		8.5	1.7	7.5	ns
t _{sk(o)}										1	ns

⁽¹⁾ This information was not available at the time of publication.

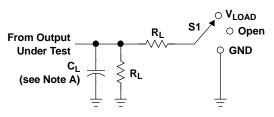
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
C	Power dissipation capacitance	Outputs enabled	f = 10 MHz	(1)	(1)	47	pF	
C _{pd}	per transceiver	Outputs disabled	I = IO WIHZ	(1)	(1)	2		

⁽¹⁾ This information was not available at the time of publication.

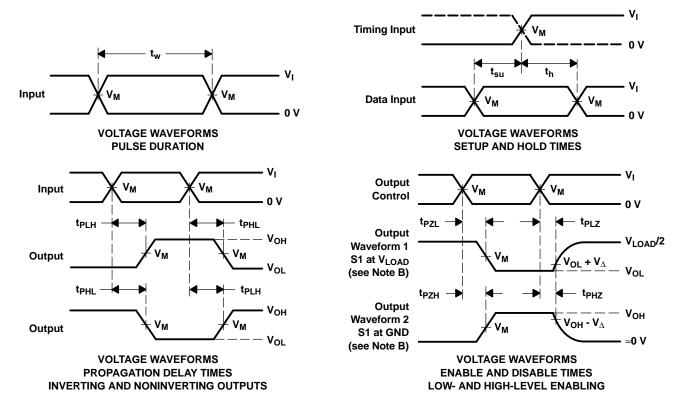
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INF	PUTS	.,	.,		_	.,
V _{CC}	V _I	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_{\Delta}$
1.8 V \pm 0.15 V	v _{cc}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time with, one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





22-Jan-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
5962-9754301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9754301QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9754301QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-9754301V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9754301VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9754301VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN74LVCH245ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LVCH245ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245AGQNR	NRND	BGA MI CROSTA R JUNI OR	GQN	20	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVCH245ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APW	ACTIVE	TSSOP	PW	20	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWE4	ACTIVE	TSSOP	PW	20	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWG4	ACTIVE	TSSOP	PW	20	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI





22-Jan-2010

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
SN74LVCH245APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCH245ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVCH245ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVCH245AZQNR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVCH245AZXYR	ACTIVE	BGA MI CROSTA R JUNI OR	ZXY	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SNJ54LVCH245AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LVCH245AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54LVCH245AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

查询"SN54LVCH245A-SP"供应商

22-Jan-2010

information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVCH245A, SN54LVCH245A-SP, SN74LVCH245A:

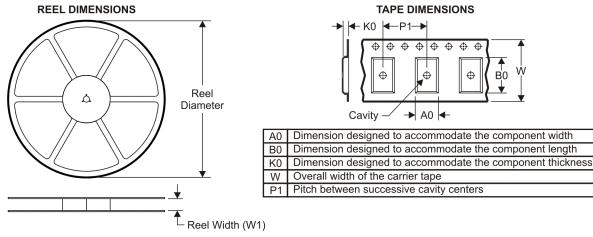
Automotive: SN74LVCH245A-Q1

NOTE: Qualified Version Definitions:

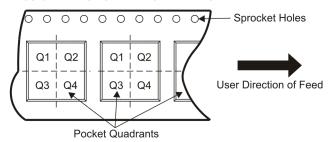
• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

6-Aug-2010

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

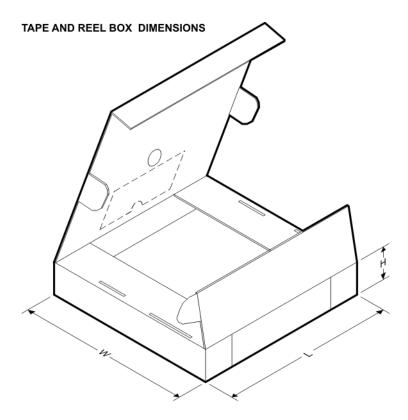
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCH245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVCH245AGQNR	BGA MI CROSTA R JUNI OR	GQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1
SN74LVCH245AGQNR	BGA MI CROSTA R JUNI OR	GQN	20	1000	330.0	12.4	3.3	4.3	1.5	8.0	12.0	Q1
SN74LVCH245ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVCH245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LVCH245AZQNR	BGA MI CROSTA R JUNI OR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.5	8.0	12.0	Q1
SN74LVCH245AZQNR	BGA MI CROSTA	ZQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1





6-Aug-2010

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	R JUNI OR											
SN74LVCH245AZXYR	BGA MI CROSTA R JUNI OR	ZXY	20	2500	330.0	12.4	2.8	3.3	1.0	4.0	12.0	Q2



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH245ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVCH245ADGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74LVCH245ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVCH245AGQNR	BGA MICROSTAR JUNIOR	GQN	20	1000	340.5	338.1	20.6
SN74LVCH245AGQNR	BGA MICROSTAR JUNIOR	GQN	20	1000	346.0	346.0	29.0
SN74LVCH245ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LVCH245APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74LVCH245APWT	TSSOP	PW	20	250	346.0	346.0	33.0
SN74LVCH245ARGYR	VQFN	RGY	20	3000	346.0	346.0	29.0
SN74LVCH245AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	346.0	346.0	29.0



PACKAGE MATERIALS INFORMATION

查询"SN54LVCH245A-SP"供应商

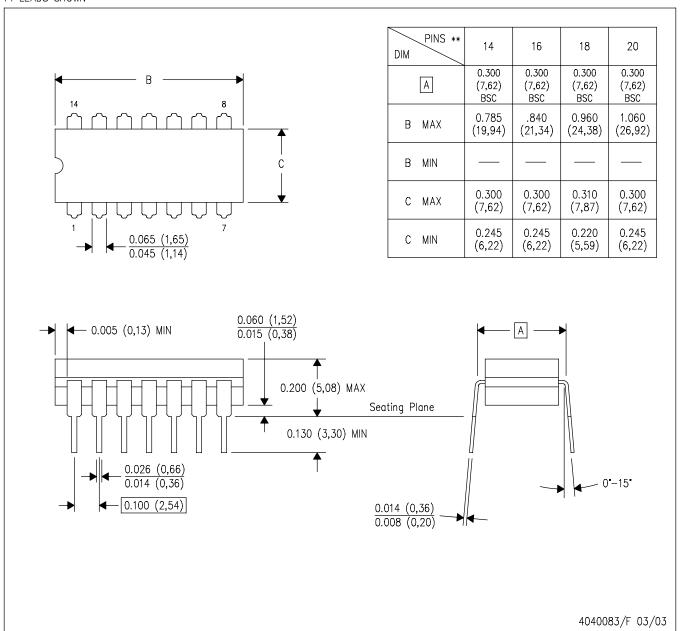
6-Aug-2010

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH245AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	340.5	338.1	20.6
SN74LVCH245AZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	340.5	338.1	20.6

J (R-GDIP-T**)

CERAMIC DUAL IN-LINE PACKAGE

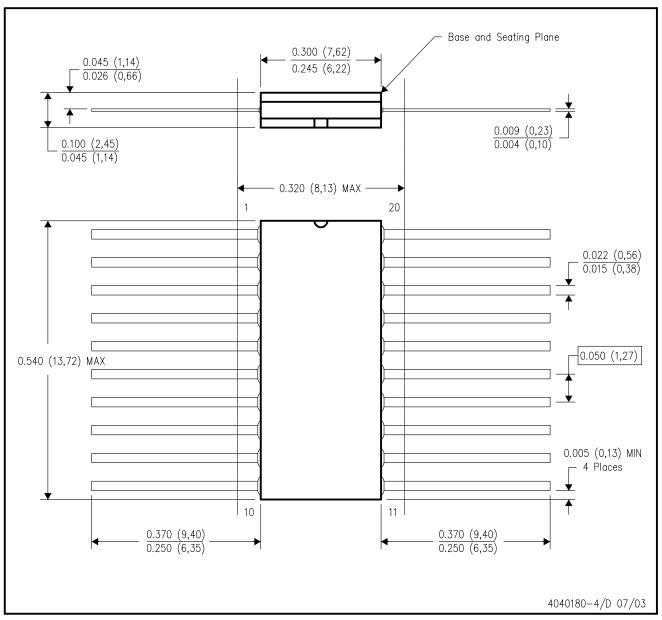
14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



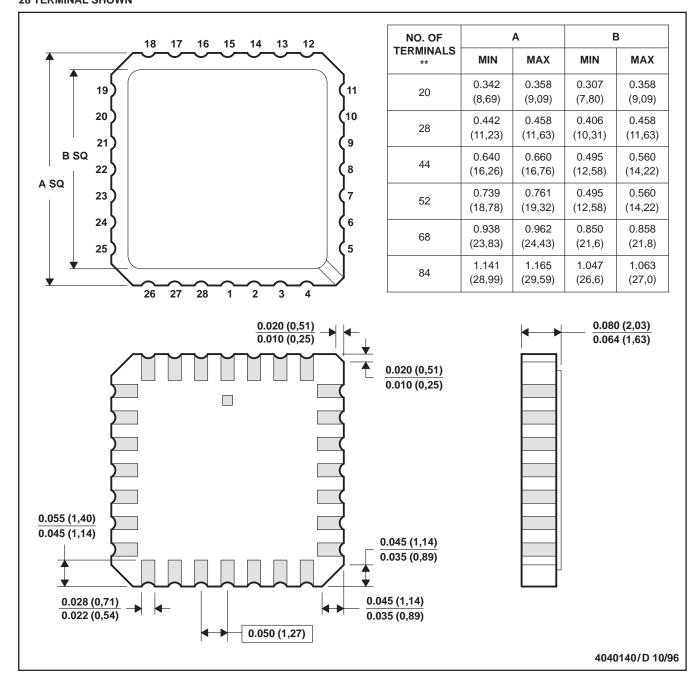
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



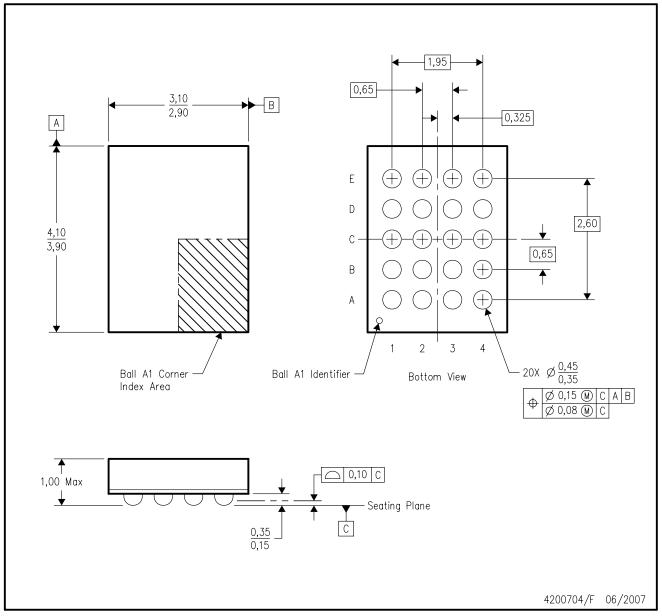
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



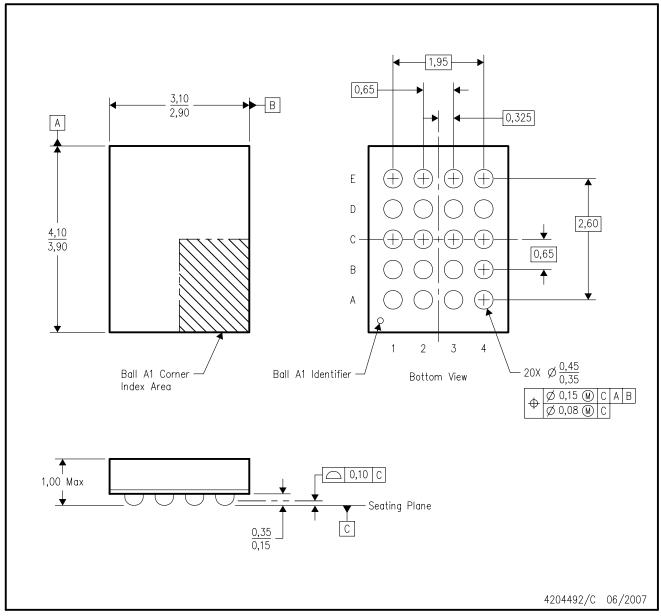
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BC-2.
- D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.



ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



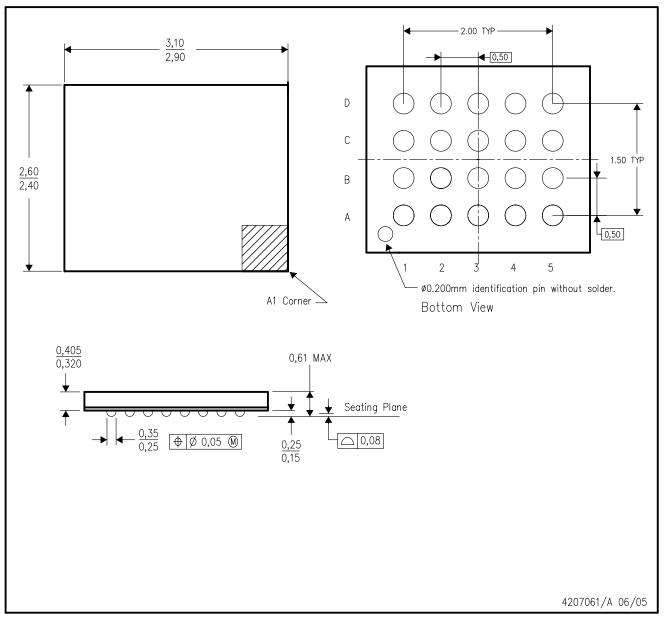
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BC-2.
- D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).



ZXY (S-PBGA-N20)

PLASTIC BALL GRID ARRAY



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is a lead-free solder ball design.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

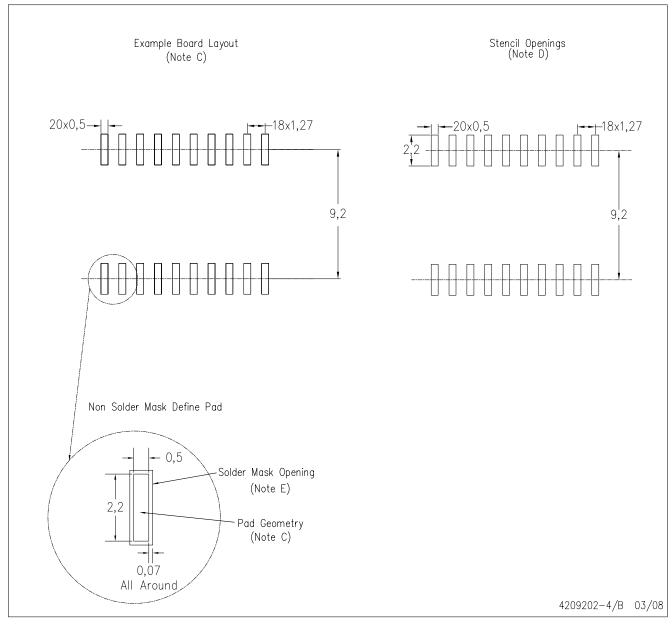
PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

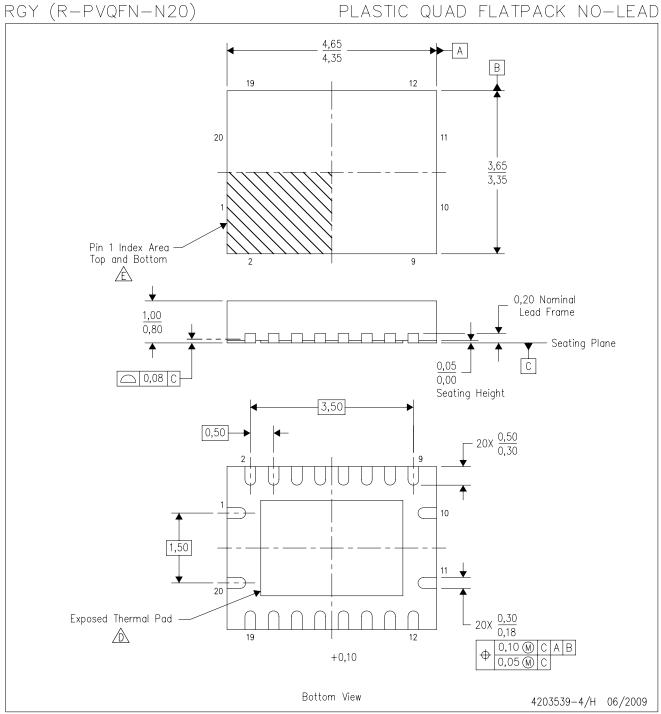


DW (R-PDSO-G20)



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.

 The Pin 1 identifiers are either a molded, marked, or metal feature.
- F. Package complies to JEDEC MO-241 variation BC.



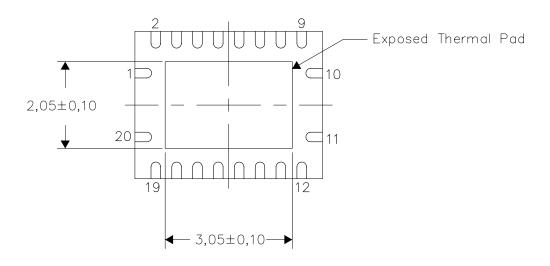
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



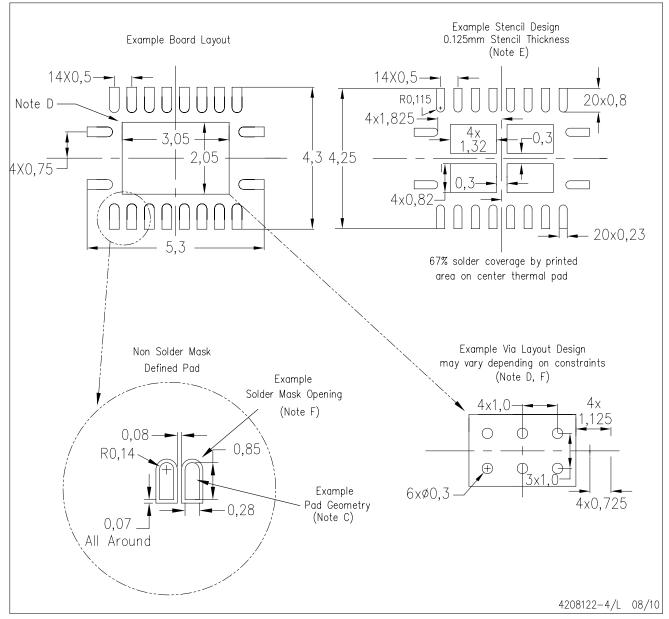
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

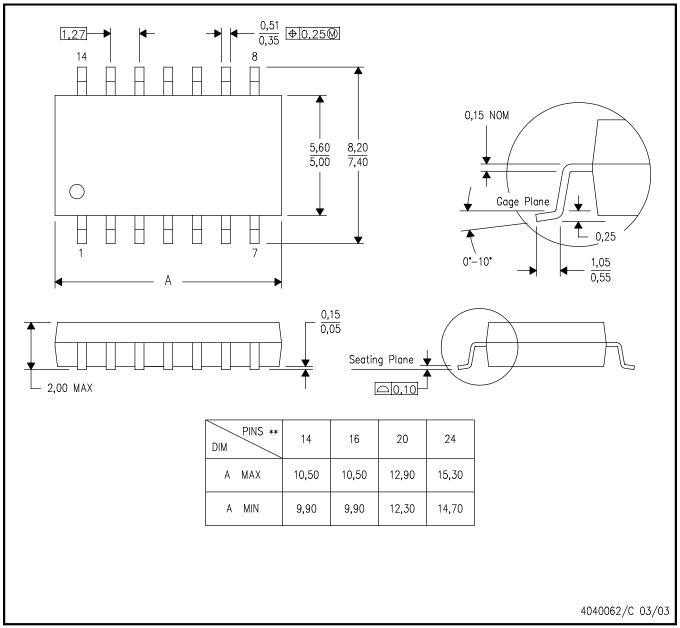


MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



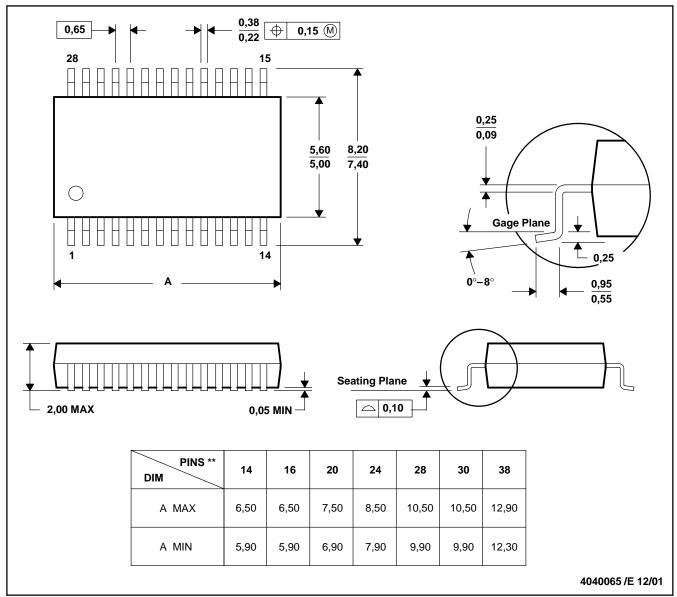
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

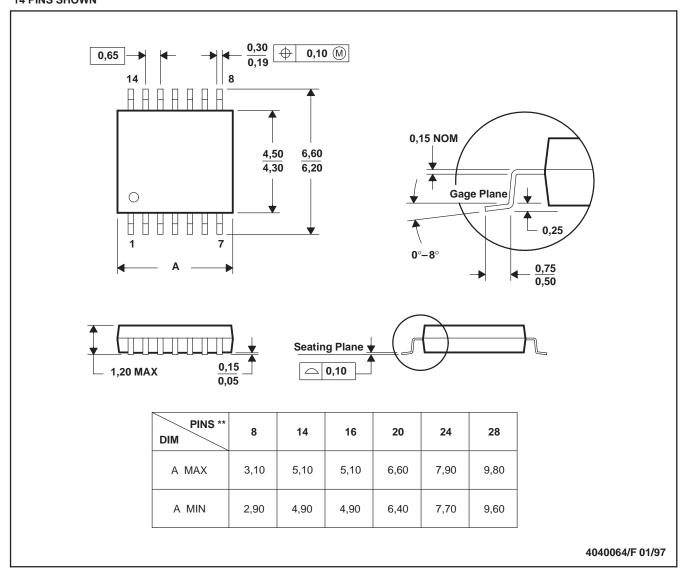
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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		Wireless	www.ti.com/wireless-apps