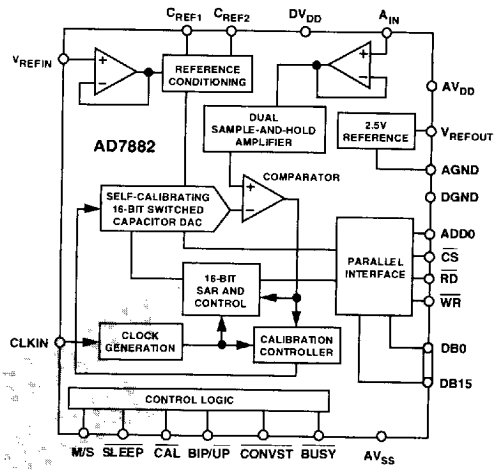
LC²MOS 16-Bit, 2.5 µs, Sampling ADC

AD7882

FEATURES
- 2.5 µs Throughput Time
- 16-Bit Sampling ADC
- Self-Calibration
- High Speed Parallel Interface
- 92 dB Signal-to-Noise Ratio
- Low Power: 200 mW typ
  - 1 mW in Power-Down Mode
- Unipolar and Bipolar Input Signal Ranges
- On-Chip 2.5 V Reference
- Operates from ±5 V Supplies

APPLICATIONS
- Data Acquisition Systems
- Digital Signal Processing
- Spectrum Analysis
- DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7882 is a fast, 16-bit self-calibrating A/D converter. It consists of a sample-and-hold amplifier, a self-calibrating 16-bit ADC, a 2.5 V reference and versatile interface logic. An on-chip controller manages the self-calibrating algorithm that reduces linearity, offset and gain errors to ±0.0015%. System offset and gain errors, caused by external conditioning circuitry, can also be included in the calibration procedure. Throughput time is minimized at 2.5 µs by the use of a dual sample-and-hold amplifier. The ADC also has a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time; alternatively, an external clock may be used.

Another feature of the AD7882 is a power-down mode that reduces power dissipation from its normal operating value of 200 mW to 1 mW.

The AD7882 operates from ±5 V supplies. Analog input ranges can be unipolar, 0 to 2.5 V or bipolar, ±2.5 V. The analog input bandwidth is 200 kHz.

In addition to traditional dc accuracy specifications such as linearity, the AD7882 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio (SNR).

The AD7882 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power high-speed CMOS logic. The part is available in a 44-pin plastic quad flatpack (PQFP) and 40-pin cerdip.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. Fast 2.5 µs Throughput Time
   A fast 2.5 µs throughput time makes the AD7882 suitable for a wide range of data acquisition applications.
2. Self-Calibration Achieves High Accuracy
   A self-calibrating algorithm minimizes linearity, offset and gain errors. The calibration procedure can also include external offset and gain errors.
3. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7882 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
4. Fast, Versatile Microprocessor Interface
   Fast bus access times and standard control signals make the AD7882 easy to interface to microprocessors.
5. Low Power
   Low power monolithic solution allows ease of application. The AD7882 also has a power down facility.

AD7882—SPECIFICATIONS (AV_{DD} = 5 V ± 5%, DV_{DD} = 5 V ± 5%, AV_{SS} = –5 V ± 5%, V_{REFIN} = 2.5 V, AGND = DGND = 0 V, f_{CLKIN} = 10 MHz, f_{SAMPLE} = 400 kHz. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	B, T Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal to (Noise + Distortion Ratio)	90	90	dB min	A_{IN} = 10 kHz, Typical SNR = 92 dB
	85	85	dB min	A_{IN} = 100 kHz, Typical SNR = 87 dB
THD	–95	–95	dB max	A_{IN} = 10 kHz, Typical THD = –100 dB
	–88	–88	dB max	A_{IN} = 100 kHz, Typical THD = –90 dB
Peak Harmonic or Spurious Noise	–98	–98	dB max	A_{IN} = 10 kHz, Typical Peak Harmonic = –100 dB
	–90	–90	dB max	A_{IN} = 100 kHz, Typical Peak Harmonic = –92 dB
Intermodulation Distortion (IMD)				
2nd Order Terms	–88	–88	dB max	f_A = 98 kHz, f_B = 100 kHz
3rd Order Terms	–88	–88	dB max	
Throughput Time	2.5	2.5	µs max	
Aperture Delay	10	10	ns typ	
Aperture Jitter	20	20	ps typ	
Noise	70	70	µV rms typ	
DC ACCURACY[2]				
Resolution	16	16	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	16	16	Bits	
Integral Nonlinearity	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1.0	LSB max	
Differential Nonlinearity	±0.9	±0.5	LSB max	
Unipolar Offset Error	±2	±2	LSB max	
Unipolar Gain Error	±2	±2	LSB max	
Bipolar Zero Error	±2	±2	LSB max	
Bipolar Positive Gain Error	±2	±2	LSB max	
Bipolar Negative Gain Error	±2	±2	LSB max	
POWER SUPPLY REJECTION				
AV_{DD} Only	84	84	dB typ	
AV_{SS} Only	84	84	dB typ	
ANALOG I/P				
Input Current	±1	±1	µA max	Input Range = 0 V to +2.5 V or ±2.5 V
Input Capacitance[3]	20	20	pF max	
REFERENCE OUTPUT				
V_{REFOUT} @ +25°C	2.5	2.5	Volts Nominal	±1%
V_{REFOUT} Tempco	20	20	ppm/°C typ	
REFERENCE INPUT				
V_{REFIN} Range	2.5	2.5	Volts	±2%
V_{REFIN} Current	±1	±1	µA max	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	Volts min	
Input Low Voltage, V_{INL}	0.8	0.8	Volts max	
Input Current	±10	±10	µA max	
Input Capacitance[3]	10	10	pF max	
$\overline{SLEEP}$ INPUT				
Input High Voltage, V_{INH}	V_{DD} – 0.2	V_{DD} – 0.2	Volts min	
Input Low Voltage, V_{INL}	0.2	0.2	Volts max	
CLKIN INPUT				
Negative Trigger Level	–2	–2	Volts min	This is the Trigger Level for Choosing Internal Clock Operation of the Device

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	A, S Versions[1]	B, T Versions[1]	Units	Test Conditions/Comments
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	2.4	2.4	Volts min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	Volts max	I_{SINK} = 1.6 mA
DB15–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[3]	20	20	pF max	
POWER REQUIREMENTS				
DV_{DD}	+5	+5	Volts	±5%
AV_{DD}	+5	+5	Volts	±5%
AV_{SS}	–5	–5	Volts	±5%
Normal Mode				
DI_{DD}	1	1	mA max	
AI_{DD}	29	29	mA max	
AI_{SS}	27	27	mA max	
Power Dissipation	300	300	mW max	Typically 200 mW, CLKIN not Running
Sleep Mode				
DI_{DD}	40	40	μA max	
AI_{DD}	50	50	μA max	
AI_{SS}	40	40	μA max	
Power Dissipation	1	1	mW max	Typically 500 μW, Input Logic Levels of 0.2 V and V_{DD} – 0.2 V, CLKIN Not Running. Typically 1.5 mW with CLKIN Running

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S, T Versions: –55°C to +125°C.
[2]Specifications apply after calibration.
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1]

(AV_{DD} = 5 V ± 5%, DV_{DD} = 5 V ± 5%, AV_{SS} = –5 V ± 5%, V_{REFIN} = 2.5 V, AGND = DGND = 0 V, f_{CLKIN} = 10 MHz, f_{SAMPLE} = 400 kHz. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit @ +25°C (All Versions)	Limit @ T_{MIN}, T_{MAX} (A, B Versions)	Limit @ T_{MIN}, T_{MAX} (S, T Versions)	Units	Conditions/Comments
t_1	10	15	20	ns min	ADD0 to $\overline{WR}$ Setup Time
t_2	5	5	10	ns min	ADD0 to $\overline{WR}$ Hold Time
t_3	10	15	20	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_4	5	5	10	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_5	30	40	50	ns min	$\overline{WR}$ Pulse Width
t_6	30	40	50	ns min	Data Setup Time
t_7	5	5	10	ns min	Data Hold Time
$t_{CONVERT}$	**22 t_{CLKIN}**	**22 t_{CLKIN}**	**22 t_{CLKIN}**		Conversion Time: Synchronous Operation
	2.3	**2.3**	**2.3**	µs max	Conversion Time: Internal Clock Operation
t_{SAMPLE}	**25 t_{CLKIN}**	**25 t_{CLKIN}**	**25 t_{CLKIN}**		Time Between Samples: Synchronous Operation
	2.6	**2.6**	**2.6**	µs max	Time Between Samples: Internal Clock Operation
t_8	30	40	50	ns min	$\overline{CONVST}$ Pulse Width
t_9	20	30	40	ns max	$\overline{CONVST}$ High to BUSY Low Delay
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{11}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{12}	40	50	60	ns min	$\overline{RD}$ Pulse Width
t_{13}[2]	40	50	60	ns max	$\overline{RD}$ Low to Data Valid Delay (Data Access Time)
t_{14}[3]	10	10	10	ns min	Data Hold Time After $\overline{RD}$ (Bus Relinquish Time)
	75	75	75	ns max	
t_{15}	10	15	20	ns min	ADD0 to $\overline{RD}$ Setup Time
t_{16}	5	5	10	ns min	ADD0 to $\overline{RD}$ Hold Time
t_{17}	40	40	50	ns min	New Data Valid before Rising Edge of $\overline{BUSY}$
t_{18}	20	30	40	ns max	CLKIN Falling Edge to $\overline{BUSY}$ Low Delay
t_{19}	10	20	30	ns min	$\overline{CS}$ to $\overline{CAL}$ Setup Time
t_{20}	0	0	0	ns min	$\overline{CS}$ to $\overline{CAL}$ Hold Time
t_{21}	30	40	50	ns min	$\overline{CAL}$ Pulse Width
t_{22}	20	30	40	ns max	$\overline{CAL}$ High to $\overline{BUSY}$ Low Delay
t_{23}	20	30	40	ns max	$\overline{CONVST}$ High to $\overline{BUSY}$ Low Delay: System CAL Mode
$t_{CAL\,1}$	9276744 t_{CLKIN}				Device Calibration Time: Device CAL Mode
$t_{CAL\,2}$	6359324 t_{CLKIN}				DAC Calibration Time: System CAL Mode
$t_{CAL\,3}$	1475104 t_{CLKIN}				Offset Calibration Time: System CAL Mode
$t_{CAL\,4}$	1442324 t_{CLKIN}				Gain Calibration Time: System CAL Mode

NOTES

[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_{13} is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_{14} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_{14}, quoted in the Timing Specifications is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice

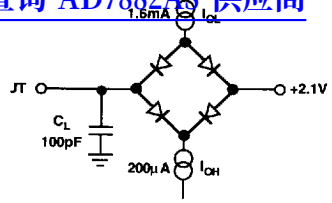


Figure 1. Load Circuit for Bus Access and Relinquish Time

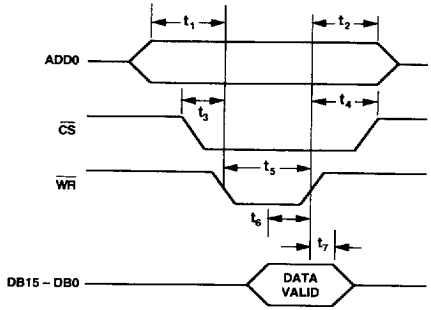


Figure 2. Write Timing Diagram

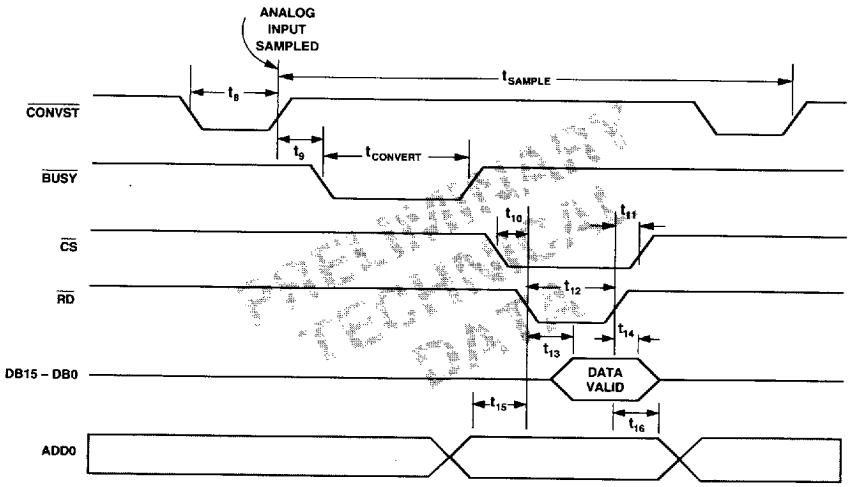


Figure 3. Read Timing Diagram, Asynchronous Operation (M/S = Low; $\overline{CAL}$ = High)

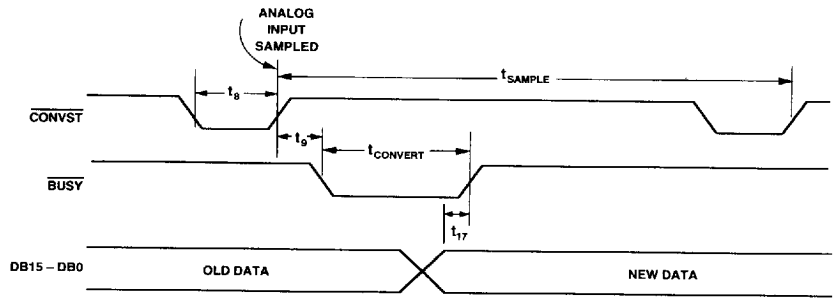


Figure 4. Read Timing Diagram, Asynchronous Operation (M/S, $\overline{CS}$, $\overline{RD}$, ADD0 = Low; $\overline{CAL}$ = High)

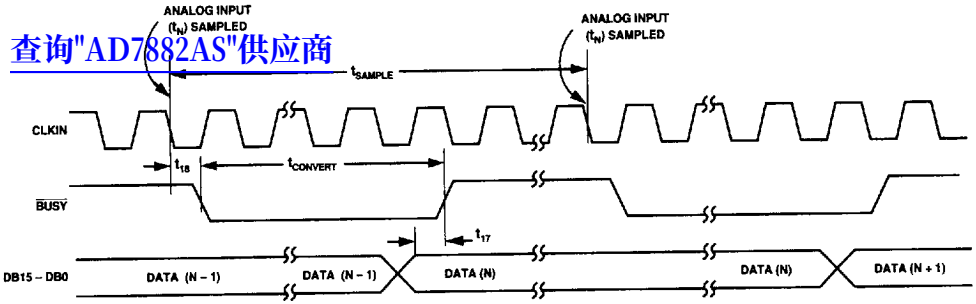


Figure 5. Read Timing Diagram, Synchronous Operation ($\overline{CS}$, $\overline{RD}$ = Low: M/S, $\overline{CAL}$ = High)

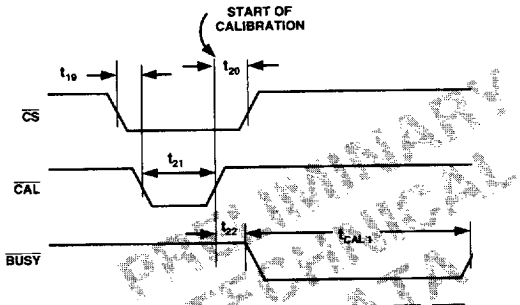


Figure 6. Device Calibration Timing (M/S = Low; $\overline{RD}$, $\overline{WR}$ = High)

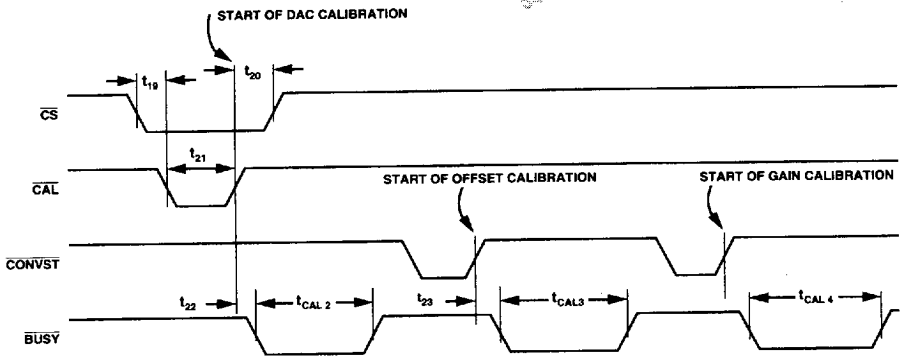


Figure 7. System Calibration Timing (M/S = High; $\overline{RD}$, $\overline{WR}$ = High)

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

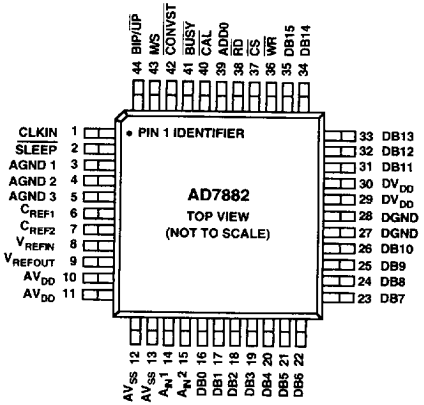
AV_{DD} to AGND . . . . . −0.3 V to +7 V
AV_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to +0.3 V
AV_{DD} to DV_{DD} . . . . . −0.3 V to +0.3 V
Analog Inputs to AGND . . . . . AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
Reference Inputs to AGND . . . AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
Digital Inputs to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial Plastic (A, B Versions) . . . . . −40°C to +85°C
Extended Hermetic (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range. . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Cerdip Package, Power Dissipation . . . . . 1000 mW
θ_{JA} Thermal Impedance . . . . . 50°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
PQFP Package, Power Dissipation . . . . . .875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES

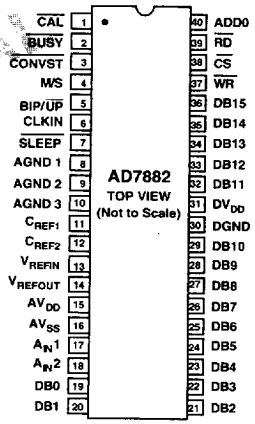
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PQFP Pinout



Cerdip Pinout



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7882 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
Power Supply	
DV_{DD}	Digital positive supply, +5 V ± 5%.
AV_{SS}	Analog negative supply, –5 V ± 5%.
AV_{DD}	Analog positive supply, +5 V ± 5%.
DGND	Digital Ground. Ground reference for digital circuitry.
AGND	Analog Ground. Ground reference for analog circuitry.
Analog and Reference Pins	
$A_{IN}1$, $A_{IN}2$	Analog Inputs. Both analog inputs must be tied together. The input ranges are; 0 V to 2.5 V and ±2.5 V.
V_{REFIN}	Voltage Reference Input. The AD7882 is specified with a voltage reference of 2.5 V, which can be provided externally or by the on-chip voltage reference.
V_{REFOUT}	Voltage Reference Output. The internal 2.5 V reference is provided at this pin. It has an output impedance which is nominally 20 kΩ.
C_{REF1}	10 µF Reference Capacitor. This is a charge reservoir for the coarse internal reference buffer, and it damps voltage excursions at the buffer output. This must be a high quality, low series inductance capacitor.
C_{REF2}	0.2 µF Reference Capacitor. This is a charge reservoir for the fine internal reference buffer, and it damps voltage excursions at the buffer output. This must be a high quality, low series inductance capacitor.
Interface	
$\overline{RD}$	Read, active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the three-state data outputs.
$\overline{CS}$	Chip select, active low logic input. The device is selected when this input is active.
ADD0	Address Input. This control input determines whether the word placed on the output data bus during a read operation is an ADC conversion result or the contents of the control register. A logic low accesses a conversion result while a logic high accesses the control register. When writing, if ADD0 is high, the control register is the destination. If ADD0 is low, the calibration data memory is the destination.
$\overline{WR}$	Write, active low logic input. This input is used in conjunction with $\overline{CS}$ and ADD0 to write data to the AD7882.
DB15–DB0	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Data output coding is 2s complement binary.
Timing and Control	
CLKIN	Clock input, an external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to AV_{SS} enables the internal clock oscillator.
$\overline{BUSY}$	This output indicates converter status. $\overline{BUSY}$ is low during conversion and calibration.
$\overline{CONVST}$	Conversion Start. A low to high transition on this logic input pin, when the AD7882 is configured for asynchronous operation, places the sample-and-hold amplifier in the hold mode and starts conversion.
BIP/$\overline{UP}$	Bipolar/Unipolar select logic input. A logic high selects the bipolar input range (A_{IN} Range = $\pm V_{REFIN}$), and a logic low selects the unipolar range (A_{IN} Range = 0 to V_{REFIN}).
$\overline{SLEEP}$	Sleep function, active low logic input. Once asserted, the AD7882 enters the low power mode. All internal circuitry including the internal voltage reference is powered down. Calibration data is retained.
$\overline{CAL}$	Active low logic input. A logic low on this input resets all internal logic and initiates a calibration. Initiating a calibration overrides all other internal operations and if a conversion is in progress, it will be terminated.
M/S	Mode/Sync Logic Input. This is a dual function pin. When the device is in the CAL mode ($\overline{CAL}$ input low), it determines the calibration mode. When the device is in the normal operating mode, it determines whether conversion is synchronous or asynchronous. Synchronous operation means that the device continuously converts the input in synchronism with the clock. Asynchronous operation means that the device converts the analog input in response to the application of a $\overline{CONVST}$ signal. See Table I for the $\overline{CAL}$, M/S Truth Table. Note that the control register can be used to disable this input pin. See Control Register Section.

Table I. AD7882 Operating Modes

$\overline{CAL}$	M/S	Function
1	0	Asynchronous Operation
1	1	Synchronous Operation
0	0	Device Calibration
0	1	System Calibration

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed in LSBs.

Differential Nonlinearity/No Missed Codes
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC. Differential linearity error is expressed in LSBs. A differential linearity error of ±0.9 LSB or less guarantees no missed codes to the full resolution of the device. Thus, the AD7882 has no missed codes guaranteed to 16 bits.

Unipolar Offset Error
When the device is operating in the 0 to $+V_{REFIN}$ range, the deviation of the first code transition from the ideal (+0.5 LSB) is the unipolar offset error. It is expressed in LSBs.

Unipolar Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (V_{REFIN} – 1.5 LSB) after bipolar zero error has been adjusted out.

Bipolar Zero Error
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal (AGND).

Positive Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal (V_{REFIN} – 1.5 LSB) after bipolar zero error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal (–V_{REFIN} + 0.5 LSB) after bipolar zero error has been adjusted out.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ \text{dB}$$

Thus for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7882, it is defined as

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7882 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Power Supply Rejection Ratio
This is the ratio, in dBs, of the change in positive gain error to the change in AV_{DD}, DV_{DD} or AV_{SS}. It is a dc measurement.

CIRCUIT DESCRIPTION

Analog Input

The analog input circuitry of the AD7882 has SHAs in a ping-pong configuration as in Figure 8. The SHAs alternatively acquire the analog input and hold the output constant for the ADC conversions. During conversion, one of the SHAs is in the hold mode while the other is in the sample mode. The sample and

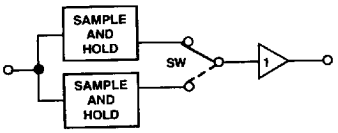


Figure 8. Input SHA Configuration

hold states are then switched after every conversion. The benefit of this configuration is to eliminate the need for acquisition time between conversions. The throughput time is now effectively equal to the conversion time which is 2.5 µs. The analog input range can be either unipolar or bipolar depending on the status of the BIP/$\overline{UP}$ input. The transfer function for the unipolar range is straight binary while the transfer function for the bipolar input is 2s complement. These are shown in Figures 9 and 10.

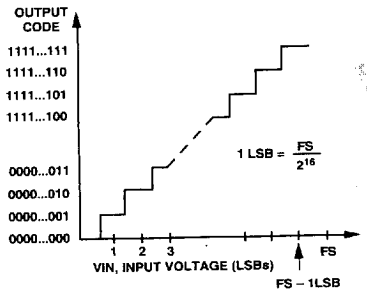


Figure 9. Unipolar Transfer Function

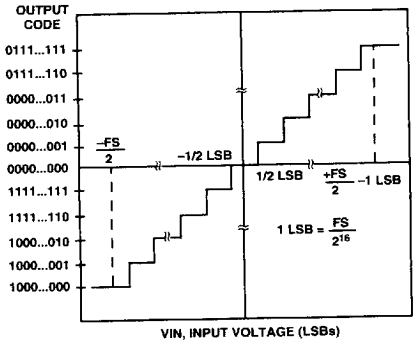


Figure 10. Bipolar Transfer Function

Calibration

The AD7882 conversion procedure is based on the successive approximation algorithm. Accuracy of the individual components, such as the DAC and comparator, is critical to achieve 16-bit performance. The comparator uses an autozero technique to null both internal and external offsets. Another advantage of this scheme is that it nulls 1/f noise. The autozero switching occurs well above the 1/f roll-off frequency, thus the noise appears as a dc offset which gets cancelled.

The internal DAC uses binary weighted capacitors instead of the traditional R-2 R ladder type. This allows the AD7882 to employ a calibration routine that nulls the errors of the individual DAC segments along with offset and gain errors. Each segment of the capacitor DAC contains multiple capacitors that are used to trim for absolute accuracy. During a calibration routine, the DAC segments are compared against other segments and trimmed to 1/4 LSB accuracy. Offset and gain errors are then calibrated either against the device AGND and V_{REFIN} inputs or external reference voltages that are applied at the A_{IN} input.

Calibration Routine

The AD7882 is capable of two calibration methods; system calibration and device calibration. Both modes calibrate the internal DAC linearity along with offset and gain errors. A system calibration is where the device calibrates its full scale and offset voltages against externally applied voltages. For a device calibration, full scale and offset are calibrated against the V_{REFIN} and AGND inputs. Note that a calibration must always be initiated after power on to meet the device performance specifications.

Calibration may be initiated in hardware by asserting the $\overline{CAL}$ pin or in software by writing the appropriate word to the control register. The AD7882 will always perform a full calibration if initiated in hardware. However, under software control, partial calibration options including only offset and gain, can be performed. These options are shown in Table III.

Device Calibration

Device calibration is initiated by pulsing $\overline{CAL}$ low; see Figure 6. Offset and gain are calibrated against the AGND and V_{REFIN} inputs respectively. This calibration procedure takes 928 ms, when using a 10 MHz clock.

System Calibration

System calibration is initiated by a positive edge on $\overline{CAL}$ as shown in Figure 7. $\overline{BUSY}$ goes low three times during the calibration procedure corresponding to the DAC, offset and gain calibrations respectively. The rising edge of the first $\overline{BUSY}$ pulse indicates that the DAC calibration is complete and the AD7882 is now ready to calibrate the offset. This is achieved by applying an external 0 V input at the A_{IN} input and asserting the $\overline{CONVST}$ input. Note, the external 0 V input must be within ±1.5% of AGND. The rising edge of the second $\overline{BUSY}$ pulse indicates that the part is ready to calibrate full scale. This time, the full scale input voltage must be applied to the analog input, and $\overline{CONVST}$ must be asserted once again. The full-scale input voltage must be within ±1.5% of the reference input voltage. Complete calibration time is 928 ms plus the width of the two $\overline{CONVST}$ start pulses, when using a 10 MHz clock for the device.

Configuring the M/S Input

The M/S input with conjunction with the $\overline{CAL}$ input determines the type of calibration to be used when $\overline{CAL}$ is taken low. It also determines whether the conversion is asynchronous (controlled by the $\overline{CONVST}$ input) or synchronous (with CLKIN). In all, they can be configured in four different ways as shown in Figure 11. The $\overline{CAL}$ input is asserted by a positive edge, when calibration is required. Then, for example if synchronous operation and device calibration is required, M/S is tied to $\overline{CAL}$. Note, an inverter can be used between the $\overline{CAL}$ and the M/S inputs when asynchronous operation and system calibration is required.

If $\overline{CAL}$ is high, then the user can start a Calibration from the Control Register.

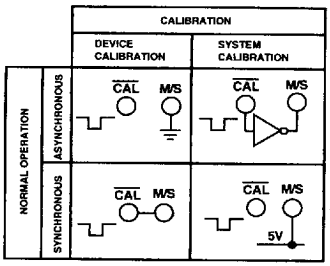


Figure 11. M/S Input Configuration

Timing and Control

Data communication with the AD7882 is controlled by four control inputs: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and ADD0. The data transfer consists of reading and writing to the control register or coefficients register and reading the conversion result from the output data register.

Conversion Control and Data Reads

Conversion can be controlled in hardware by asserting the $\overline{CONVST}$ input (Asynchronous Mode) or the device can be set up for continuous "back-to-back" conversions (Synchronous Mode). The M/S input controls these as outlined above. In synchronous mode, a power-up, CAL or CONVST will initiate operation.

The data outputs are controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. The possible timing configurations are shown in Figures 3, 4 and 5. If $\overline{CS}$ and $\overline{RD}$ are tied permanently low, then the data bus will always be active. However, it will change state at the end of conversion to reflect the most recent result. Reading the data bus must be avoided at this time.

Control Register

The control register serves the dual function of providing control and monitoring the status of the AD7882. This register is directly accessible through the data bus with a read or write operation while ADD0 is high. One of the option settings in the control register is to set up the coefficients register for reading or writing. The coefficient registers contain the calibration coefficients. Loading the coefficients to the register consists of writing forty 16-bit words. This activity is considerably shorter for almost any processor than performing a calibration. Thus, a typical application might read all the coefficients after calibration, store them in the backup memory and rewrite them to the AD7882 in future power-up initialization routines. Reading the calibration coefficients consists of forty read cycles to the AD7882. This will return forty 16-bit words to the microprocessor.

Writing to the AD7882

Data can be written to either the control register or the coefficients register. A typical timing diagram is shown in Figure 12.

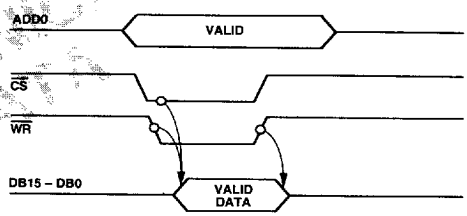


Figure 12. Typical Write Timing

Table II. Control Register Bit Functions

Bit Location	Read/Write I/O Option	Power-Up Default	Function
CR0	Read Only	0	Conversion status. This bit is high during conversion.
CR1	Read Only	0	Calibration status. This bit is high during calibration.
CR2	Read/Write	BIP/$\overline{UP}$	BIP/$\overline{UP}$ Select. Unipolar operation is selected when CR2 is 0; bipolar operation is selected when CR2 is 1. This assumes that CR3 is 1. When CR3 is 0, CR2 reflects the BIP/$\overline{UP}$ input.
CR3	Read/Write	0	If CR3 = 1, then Control Register bits CR2, CR9 and CR10 have priority. Otherwise external pins, $\overline{SLEEP}$ and BIP/$\overline{UP}$, have priority.
CR4	Read/Write	0	CR4 to CR7 determine the calibration function, see Table III.
CR5	Read/Write	1	Calibration function, See CR4.
CR6	Read/Write	1	Calibration function, See CR4.
CR7	Read/Write	1	Calibration function, See CR4.
CR8			Not Used
CR9	Read/Write	$\overline{SLEEP}$	Sleep Control Bit. When CR3 is 1, setting CR9 to 0 powers down all circuitry except the reference. When CR3 is 0, CR9 reflects the state of the $\overline{SLEEP}$ input.
CR10	Read/Write	$\overline{SLEEP}$	Reference power down. When CR3 is 1, reference is powered by writing a 0 to CR10. When CR3 is 0, CR10 reflects the state of the $\overline{SLEEP}$ input.
CR11	Read	0	A 1 in this location indicates an overflow on A_{IN} in the last conversion and a gain adjust is required to bring the input back within range.
CR12	Read	0	A 1 in this location indicates an underflow on A_{IN} in the last conversion and a gain adjust is required to bring the input back within range.
CR13			Not Used
CR14	Read/Write	0	Status Bit. If this is 1, it means that the calibration is halted. Calibration can be continued by writing a 0 to this location.
CR15	Read/Write	1	Reset Bit. All memory and logic is reset when a 0 is written to this location. Reset happens on the rising edge of $\overline{WR}$. If there is a subsequent control register read all bits except CR15 will have power-up default setting. Therefore, to restart after a software reset, it is necessary to write a 1 back into CR15.

Table III. Calibration Options Using the Control Register

CR7	CR6	CR5	CR4	Function
0	0	0	0	Normal Conversion, No Calibration
0	0	0	1	Normal Conversion, No Calibration
0	0	1	0	Gain Error Only–Device Calibration
0	0	1	1	Gain Error Only–System Calibration
0	1	0	0	Offset Error Only–Device Calibration
0	1	0	1	Offset Error Only–System Calibration
0	1	1	0	Offset and Gain Error Only–Device Calibration
0	1	1	1	Offset and Gain Error Only–System Calibration
1	0	0	0	Read All Calibration Coefficients
1	0	0	1	Write All Calibration Coefficients
1	0	1	0	Read Gain Calibration Coefficients Only
1	0	1	1	Write Gain Calibration Coefficients Only
1	1	0	0	Read Offset Calibration Coefficients Only
1	1	0	1	Write Offset Calibration Coefficients Only
1	1	1	0	Full Device Calibration
1	1	1	1	Full System Calibration