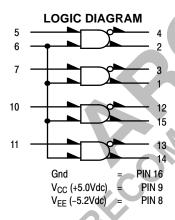
Quad TTL to MECL Translator

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open–emitter outputs that allow use as an inverting/ non–inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

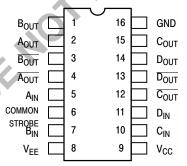
Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

- $P_D = 380 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 3.5 \text{ ns typ } (+1.5 \text{ Vdc in to } 50\% \text{ out})$
- t_r , $t_f = 2.5$ ns typ (20%–80%)



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10124L	CDIP-16	25 Units / Rail
MC10124P	PDIP-16	25 Units / Rail
MC10124FN	PLCC-20	46 Units / Rail

ENTRICAD CHARACTERISTICS

			Test Limits							
		Pin Under	-30	0∘C		+25°C		+85	5°C	1
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit
Negative Power Supply Drain Current	Ι _Ε	8		72			66		72	mAdc
Positive Power Supply	Іссн	9		16			16		18	mAdc
Drain Current	I _{CCL}	9		25			25		25	mAdc
Reverse Current	I _R	6 7		200 50			200 50		200 50	μAdc
Forward Current	I _F	6 7		-12.8 -3.2			-12.8 -3.2		-12.8 -3.2	mAdc
Input Breakdown Voltage	BV _{in}	6 7	5.5 5.5		5.5 5.5			5.5 5.5	C	Vdc
Clamp Input Voltage	VI	6 7		-1.5 -1.5			-1.5 -1.5		-1.5 -1.5	Vdc
High Output Voltage	V _{OH}	1 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Low Output Voltage	V _{OL}	1 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
High Threshold Voltage	V _{OHA}	1 3	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdc
Low Threshold Voltage	V _{OLA}	1 3		-1.655 -1.655		0	-1.630 -1.630		-1.595 -1.595	Vdc
Switching Times (50 Load)	Ω									ns
Propagation Delay (+3.5Vdc to 50%	t ₆₊₁₊ t ₆₋₁₋ t ₇₊₁₊ t ₇₋₁₋ t ₇₊₃₋ t ₇₋₃₊	1 1 1 1 3 3	1.5 1.0 1.5 1.0 1.5	6.8 6.0 6.8 6.0 6.8 6.0	1.0 1.0 1.0 1.0 1.0	3.5 3.5 3.5 3.5 3.5 3.5	6.0 6.0 6.0 6.0 6.0	1.0 1.5 1.0 1.5 1.0	6.0 6.8 6.0 6.8 6.0 6.8	
Rise Time (20 to 809	%) t ₁₊	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3	
Fall Time (20 to 80%	%) t ₁₋	1 .	1.0	4.2	1.1	2.5	3.9	1.1	4.3	

See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

ELECTRICAD CHARACTERISTICS (continued)

OEVICE NO

宣明 1010/10 124亿快业图				TEST VOL	TAGE VALU	ES (Volts)		
	@ Test Te	mperature	V _{IH}	V _{ILmax}	V _{IHA} ,	V _{ILA} ,	V _F	
		-30°C	+4.0	+0.40	+2.00	+1.10	+0.40	
		+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	
		+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	
		Pin	TEST VO	DLTAGE APF	PLIED TO PI	NS LISTED E	BELOW	
Characteristic	Symbol	Under Test	V _{IH}	V _{ILmax}	V _{IHA} ,	V _{ILA} ,	V _F	Gnd
Negative Power Supply Drain Current	Ι _Ε	8						16
Positive Power Supply Drain	Іссн	9	5,6,7,10,11					16
Current	I _{CCL}	9						5,6,7,10,11,16
Reverse Current	I _R	6 7					5,7,10,11 6	16 16
Forward Current	I _F	6 7	5,7,10,11 6				6 7	16 16
Input Breakdown Voltage	BV _{in}	6 7					0,	5,7,10,11,16 6,16
Clamp Input Voltage	VI	6 7						16 16
High Output Voltage	V _{OH}	1 3	6,7	6,7				16 16
Low Output Voltage	V _{OL}	1 3	6,7	6,7	.0			16 16
High Threshold Voltage	V _{OHA}	1 3	6 6		7	7		16 16
Low Threshold Voltage	V _{OLA}	1 3	6		7	7		16 16
Switching Times (50Ω Load)		05	+6.0 V	Pulse In	Pulse Out			+2.0 V
Propagation Delay (+3.5Vdc to 50%) ¹	t ₆₊₁₊ t ₆₋₁₋	1 1	7 7 6	6 6 7	1 1 1			16 16 16
	t ₇₊₁₊ t ₇₋₁₋	1	6	7	1			16
	t ₇₊₃₋	3	6 6	7 7	3 3			16 16
Pigo Timo (20 to 200/)	t ₇₋₃₊							16 16
Rise Time (20 to 80%)	t ₁₊		6	7 7	1			16
Fall Time (20 to 80%)	t ₁₋		6	·	1			16

^{1.} See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS (continued)

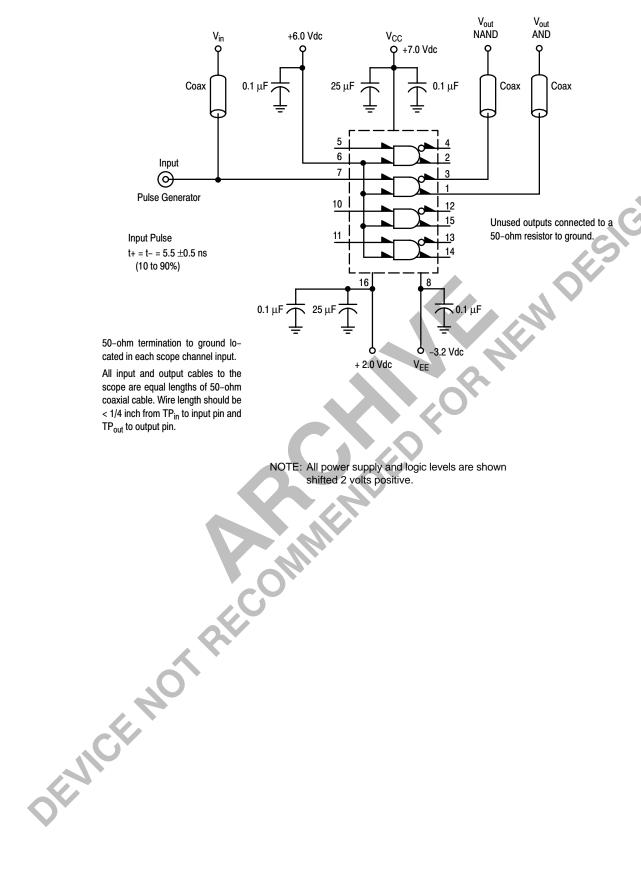
			TEST VOLTAGE VALUES (Volts)		(mA)			
	@ Test Temperature			V _{CC}	V _{EE}	lı	l _{in}	
		-30°C	+2.40	+5.00	-5.2	-10	+1.0	
	+25°C		+2.40	+5.00	-5.2	-10	+1.0	
		+85°C	+2.40	+5.00	-5.2	-10	+1.0	
		Pin	TEST V	OLTAGE AP	PLIED TO PI	NS LISTED	BELOW	
Characteristic	Symbol	Under Test	V _R	V _{CC}	V _{EE}	I _I	l _{in}	Gnd
Negative Power Supply Drain Current	ΙE	8		9	8			16
Positive Power Supply Drain	Іссн	9		9	8			16
Current	I _{CCL}	9		9	8			5,6,7,10,11,16
Reverse Current	I _R	6 7	6 7	9 9	8 8			16 16
Forward Current	l _F	6 7		9 9	8 8			16 16
Input Breakdown Voltage	BV _{in}	6 7		9 9	8 8		6 7	5,7,10,11,16 6,16
Clamp Input Voltage	VI	6 7		9 9	8 8	6 7		16 16
High Output Voltage	V _{OH}	1 3		9 9	8 8			16 16
Low Output Voltage	V _{OL}	1 3		9 9	8 8			16 16
High Threshold Voltage	V _{OHA}	1 3		9 9	8 8			16 16
Low Threshold Voltage	V _{OLA}	1 3		9	8 8			16 16
Switching Times (50Ω Load)				+7.0 V	-3.2 V			+2.0 V
Propagation Delay (+3.5Vdc to 50%) ¹	t ₆₊₁₊ t ₆₋₁₋	1		9 9	8 8			16 16
(13.3740 to 3070)	t ₇₊₁₊	1		9	8			16
	t ₇₋₁₋	1		9	8			16
	t ₇₊₃ _ t ₇₋₃₊	3		9 9	8 8			16 16
Rise Time (20 to 80%)	t ₁₊	9		9	8			16
Fall Time (20 to 80%)	t ₁₋	1		9	8			16

^{1.} See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

查询"MC10124L"供应商

SWITCHING TIME TEST CIRCUIT



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

查询"MC10124L"供应商

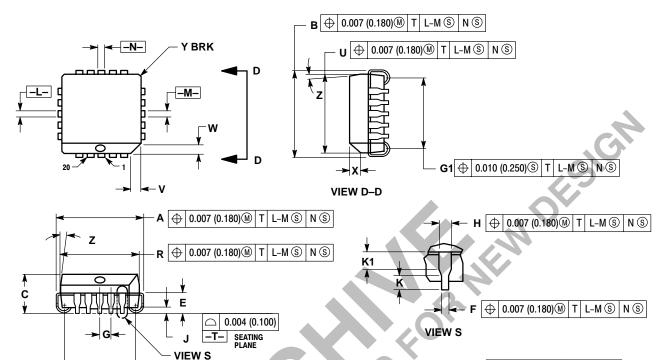
G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF VICE NOT PRESCO

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



- OTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

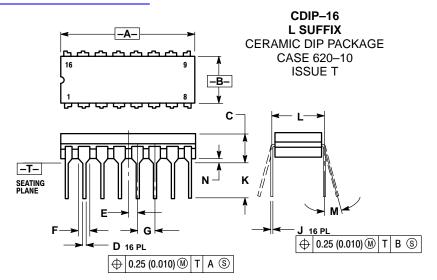
 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

 4. DIMENSIONING AND TOLERANCING PER ANSI V14 5M 1982
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
Ε	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50
Z	2°	10°	2°	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

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PACKAGE DIMENSIONS



NOTES:

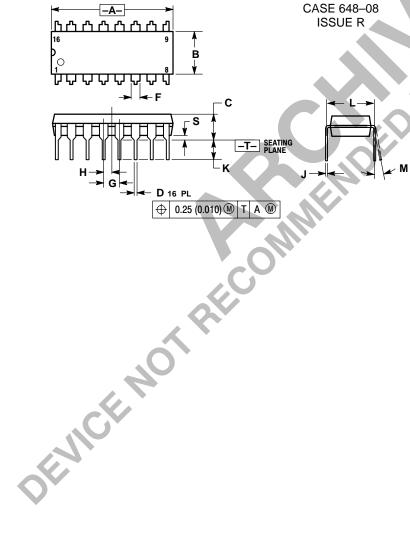
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
C		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62		
M	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0°	10 °	
S	0.020	0.040	0.51	1.01	

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