

ULTRA-SMALL LOW-POWER 12-BIT ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE

Check for Samples: [ADS1015-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Wide Supply Range: 2.0V to 5.5V
- Low Current Consumption:
Continuous Mode: Only 150 μ A
Single-Shot Mode: Auto Shut-Down
- Programmable Data Rate:
128SPS to 3.3kSPS
- Internal Low-Drift Voltage Reference
- Internal Oscillator
- Internal PGA
- I²C™ Interface: Pin-Selectable Addresses
- Four Single-Ended or Two Differential Inputs
- Programmable Comparator

APPLICATIONS

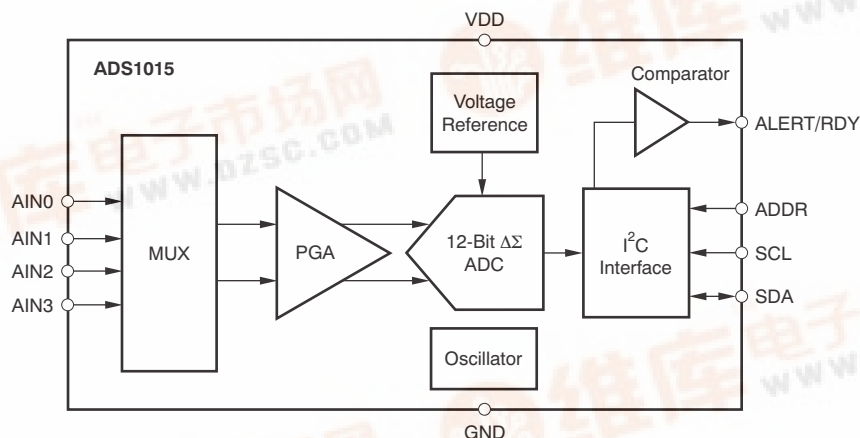
- Portable Instrumentation
- Consumer Goods
- Battery Monitoring
- Temperature Measurement
- Factory Automation and Process Controls

DESCRIPTION

The ADS1015 is a precision analog-to-digital converter (ADC) with 12 bits of resolution offered in an MSOP-10 package. The ADS1015 is designed with precision, power, and ease of implementation in mind. The ADS1015 features an on-board reference and oscillator. Data are transferred via an I²C-compatible serial interface; four I²C slave addresses can be selected. The ADS1015 operates from a single power supply ranging from 2.0V to 5.5V.

The ADS1015 can perform conversions at rates up to 3300 samples per second (SPS). An onboard PGA is available that offers input ranges from the supply to as low as ± 256 mV, allowing both large and small signals to be measured with high resolution. The ADS1015 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs.

The ADS1015 operates either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods. The ADS1015 is specified from -40°C to $+125^{\circ}\text{C}$.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 125°C | VSSOP – DGS | Reel of 2500 | ADS1015QDGSRQ1 | BCMQ |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | ADS1015 | UNIT |
|--|-------------------|------|
| VDD to GND | –0.3 to +5.5 | V |
| Analog input current | 100, momentary | mA |
| Analog input current | 10, continuous | mA |
| Analog input voltage to GND | –0.3 to VDD + 0.3 | V |
| SDA, SCL, ADDR, ALERT/RDY voltage to GND | –0.5 to +5.5 | V |
| Maximum junction temperature | +150 | °C |
| Storage temperature range | –60 to +150 | °C |

- (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT FAMILY

| DEVICE | PACKAGE DESIGNATOR MSOP/QFN | RESOLUTION (Bits) | MAXIMUM SAMPLE RATE (SPS) | COMPARATOR | PGA | INPUT CHANNELS (Differential/ Single-Ended) |
|---------|--------------------------------|----------------------|------------------------------|------------|-----|---|
| ADS1113 | BROI/N6J | 16 | 860 | No | No | 1/1 |
| ADS1114 | BRNI/N5J | 16 | 860 | Yes | Yes | 1/1 |
| ADS1115 | BOGI/N4J | 16 | 860 | Yes | Yes | 2/4 |
| ADS1013 | BRMI/N9J | 12 | 3300 | No | No | 1/1 |
| ADS1014 | BRQI/N8J | 12 | 3300 | Yes | Yes | 1/1 |
| ADS1015 | BRPI/N7J | 12 | 3300 | Yes | Yes | 2/4 |

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C.

| PARAMETER | TEST CONDITIONS | ADS1015 | | | UNIT |
|---|---|---|---|-------------------|--------|
| | | MIN | TYP | MAX | |
| ANALOG INPUT | | | | | |
| Full-scale input voltage ⁽¹⁾ | V _{IN} = (A _{INP}) – (A _{INN}) | | ±4.096/PGA | | V |
| Analog input voltage | A _{INP} or A _{INN} to GND | GND | | VDD | V |
| Differential input impedance | | | See Table 2 | | |
| Common-mode input impedance | FS = ±6.144V ⁽¹⁾ | | 10 | | MΩ |
| | FS = ±4.096V ⁽¹⁾ , ±2.048V | | 6 | | MΩ |
| | FS = ±1.024V | | 3 | | MΩ |
| | FS = ±0.512V, ±0.256V | | 100 | | MΩ |
| SYSTEM PERFORMANCE | | | | | |
| Resolution | No missing codes | 12 | | | Bits |
| Data rate (DR) | | | 128, 250, 490, 920, 1600, 2400, 3300 | | SPS |
| Data rate variation | All data rates | –10 | | 10 | % |
| Output noise | | See Typical Characteristics | | | |
| Integral nonlinearity | DR = 128SPS, FS = ±2.048V, best fit ⁽²⁾ | | | 0.5 | LSB |
| Offset error | FS = ±2.048V, differential inputs | | 0 | ±0.5 | LSB |
| | FS = ±2.048V, single-ended inputs | | ±0.25 | | LSB |
| Offset drift | FS = ±2.048V | | 0.005 | | LSB/°C |
| Gain error ⁽³⁾ | FS = ±2.048V at 25°C | | 0.05 | 0.25 | % |
| Gain drift ⁽³⁾ | FS = ±0.256V | | 7 | | ppm/°C |
| | FS = ±2.048V | | 5 | 40 ⁽⁴⁾ | ppm/°C |
| | FS = ±6.144V ⁽¹⁾ | | 5 | | ppm/°C |
| PGA gain match ⁽³⁾ | Match between any two PGA gains | | 0.02 | 0.1 | % |
| Gain match | Match between any two inputs | | 0.05 | 0.1 | % |
| Offset match | Match between any two inputs | | 0.25 | | LSB |
| DIGITAL INPUT/OUTPUT | | | | | |
| Logic level | | | | | |
| V _{IH} | | 0.7VDD | | 5.5 | V |
| V _{IL} | | GND – 0.5 | | 0.3VDD | V |
| V _{OL} | I _{OL} = 3mA | GND | 0.15 | 0.4 | V |
| Input leakage | | | | | |
| I _H | V _{IH} = 5.5V | | | 10 | μA |
| I _L | V _{IL} = GND | 10 | | | μA |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

(2) 99% of full-scale.

(3) Includes all errors from onboard PGA and reference.

(4) Not production tested

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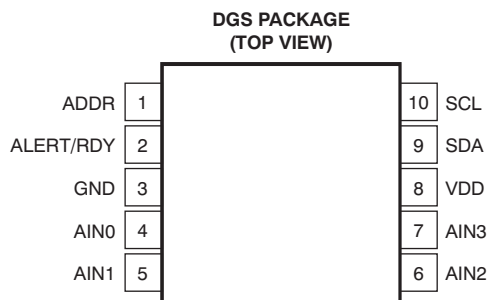
ELECTRICAL CHARACTERISTICS (continued)

All specifications at -40°C to $+125^{\circ}\text{C}$, $V_{\text{DD}} = 3.3\text{V}$, and Full-Scale (FS) = $\pm 2.048\text{V}$, unless otherwise noted.

Typical values are at $+25^{\circ}\text{C}$.

| PARAMETER | TEST CONDITIONS | ADS1015 | | | UNIT |
|---------------------------|--------------------------------|---------|-----|------|------|
| | | MIN | TYP | MAX | |
| POWER-SUPPLY REQUIREMENTS | | | | | |
| Power-supply voltage | | 2 | | 5.5 | V |
| Supply current | Power-down current at 25°C | | 0.5 | 2 | μA |
| | Power-down current up to 125°C | | | 5 | μA |
| | Operating current at 25°C | | 150 | 200 | μA |
| | Operating current up to 125°C | | | 300 | μA |
| Power dissipation | VDD = 5.0V | | 0.9 | | mW |
| | VDD = 3.3V | | 0.5 | | mW |
| | VDD = 2.0V | | 0.3 | | mW |
| TEMPERATURE | | | | | |
| Storage temperature | | −60 | | +150 | °C |
| Specified temperature | | −40 | | +125 | °C |

PIN CONFIGURATIONS



PIN DESCRIPTIONS

| PIN | | FUNCTION | DESCRIPTION |
|-----|-----------|----------------|--|
| NO. | NAME | | |
| 1 | ADDR | Digital input | $I^2\text{C}$ slave address select |
| 2 | ALERT/RDY | Digital output | Digital comparator output or conversion ready |
| 3 | GND | Supply | Ground |
| 4 | AIN0 | Analog input | Differential channel 1: Positive input or single-ended channel 1 input |
| 5 | AIN1 | Analog input | Differential channel 1: Negative input or single-ended channel 2 input |
| 6 | AIN2 | Analog input | Differential channel 2: Positive input or single-ended channel 3 input |
| 7 | AIN3 | Analog input | Differential channel 2: Negative input or single-ended channel 4 input |
| 8 | VDD | Supply | Power supply: 2.0V to 5.5V |
| 9 | SDA | Digital I/O | Serial data: Transmits and receives data |
| 10 | SCL | Digital input | Serial clock input: Clocks data on SDA |

TIMING REQUIREMENTS

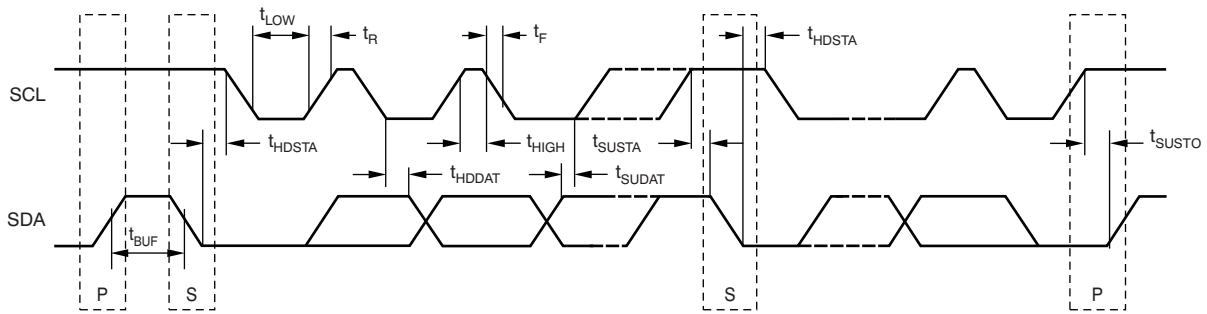


Figure 1. I²C Timing Diagram

Table 1. I²C Timing Definitions

| PARAMETER | | FAST MODE | | HIGH-SPEED MODE | | UNIT |
|--|-------------|-----------|-----|-----------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| SCL operating frequency | f_{SCL} | 0.01 | 0.4 | 0.01 | 3.4 | MHz |
| Bus free time between START and STOP condition | t_{BUF} | 600 | | 160 | | ns |
| Hold time after repeated START condition. After this period, the first clock is generated. | t_{HDSTA} | 600 | | 160 | | ns |
| Repeated START condition setup time | t_{SUSTA} | 600 | | 160 | | ns |
| Stop condition setup time | t_{SUSTO} | 600 | | 160 | | ns |
| Data hold time | t_{HDDAT} | 0 | | 0 | | ns |
| Data setup time | t_{SUDAT} | 100 | | 10 | | ns |
| SCL clock low period | t_{LOW} | 1300 | | 160 | | ns |
| SCL clock high period | t_{HIGH} | 600 | | 60 | | ns |
| Clock/data fall time | t_F | | 300 | | 160 | ns |
| Clock/data rise time | t_R | | 300 | | 160 | ns |

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_{DD} = 3.3\text{V}$, unless otherwise noted.

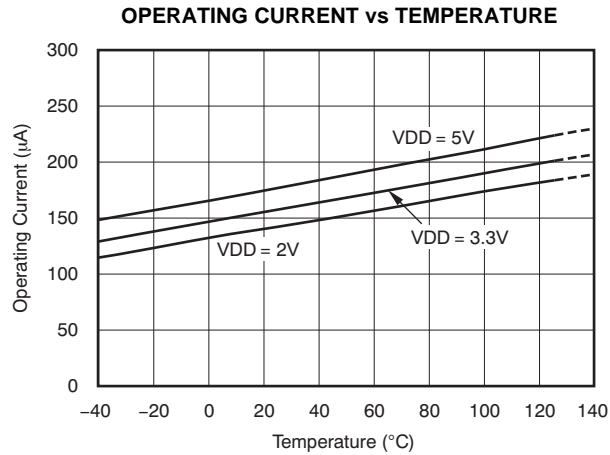


Figure 2.

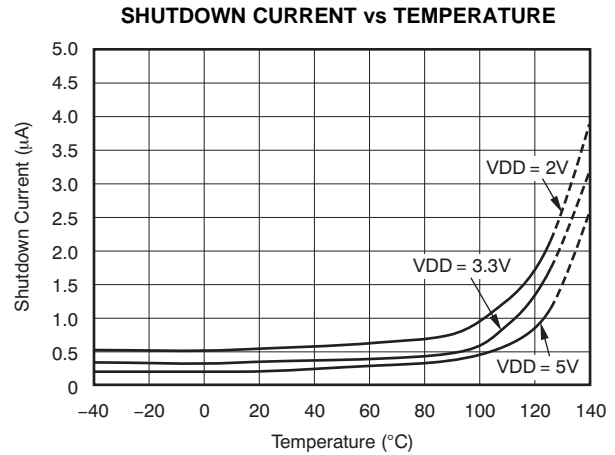


Figure 3.

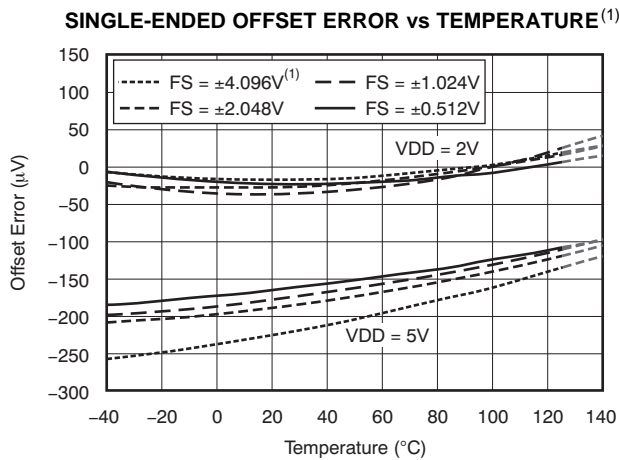


Figure 4.

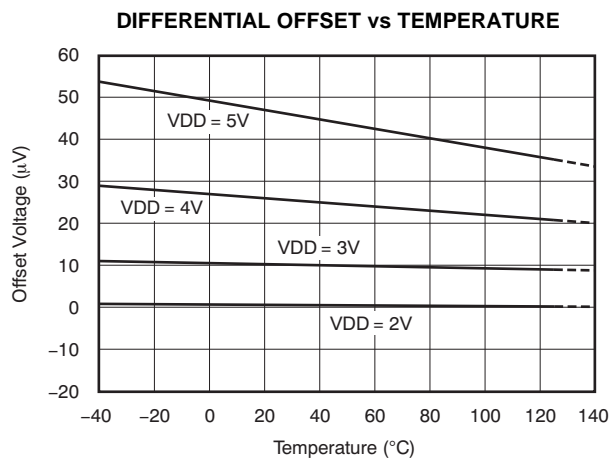


Figure 5.

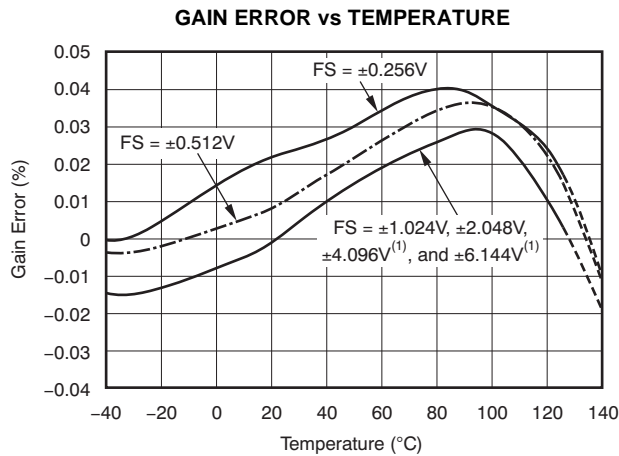


Figure 6.

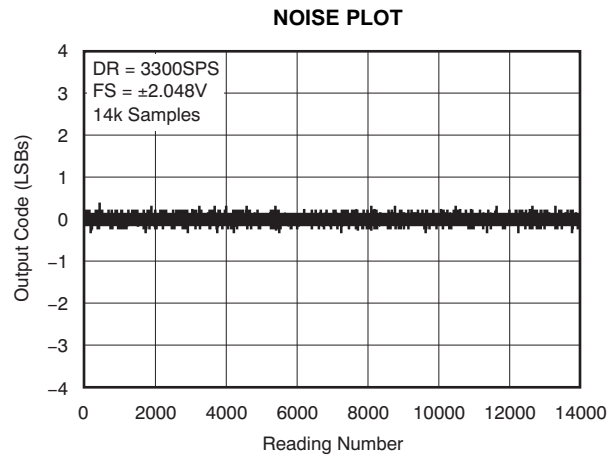


Figure 7.

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than $V_{DD} + 0.3\text{V}$ be applied to this device.

OVERVIEW

The ADS1015 is very small, low-power, 12-bit, delta-sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs). The ADS1015 is extremely easy to configure and design into a wide variety of applications, and allow precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1015 to be intuitive and problem-free.

The ADS1015 consist of a $\Delta\Sigma$ analog-to-digital (A/D) core with adjustable gain, an internal voltage reference, a clock oscillator, and an I²C interface. Another feature available on the ADS1015 is a programmable digital comparator that provides an alert on a dedicated pin. All of these features are intended to reduce required external circuitry and improve performance. [Figure 8](#) shows the ADS1015 functional block diagram.

The ADS1015 A/D core measures a differential signal, V_{IN} , that is the difference of A_{INP} and A_{INN} . A MUX is available on the ADS1015. This architecture results in a very strong attenuation of any common-mode signals. The converter core consists of a differential, switched-capacitor $\Delta\Sigma$ modulator followed by a digital filter. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1015 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal result register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

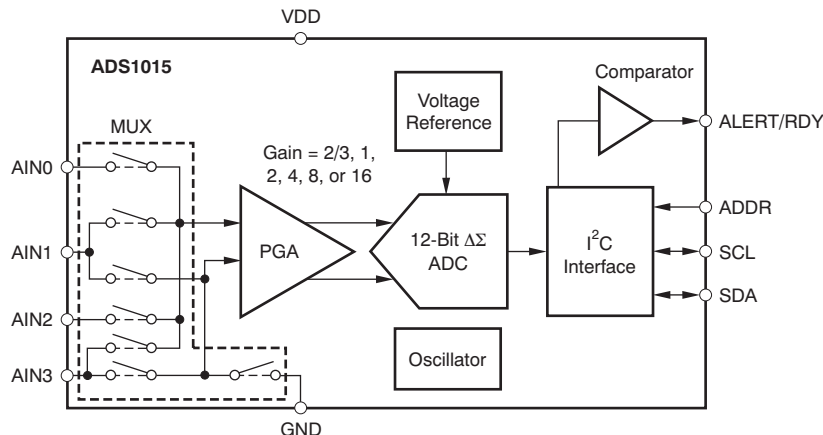


Figure 8. Functional Block Diagram

QUICKSTART GUIDE

This section provides a brief example of ADS1015 communications. Refer to subsequent sections of this data sheet for more detailed explanations. Hardware for this design includes: one ADS1015 configured with an I²C address of 1001000; a microcontroller with an I²C interface (TI recommends the [MSP430](#) product line); discrete components such as resistors, capacitors, and serial connectors; and a 2V to 5V power supply. [Figure 9](#) shows the basic hardware configuration.

The ADS1015 communicates with the master (microcontroller) through an I²C interface. The master provides a clock signal on the SCL pin and data are transferred via the SDA pin. The ADS1015 never drives the SCL pin. For information on programming and debugging the microcontroller being used, refer to the device-specific product data sheet.

The first byte sent by the master should be the ADS1015 address followed by a bit that instructs the ADS1015 to listen for a subsequent byte. The second byte is the register pointer. Refer to [Table 6](#) for a register map. The third and fourth bytes sent from the master are written to the register indicated in the second byte. Refer to [Figure 16](#) and [Figure 17](#) for read and write operation timing diagrams, respectively. All read and write transactions with the ADS1015 must be preceded by a start condition and followed by a stop condition.

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For example, to write to the configuration register to set the ADS1015 to continuous conversion mode and then read the conversion result, send the following bytes in this order:

Write to Config register:

First byte: 0b10010000 (first 7-bit I²C address followed by a low read/write bit)

Second byte: 0b00000001 (points to Config register)

Third byte: 0b00000100 (MSB of the Config register to be written)

Fourth byte: 0b10000011 (LSB of the Config register to be written)

Write to Pointer register:

First byte: 0b10010000 (first 7-bit I²C address followed by a low read/write bit)

Second byte: 0b00000000 (points to Conversion register)

Read Conversion register:

First byte: 0b10010001 (first 7-bit I²C address followed by a high read/write bit)

Second byte: the ADS1015 response with the MSB of the Conversion register

Third byte: the ADS1015 response with the LSB of the Conversion register

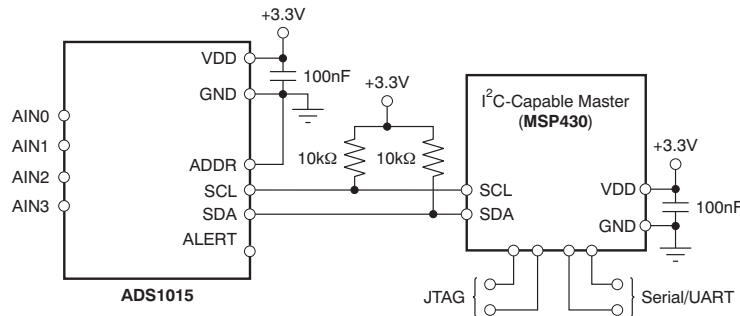


Figure 9. Basic Hardware Configuration

MULTIPLEXER

The ADS1015 contains an input multiplexer, as shown in [Figure 10](#). Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 may be measured differentially to AIN3. The multiplexer is configured by three bits in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

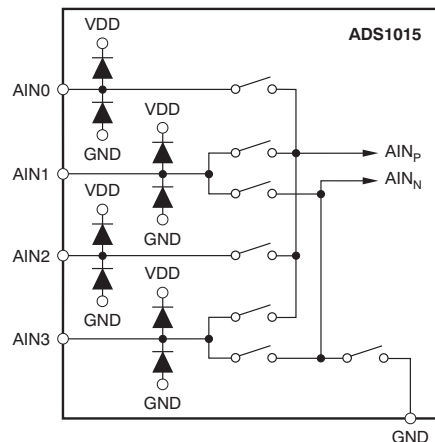


Figure 10. Multiplexer

When measuring single-ended inputs it is important to note that the negative range of the output codes are not used. These codes are for measuring negative differential signals such as $(A_{IN_P} - A_{IN_N}) < 0$. ESD diodes to VDD and GND protect the inputs on the ADS1015. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the following range:

$$GND - 0.3V < A_{INx} < VDD + 0.3V \quad (1)$$

If it is possible that the voltages on the input pins may violate these conditions, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the [Absolute Maximum Ratings](#) table).

Also, overdriving one unused input on the ADS1015 may affect conversions taking place on other input pins. If overdrive on unused inputs is possible, again it is recommended to clamp the signal with external Schottky diodes.

ANALOG INPUTS

The ADS1015 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between A_{IN_P} and A_{IN_N} . The capacitors used are small, and to external circuitry the average loading appears resistive. This structure is shown in [Figure 12](#). The resistance is set by the capacitor values and the rate at which they are switched. [Figure 11](#) shows the on/off setting of the switches illustrated in [Figure 12](#). During the sampling phase, S_1 switches are closed. This event charges C_{A1} to A_{IN_P} , C_{A2} to A_{IN_N} , and C_B to $(A_{IN_P} - A_{IN_N})$. During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7V and C_B discharges to 0V. This charging draws a very small transient current from the source driving the ADS1015 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}) where $R_{eff} = V_{IN}/I_{AVERAGE}$.

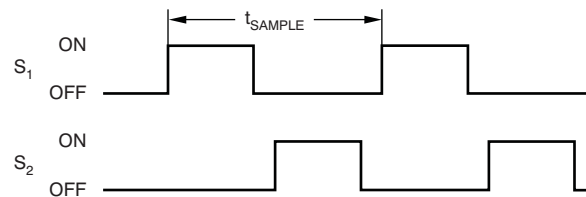


Figure 11. S_1 and S_2 Switch Timing for [Figure 12](#)

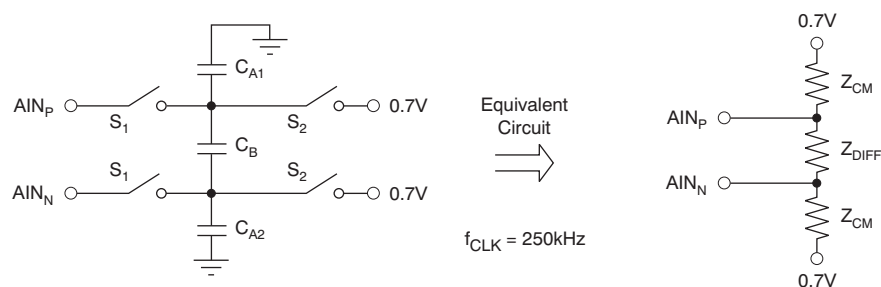


Figure 12. Simplified Analog Input Circuit

The common-mode input impedance is measured by applying a common-mode signal to shorted A_{IN_P} and A_{IN_N} inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately $6M\Omega$ for the default PGA gain setting. In [Figure 12](#), the common-mode input impedance is Z_{CM} .

The differential input impedance is measured by applying a differential signal to A_{IN_P} and A_{IN_N} inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the PGA gain setting. In [Figure 12](#), the differential input impedance is Z_{DIFF} . [Table 2](#) describes the typical differential input impedance.

Table 2. Differential Input Impedance

| FS (V) | DIFFERENTIAL INPUT IMPEDANCE |
|---------------------------|------------------------------|
| $\pm 6.144\text{V}^{(1)}$ | 22M Ω |
| $\pm 4.096\text{V}^{(1)}$ | 15M Ω |
| $\pm 2.048\text{V}$ | 4.9M Ω |
| $\pm 1.024\text{V}$ | 2.4M Ω |
| $\pm 0.512\text{V}$ | 710k Ω |
| $\pm 0.256\text{V}$ | 710k Ω |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than $V_{DD} + 0.3\text{V}$ be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1015 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in [Table 2](#) for typical input impedance are valid.

FULL-SCALE INPUT

A programmable gain amplifier (PGA) is implemented before the $\Delta\Sigma$ core of the ADS1015. The PGA can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 3 shows the corresponding full-scale (FS) ranges. The PGA is configured by three bits in the Config register. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when VDD is larger than 4V. Note though that in this case (as well as for PGA = 1 and VDD < 4V), it is not possible to reach a full-scale output code on the ADC. Analog input voltages may never exceed the analog input voltage limits given in the Electrical Characteristics table.

Table 3. PGA Gain Full-Scale Range

| PGA SETTING | FS (V) |
|-------------|--------------------|
| 2/3 | $\pm 6.144V^{(1)}$ |
| 1 | $\pm 4.096V^{(1)}$ |
| 2 | $\pm 2.048V$ |
| 4 | $\pm 1.024V$ |
| 8 | $\pm 0.512V$ |
| 16 | $\pm 0.256V$ |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

DATA FORMAT

The ADS1015 provides 12 bits of data in binary two complement format. The positive full-scale input produces an output code of 7FF0h and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 4 summarizes the ideal output codes for different input signals. Figure 13 shows code transitions versus input voltage.

Table 4. Input Signal versus Ideal Output Code

| INPUT SIGNAL, V_{IN} ($A_{INP} - A_{INN}$) | IDEAL OUTPUT CODE ⁽¹⁾ |
|---|----------------------------------|
| $\geq FS (2^{11} - 1)/2^{11}$ | 7FF0h |
| $+FS/2^{11}$ | 0010h |
| 0 | 0 |
| $-FS/2^{11}$ | FFF0h |
| $\leq -FS$ | 8000h |

(1) Excludes the effects of noise, INL, offset, and gain errors.

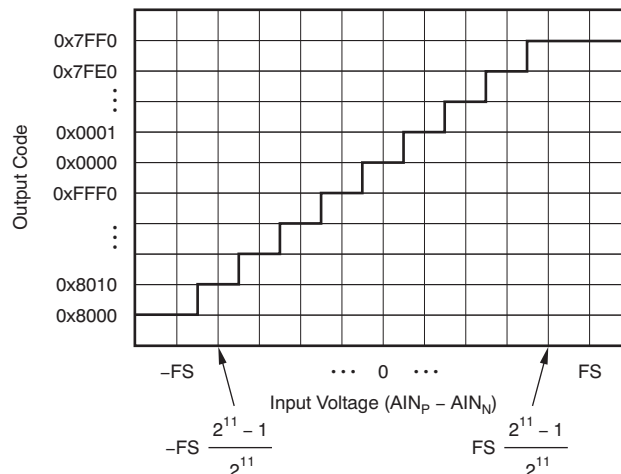


Figure 13. Code Transition Diagram

ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited. For example, the output of a thermocouple, which has a limited rate of change. Nevertheless, they can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1015 digital filter provides some attenuation of high-frequency noise, but the digital Sinc filter frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the ADS1015.

OPERATING MODES

The ADS1015 operates in one of two modes: continuous conversion or single-shot. In continuous conversion mode, the ADS1015 continuously performs conversions. Once a conversion has been completed, the ADS1015 places the result in the Conversion register and immediately begins another conversion. In single-shot mode, the ADS1015 waits until the OS bit is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the OS bit reasserts and the device powers down. Writing a '1' to the OS bit during a conversion has no effect.

RESET AND POWER-UP

When the ADS1015 powers up, a reset is performed. As part of the reset process, the ADS1015 sets all of the bits in the Config register to the respective default settings.

The ADS1015 responds to the I²C general call reset command. When the ADS1015 receives a general call reset, an internal reset is performed as if the device had been powered on.

DUTY CYCLING FOR LOW POWER

For many applications, the improved performance at low data rates may not be required. For these applications, the ADS1015 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1015 in power-down mode with a data rate set to 3300SPS could be operated by a microcontroller that instructs a single-shot conversion every 7.8ms (128SPS). Because a conversion at 3300SPS only requires about 0.3ms, the ADS1015 enters power-down mode for the remaining 7.5ms. In this configuration, the ADS1015 consumes about 1/25th the power of the ADS1015 operated in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller. The ADS1015 offers lower data rates that do not implement duty cycling and offer improved noise performance if it is needed.

COMPARATOR

The ADS1015 is equipped with a customizable comparator that can issue an alert on the ALERT/RDY pin. This feature can significantly reduce external circuitry for many applications. The comparator can be implemented as either a traditional comparator or a window comparator via the COMP_MODE bit in the Config register. When implemented as a traditional comparator, the ALERT/RDY pin asserts (active low by default) when conversion data exceed the limit set in the high threshold register. The comparator then deasserts when the input signal falls below the low threshold register value. In window comparator mode, the ALERT/RDY pin asserts if conversion data exceed the high threshold register or fall below the low threshold register.

In either window or traditional comparator mode, the comparator can be configured to latch once asserted by the COMP_LAT bit in the Config register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can be cleared by issuing an SMBus alert response or by reading the Conversion register. The COMP_POL bit in the Config register configures the ALERT/RDY pin as active high or active low. Operational diagrams for the comparator modes are shown in [Figure 14](#) and [Figure 15](#).

The comparator can be configured to activate the ALERT/RDY pin after a set number of successive readings exceed the threshold. The comparator can be configured to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin by changing the COMP_QUE bits in the Config register. The COMP_QUE bits can also disable the comparator function.

CONVERSION READY PIN

The ALERT/RDY pin can also be configured as a conversion ready pin. This mode of operation can be realized if the MSB of the high threshold register is set to '1' and the MSB of the low threshold register is set to '0'. The COMP_POL bit continues to function and the COMP_QUE bits can disable the pin; however, the COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion ready pin, ALERT/RDY continues to require a pullup resistor. When in continuous conversion mode, the ADS1015 provides a brief (~8µs) pulse on the ALERT/RDY pin at the end of each conversion. When in single-shot shutdown mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to '0'.

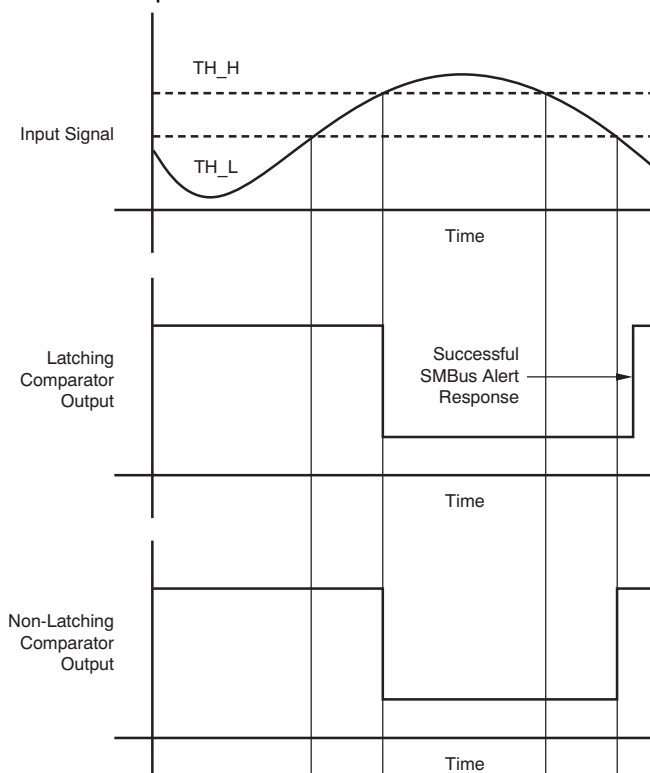


Figure 14. Alert Pin Timing Diagram When Configured as a Traditional Comparator

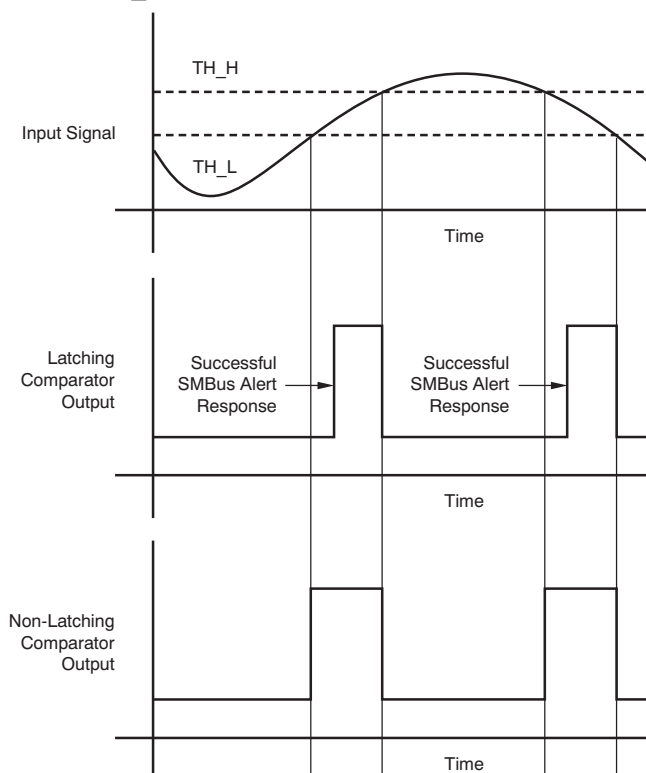


Figure 15. Alert Pin Timing Diagram When Configured as a Window Comparator

SMBus ALERT RESPONSE

When configured in latching mode (COMP_LAT = '1' in the Config register), the ALERT/RDY pin can be implemented with an SMBus alert. The pin asserts if the comparator detects a conversion that exceeds an upper or lower threshold. This interrupt is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I²C address. If conversion data exceed the upper or lower thresholds after being cleared, the pin reasserts. This assertion does not affect conversions that are already in progress. The ALERT/RDY pin, as with the SDA pin, is an open-drain pin. This architecture allows several devices to share the same interface bus. When disabled, the pin holds a high state so that it does not interfere with other devices on the same bus line.

When the master senses that the ALERT/RDY pin has latched, it issues an SMBus alert command (00011001) to the I²C bus. Any ADS1015 data converters on the I²C bus with the ALERT/RDY pins asserted respond to the command with the slave address. This sequence is illustrated in Figure 18. In the event that two or more ADS1015 data converters present on the bus assert the latched ALERT/RDY pin, arbitration during the address

response portion of the SMBus alert decides which device clears its assertion. The device with the lowest I²C address always wins arbitration. If a device loses arbitration, it does not clear the comparator output pin assertion. The master then repeats the SMBus alert response until all devices have had the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a '1' if signals exceed the high threshold and a '0' if signals exceed the low threshold.

I²C INTERFACE

The ADS1015 communicates through an I²C interface. I²C is a two-wire open-drain interface that supports multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I²C devices can act as masters or slaves, but the ADS1015 can only act as a slave device.

An I²C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I²C bus in groups of eight bits. To send a bit on the I²C bus, the SDA line is driven to the appropriate level while SCL is low (a low on SDA indicates the bit is zero; a high indicates the bit is one). Once the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I²C bus is held idle for more than 25ms, the bus times out.

The I²C bus is bidirectional: the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1015 never drives SCL, because it cannot act as a master. On the ADS1015, SCL is an input only.

Most of the time the bus is idle; no communication occurs, and both lines are high. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the *address byte*. Each device on an I²C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I²C bus, whether it is address or data, is acknowledged with an *acknowledge* bit. When the master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, it pulls SDA low to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (The master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low.

When the master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

See the [Timing Requirements](#) section for a timing diagram showing the ADS1015 I²C transaction.

I²C ADDRESS SELECTION

The ADS1015 has one address pin, ADDR, that sets the I²C address. This pin can be connected to ground, VDD, SDA, or SCL, allowing four addresses to be selected with one pin as shown in [Table 5](#). The state of the address pin ADDR is sampled continuously.

Table 5. ADDR Pin Connection and Corresponding Slave Address

| ADDR PIN | SLAVE ADDRESS |
|----------|---------------|
| Ground | 1001000 |
| VDD | 1001001 |
| SDA | 1001010 |
| SCL | 1001011 |

I²C GENERAL CALL

The ADS1015 responds to the I²C general call address (0000000) if the eighth bit is '0'. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110 (06h), the ADS1015 resets the internal registers and enters power-down mode.

I²C SPEED MODES

The I²C bus operates at one of three speeds. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz; and high-speed mode (also called Hs mode) allows a clock frequency of up to 3.4MHz. The ADS1015 is fully compatible with all three modes.

No special action is required to use the ADS1015 in standard or fast mode, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of 00001xxx following the START condition, where xxx are bits unique to the Hs-capable master. This byte is called the Hs master code. (Note that this is different from normal address bytes; the eighth bit does not indicate read/write status.) The ADS1015 does not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. Upon receiving a master code, the ADS1015 switches on Hs mode filters, and communicate at up to 3.4MHz. The ADS1015 switches out of Hs mode with the next STOP condition.

For more information on high-speed mode, consult the I²C specification.

SLAVE MODE OPERATIONS

The ADS1015 can act as either slave receivers or slave transmitter. As a slave device, the ADS1015 cannot drive the SCL line.

Receive Mode:

In slave receive mode the first byte transmitted from the master to the slave is the address with the R/W bit low. This byte allows the slave to be written to. The next byte transmitted by the master is the register pointer byte. The ADS1015 then acknowledges receipt of the register pointer byte. The next two bytes are written to the address given by the register pointer. The ADS1015 acknowledges each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

Transmit Mode:

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high R/W bit. This byte places the slave into transmit mode and indicates that the ADS1015 is being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the register pointer. This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master may terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

WRITING/READING THE REGISTERS

To access a specific register from the ADS1015, the master must first write an appropriate value to the Pointer register. The Pointer register is written directly after the slave address byte, low R/W bit, and a successful slave acknowledgment. After the Pointer register is written, the slave acknowledges and the master issues a STOP or a repeated START condition.

When reading from the ADS1015, the previous value written to the Pointer register determines the register that is read from. To change which register is read, a new value must be written to the Pointer register. To write a new value to the Pointer register, the master issues a slave address byte with the R/W bit low, followed by the Pointer

register byte. No additional data need to be transmitted, and a STOP condition can be issued by the master. The master may now issue a START condition and send the slave address byte with the R/W bit high to begin the read. [Figure 16](#) details this sequence. If repeated reads from the same register are desired, there is no need to continually send Pointer register bytes, because the ADS1015 stores the value of the Pointer register until it is modified by a write operation. However, every write operation requires the Pointer register to be written.

REGISTERS

The ADS1015 has four registers that are accessible via the I²C port. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1015 operating modes and query the status of the device. Two registers, Lo_thresh and Hi_thresh, set the threshold values used for the comparator function.

POINTER REGISTER

The four registers are accessed by writing to the Pointer register byte; see [Figure 16](#). [Table 6](#) and [Table 7](#) indicate the Pointer register byte map.

Table 6. Register Address

| BIT 1 | BIT 0 | REGISTER |
|-------|-------|---------------------|
| 0 | 0 | Conversion register |
| 0 | 1 | Config register |
| 1 | 0 | Lo_thresh register |
| 1 | 1 | Hi_thresh register |

CONVERSION REGISTER

The 16-bit register contains the result of the last conversion in binary twos complement format. Following reset or power-up, the Conversion register is cleared to '0', and remains '0' until the first conversion is completed.

The register format is shown in [Table 8](#).

CONFIG REGISTER

The 16-bit register can be used to control the ADS1015 operating mode, input selection, data rate, PGA settings, and comparator modes. The register format is shown in [Table 9](#).

Table 7. Pointer Register Byte (Write-Only)

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|------------------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | Register address | |

Table 8. Conversion Register (Read-Only)

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|
| NAME | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 0 | 0 | 0 | 0 |

Table 9. Config Register (Read/Write)

| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|------|-----|------|------|-----------|----------|----------|-------------|-------------|
| NAME | OS | MUX2 | MUX1 | MUX0 | PGA2 | PGA1 | PGA0 | MODE |
| | | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | DR2 | DR1 | DR0 | COMP_MODE | COMP_POL | COMP_LAT | COMP_QUEUE1 | COMP_QUEUE0 |

Default = 8583h.

| | |
|---------------------|--|
| Bit [15] | OS: Operational status/single-shot conversion start This bit determines the operational status of the device. This bit can only be written when in power-down mode. For a write status: 0 : No effect 1 : Begin a single conversion (when in power-down mode) For a read status: 0 : Device is currently performing a conversion 1 : Device is not currently performing a conversion |
| Bits [14:12] | MUX[2:0]: Input multiplexer configuration These bits configure the input multiplexer. 000 : AIN _P = AIN ₀ and AIN _N = AIN ₁ (default) 100 : AIN _P = AIN ₀ and AIN _N = GND 001 : AIN _P = AIN ₀ and AIN _N = AIN ₃ 101 : AIN _P = AIN ₁ and AIN _N = GND 010 : AIN _P = AIN ₁ and AIN _N = AIN ₃ 110 : AIN _P = AIN ₂ and AIN _N = GND 011 : AIN _P = AIN ₂ and AIN _N = AIN ₃ 111 : AIN _P = AIN ₃ and AIN _N = GND |
| Bits [11:9] | PGA[2:0]: Programmable gain amplifier configuration These bits configure the programmable gain amplifier. 000 : FS = ±6.144V ⁽¹⁾ 100 : FS = ±0.512V 001 : FS = ±4.096V ⁽¹⁾ 101 : FS = ±0.256V 010 : FS = ±2.048V (default) 110 : FS = ±0.256V 011 : FS = ±1.024V 111 : FS = ±0.256V |
| Bit [8] | MODE: Device operating mode This bit controls the current operational mode of the ADS1015. 0 : Continuous conversion mode 1 : Power-down single-shot mode (default) |
| Bits [7:5] | DR[2:0]: Data rate These bits control the data rate setting. 000 : 128SPS 100 : 1600SPS (default) 001 : 250SPS 101 : 2400SPS 010 : 490SPS 110 : 3300SPS 011 : 920SPS 111 : 3300SPS |
| Bit [4] | COMP_MODE: Comparator mode This bit controls the comparator mode of operation. It changes whether the comparator is implemented as a traditional comparator (COMP_MODE = '0') or as a window comparator (COMP_MODE = '1'). 0 : Traditional comparator with hysteresis (default) 1 : Window comparator |
| Bit [3] | COMP_POL: Comparator polarity This bit controls the polarity of the ALERT/RDY pin. When COMP_POL = '0' the comparator output is active low. When COMP_POL='1' the ALERT/RDY pin is active high. 0 : Active low (default) 1 : Active high |
| Bit [2] | COMP_LAT: Latching comparator This bit controls whether the ALERT/RDY pin latches once asserted or clears once conversions are within the margin of the upper and lower threshold values. When COMP_LAT = '0', the ALERT/RDY pin does not latch when asserted. When COMP_LAT = '1', the asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master, the device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line. 0 : Non-latching comparator (default) 1 : Latching comparator |
| Bits [1:0] | COMP_QUE: Comparator queue and disable These bits perform two functions. When set to '11', they disable the comparator function and put the ALERT/RDY pin into a high state. When set to any other value, they control the number of successive conversions exceeding the upper or lower thresholds required before asserting the ALERT/RDY pin. 00 : Assert after one conversion 01 : Assert after two conversions 10 : Assert after four conversions 11 : Disable comparator (default) |

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

Lo_thresh AND Hi_thresh REGISTERS

The upper and lower threshold values used by the comparator are stored in two 16-bit registers. These registers store values in the same format that the output register displays values; that is, they are stored in two's complement format. Because it is implemented as a digital comparator, special attention should be taken to readjust values whenever PGA settings are changed.

A secondary conversion ready function of the comparator output pin can be realized by setting the Hi_thresh register MSB to '1' and the Lo_thresh register MSB to '0'. However, in all other cases, the Hi_thresh register must be larger than the Lo_thresh register. The threshold register formats are shown in Table 10. When set to RDY mode, the ALERT/RDY pin outputs the state of the OS bit when in single-shot mode and pulses when in continuous conversion mode. Bits [3:0] in both the Lo_thresh and Hi_thresh registers have no effect on the comparator level thresholds. These bits should be considered as *don't care* bits.

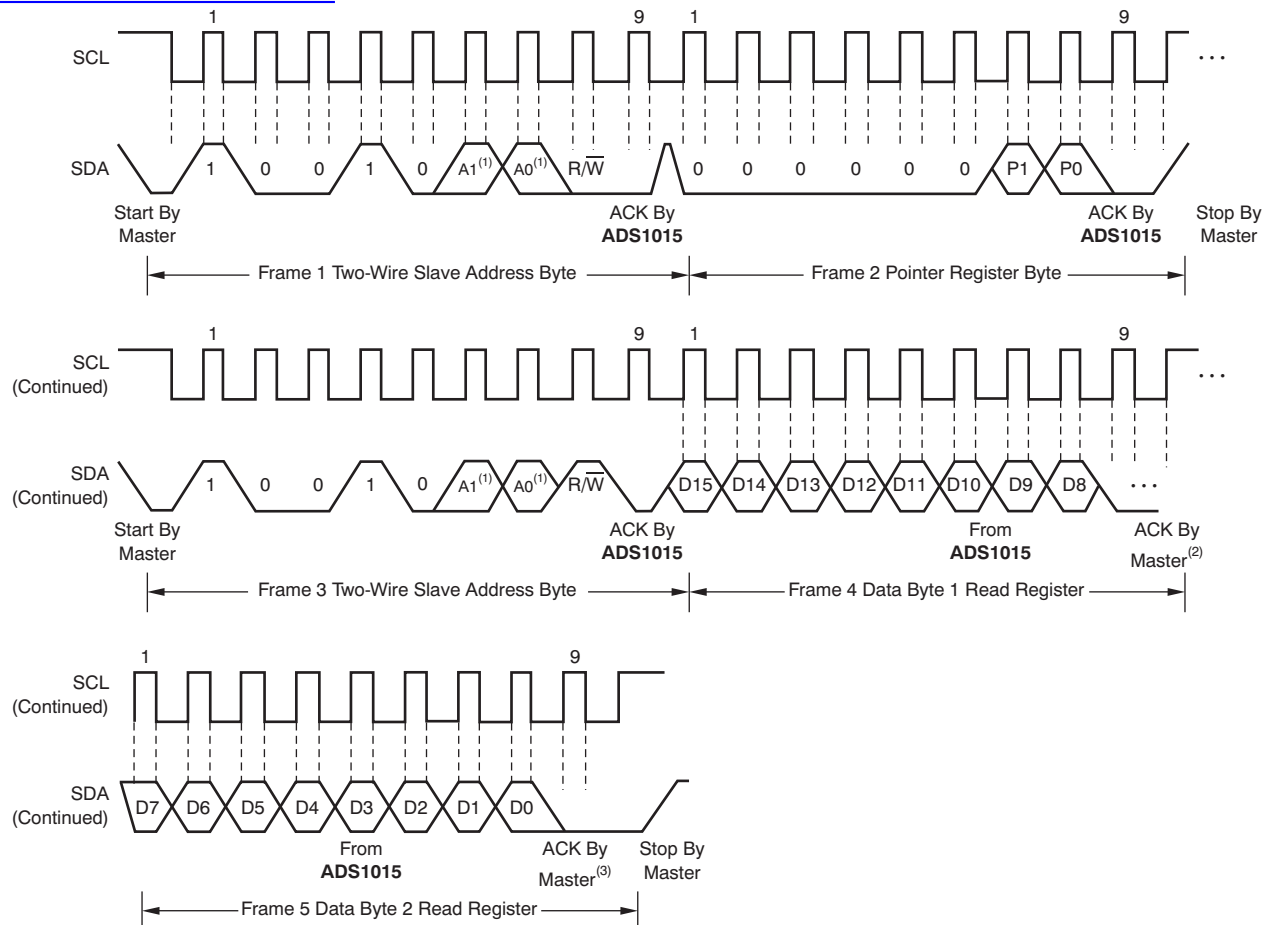
Table 10. Lo_thresh and Hi_thresh Registers

| REGISTER | Lo_thresh (Read/Write) | | | | | | | |
|----------|------------------------|-------------|------------|------------|------------|------------|------------|------------|
| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NAME | Lo_thresh11 | Lo_thresh10 | Lo_thresh9 | Lo_thresh8 | Lo_thresh7 | Lo_thresh6 | Lo_thresh5 | Lo_thresh4 |
| | | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | Lo_thresh3 | Lo_thresh2 | Lo_thresh1 | Lo_thresh0 | 0 | 0 | 0 | 0 |

| REGISTER | Hi_thresh (Read/Write) | | | | | | | |
|----------|------------------------|-------------|------------|------------|------------|------------|------------|------------|
| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NAME | Hi_thresh11 | Hi_thresh10 | Hi_thresh9 | Hi_thresh8 | Hi_thresh7 | Hi_thresh6 | Hi_thresh5 | Hi_thresh4 |
| | | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | Hi_thresh3 | Hi_thresh2 | Hi_thresh1 | Hi_thresh0 | 1 | 1 | 1 | 1 |

Lo_thresh default = 8000h.

Hi_thresh default = 7FFFh.



- (1) The values of A0 and A1 are determined by the ADDR pin.
 (2) Master can leave SDA high to terminate a single-byte read operation.
 (3) Master can leave SDA high to terminate a two-byte read operation.

Figure 16. Two-Wire Timing Diagram for Read Word Format

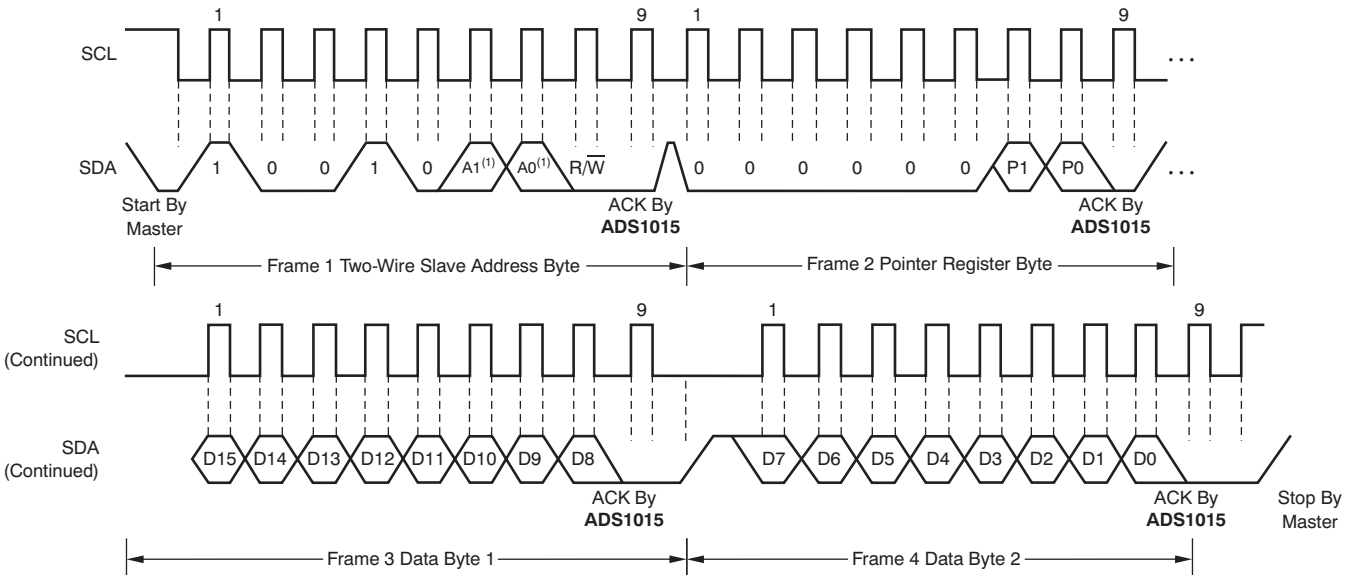


Figure 17. Two-Wire Timing Diagram for Write Word Format

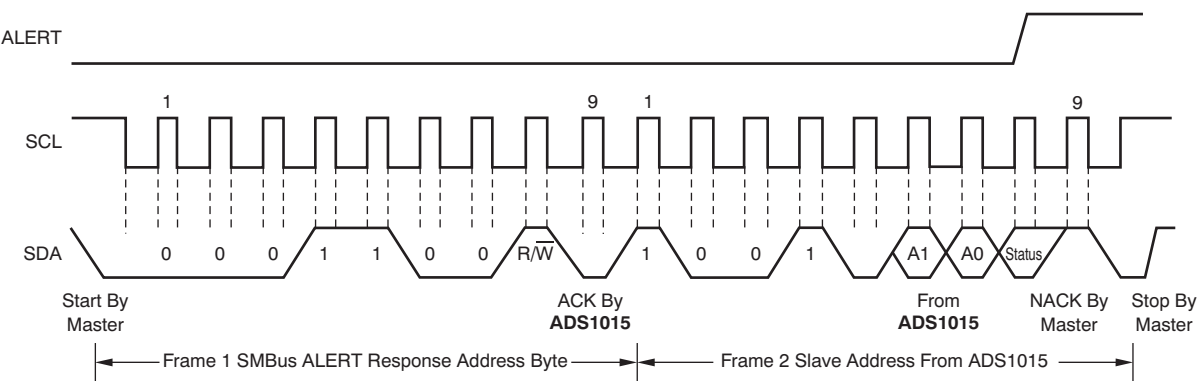


Figure 18. Timing Diagram for SMBus ALERT Response

APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1015 in various situations.

BASIC CONNECTIONS

For many applications, connecting the ADS1015 is simple. A basic connection diagram for the ADS1015 is shown in Figure 19.

The fully differential voltage input of the ADS1015 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS1015 can read bipolar differential signals, they cannot accept negative voltages on either input. It may be helpful to think of the ADS1015 positive voltage input as *noninverting*, and of the negative input as *inverting*.

When the ADS1015 is converting data, they draw current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1015 interfaces directly to standard mode, fast mode, and high-speed mode I²C controllers. Any microcontroller I²C peripheral, including master-only and non-multiple-master I²C peripherals, can operate with the ADS1015. The ADS1015 does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this function unless other clock-stretching devices are on the same I²C bus.

Pull-up resistors are required on both the SDA and SCL lines because I²C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

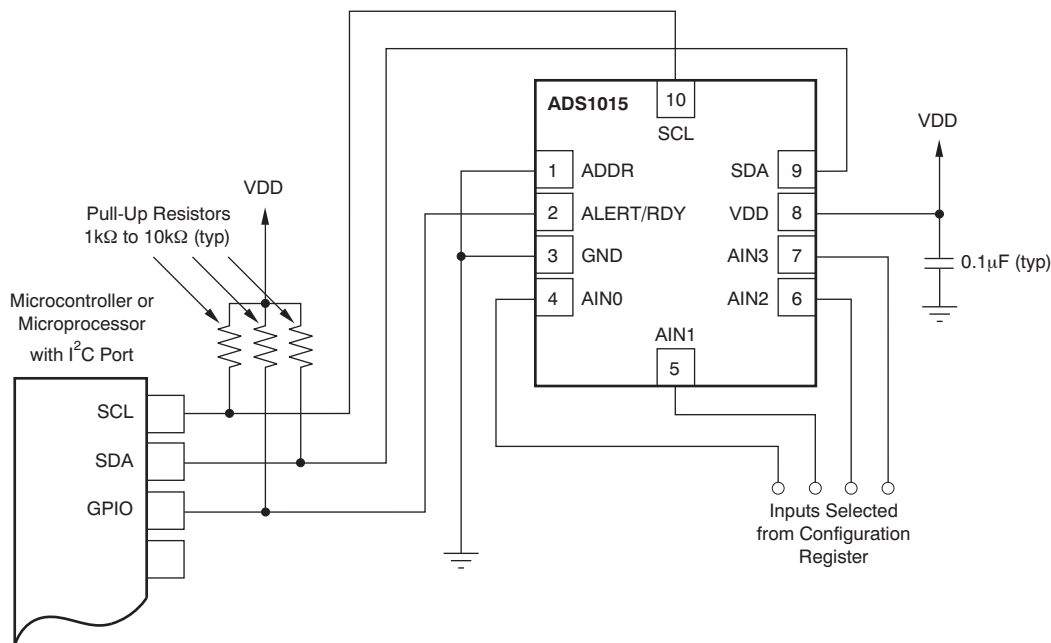


Figure 19. Typical Connections of the ADS1015

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1015s to a single bus is simple. Using the address pin, the ADS1015 can be set to one of four different I²C addresses. An example showing four ADS1015 devices is given in [Figure 21](#). Up to four ADS1015s (using different address pin configurations) can be connected to a single bus.

Note that only one set of pullup resistors is needed per bus. The pullup resistor values may need to be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

The [TMP421](#) and [DAC8574](#) devices detect the respective I²C bus addresses based on the states of pins. In [Figure 22](#), the [TMP421](#) has the address 0101010, and the [DAC8574](#) has the address 1001100. Consult the [DAC8574](#) and [TMP421](#) data sheets, available at www.ti.com, for further details.

USING GPIO PORTS FOR COMMUNICATION

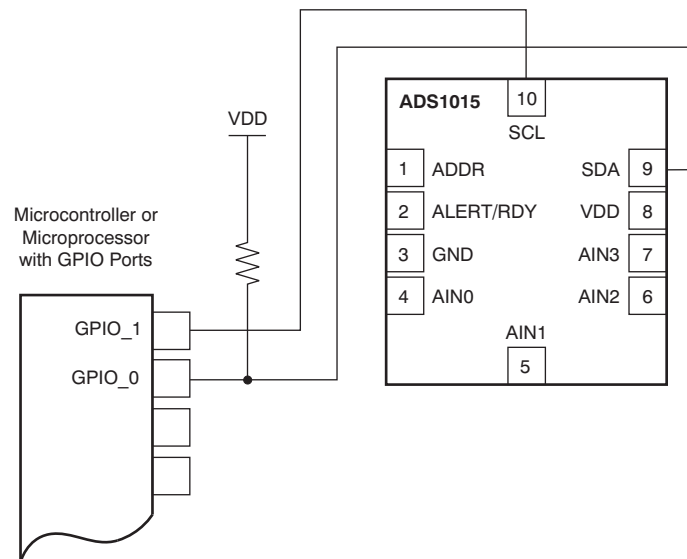
Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the ADS1015 can be connected to GPIO pins and the I²C bus protocol simulated, or *bit-banged*, in software. An example of this configuration for a single ADS1015 is shown in [Figure 20](#).

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to '0' and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this configuration reads as a '0' in the port input register.

Note that no pullup resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. This action is possible because the ADS1015 never drives the clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption as a result of the absence of a resistive pullup.

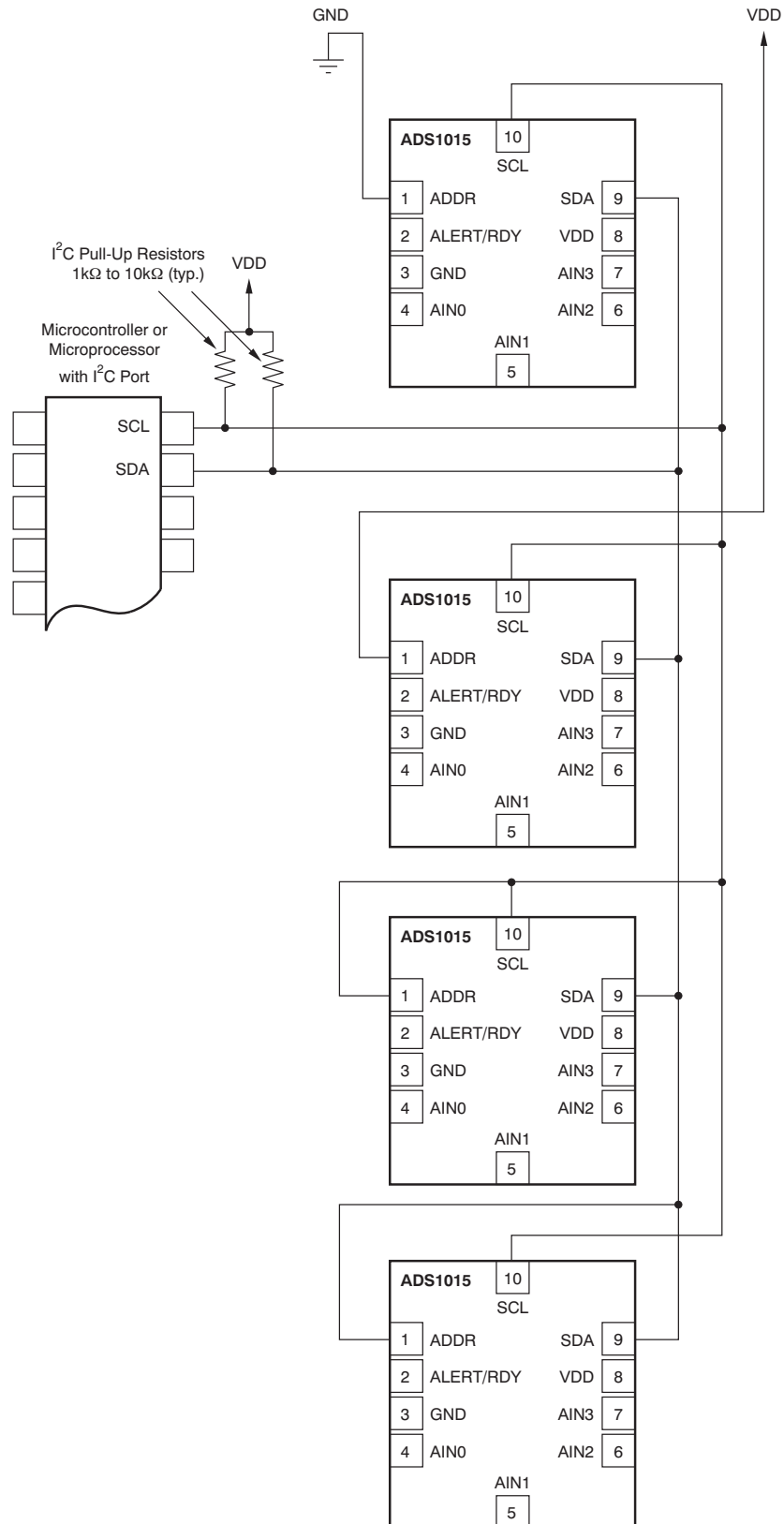
If there are any devices on the bus that may drive the clock lines low, this method should not be used; the SCL line should be high-Z or '0' and a pullup resistor provided as usual.

Some microcontrollers have selectable strong pullup circuits built in to the GPIO ports. In some cases, these circuits can be switched on and used in place of an external pullup resistor. Weak pullups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.



NOTE: ADS1015 power and input connections omitted for clarity.

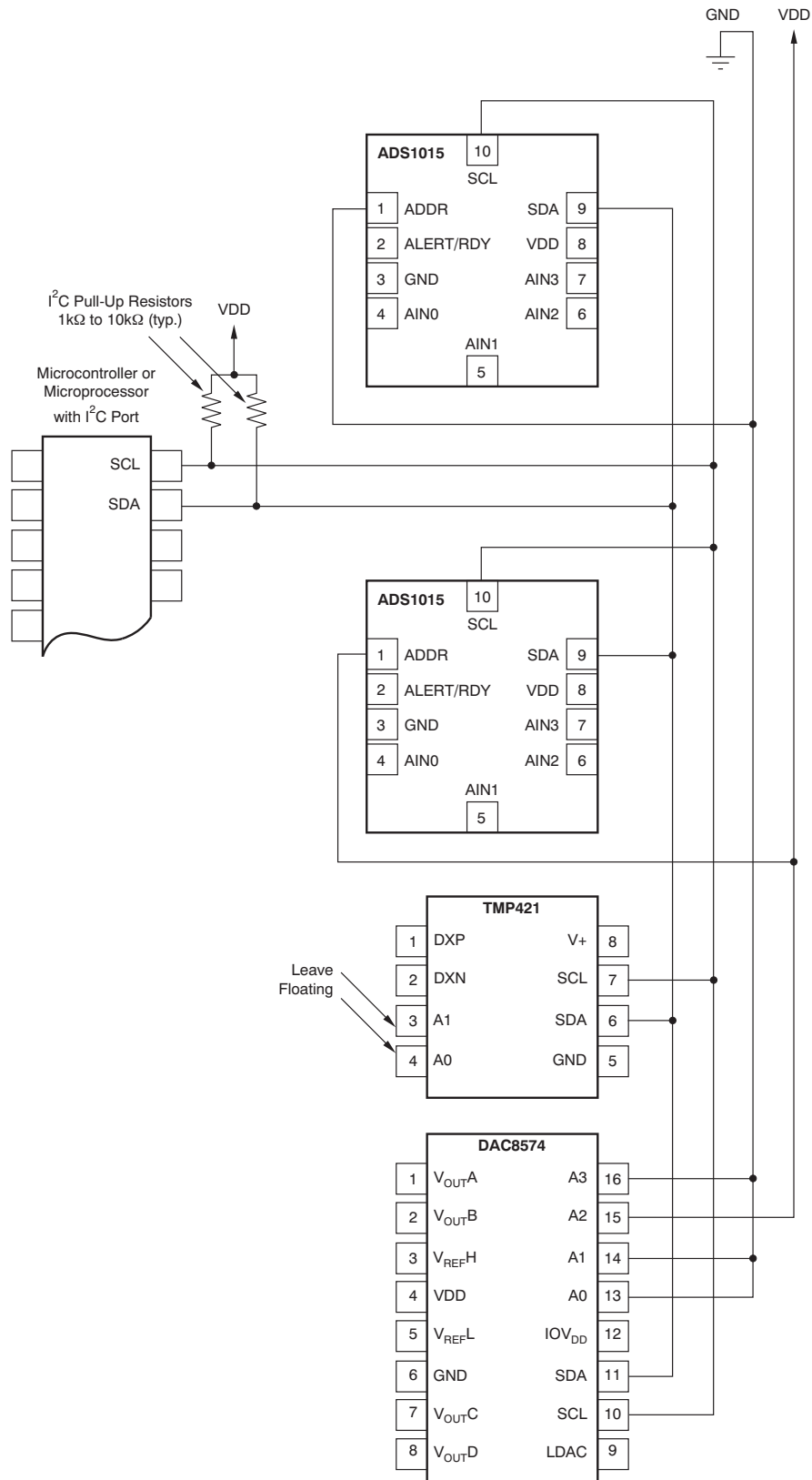
Figure 20. Using GPIO with a Single ADS1015



NOTE: ADS1015 power and input connections omitted for clarity. The ADDR pin selects the I²C address.

Figure 21. Connecting Multiple ADS1015s

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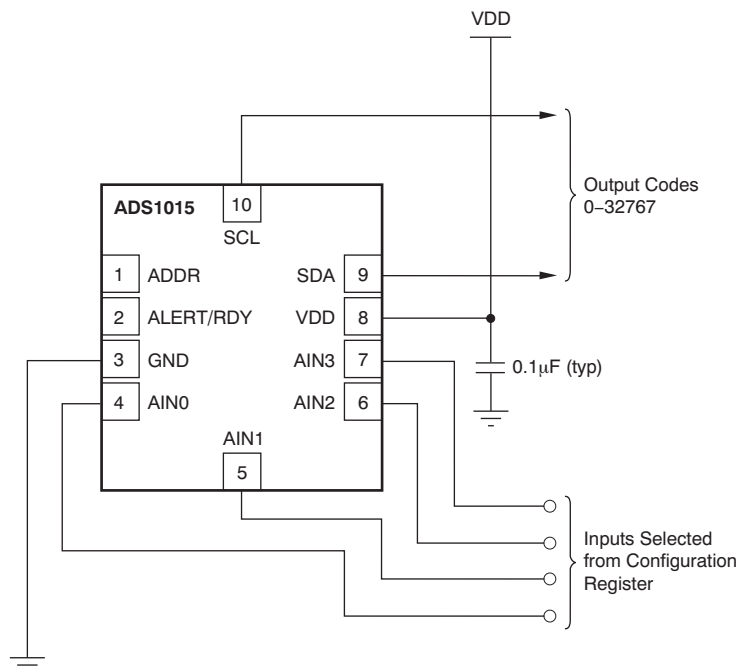
NOTE: ADS1015 power and input connections omitted for clarity. ADDR, A3, A2, A1, and A0 select the I²C addresses.

Figure 22. Connecting Multiple Device Types

SINGLE-ENDED INPUTS

Although the ADS1015 has two differential inputs, the device can easily measure four single-ended signals. Figure 23 shows a single-ended connection scheme. The ADS1015 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection on the configuration register. The single-ended signal can range from 0V to supply. The ADS1015 loses no linearity anywhere within the input range. Negative voltages cannot be applied to this circuit because the ADS1015 can only accept positive voltages.

The ADS1015 input range is bipolar differential with respect to the reference. The single-ended circuit shown in Figure 23 covers only half the ADS1015 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.



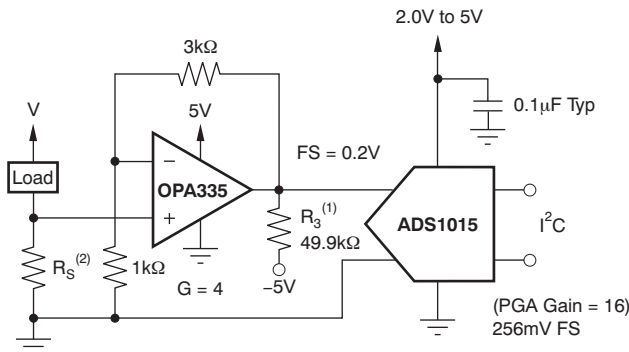
NOTE: Digital and address pin connections omitted for clarity.

Figure 23. Measuring Single-Ended Inputs

LOW-SIDE CURRENT MONITOR

Figure 24 shows a circuit for a low-side shunt-type current monitor. The circuit monitors the voltage across a shunt resistor, which is sized as small as possible while giving a measurable output voltage. This voltage is amplified by an OPA335 low-drift op amp, and the result is read by the ADS1015.

It is suggested that the ADS1015 be operated at a gain of 16. The gain of the OPA335 can then be set lower. For a gain of 16, the op amp should be set up to give a maximum output voltage no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1015 is 0.2V.



- (1) Pull-down resistor to allow accurate swing to 0V.
- (2) R_S is sized for a 50mV drop at full-scale current.

Figure 24. Low-Side Current Measurement

The ADS1015 is fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1015 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1015 analog inputs can withstand momentary currents as large as 100mA.

If the ADS1015 is driven by an op amp with high-voltage supplies, such as $\pm 12V$, protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps drift to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1015. This incremental damage results in slow, long-term failure, which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with an ADS1015, performance characteristics must be taken into account when designing the application.



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Pea |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|--------------|
| ADS1015QDGSRQ1 | ACTIVE | MSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-2600 |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com> for more information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all RoHS compliant products that contain no more than 0.1% by weight of lead in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in high temperature applications.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die attach material used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF ADS1015-Q1 :

- Catalog: [ADS1015](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS1015QDGSRQ1 | MSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

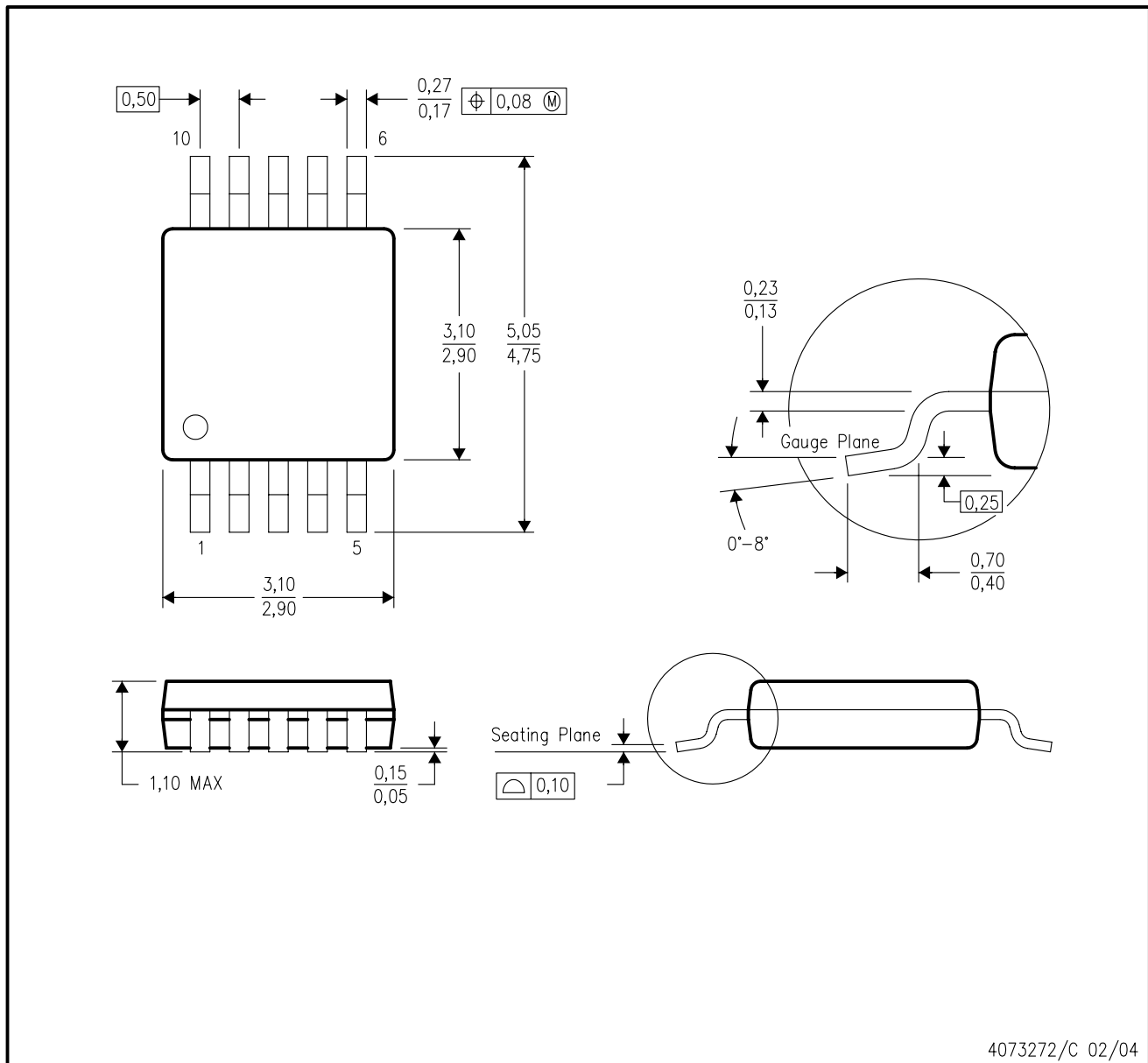


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS1015QDGSRQ1 | MSOP | DGS | 10 | 2500 | 370.0 | 355.0 | 55.0 |

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation BA.

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