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LH0082

Z80 CTC Counter Timer Circuit

Description

The Z80 product line is a complete set of micro-computer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

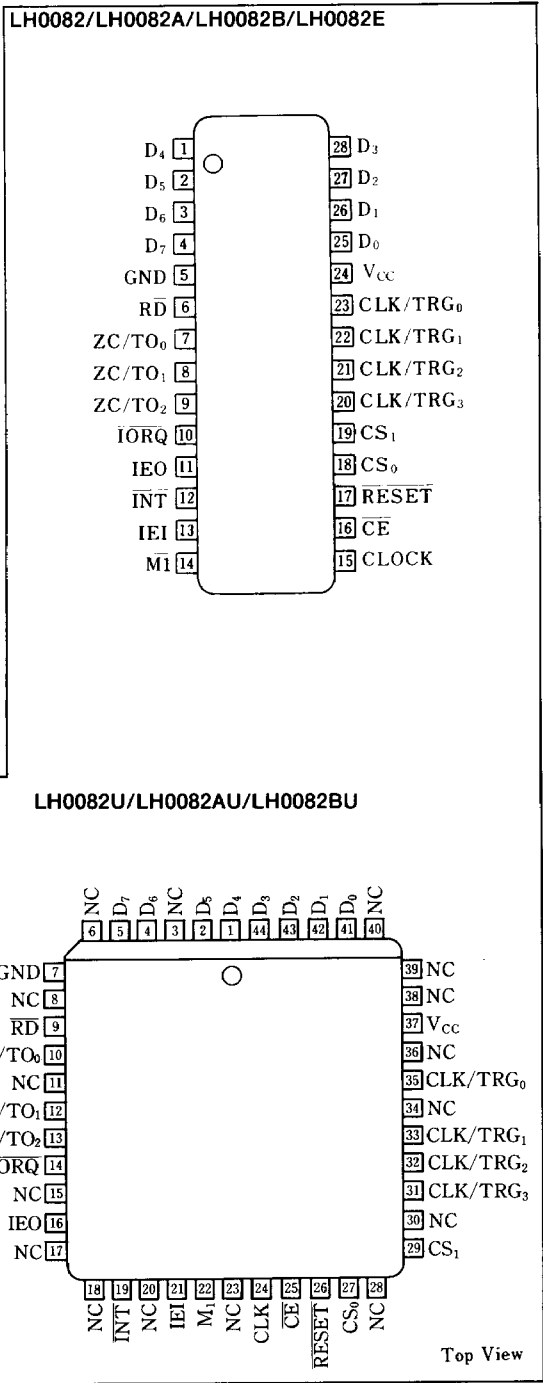
The LH0082 Z80 CTC (Z80 CTC for short below) is a programmable, four channel device that provides counting and timing functions for the Z80 CPU. The Z80 CPU configures the Z80 CTC's four independent channels to operate under various modes and conditions as required.

The LH0082A Z80A and LH0082B Z80B CTC are the high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

Features

- 1. Four independent programmable 8-bit counter/16-bit timer channels
- 2. N-channel silicon gate process
- 3. Each channel may be selected to operate in either a counter mode or timer mode

Pin Connections



* The GND pins must be connected to the GND level.

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4. Programmable interrupts on counter or timer states

5. When the down-counter reaches the zero count the CTC reloads its time constant automatically and continues it's channel operation

6. Readable down counter

7. Selectable 16 or 256 clock prescaler for each timer channels

8. Selectable positive or negative trigger may initiate timer or counter operation
9. Three channels have ZC/TO outputs capable of driving Darlington transistors

10. Vectored daisy chain priority interrupt logic included

11. Single +5V power supply and single phase clock

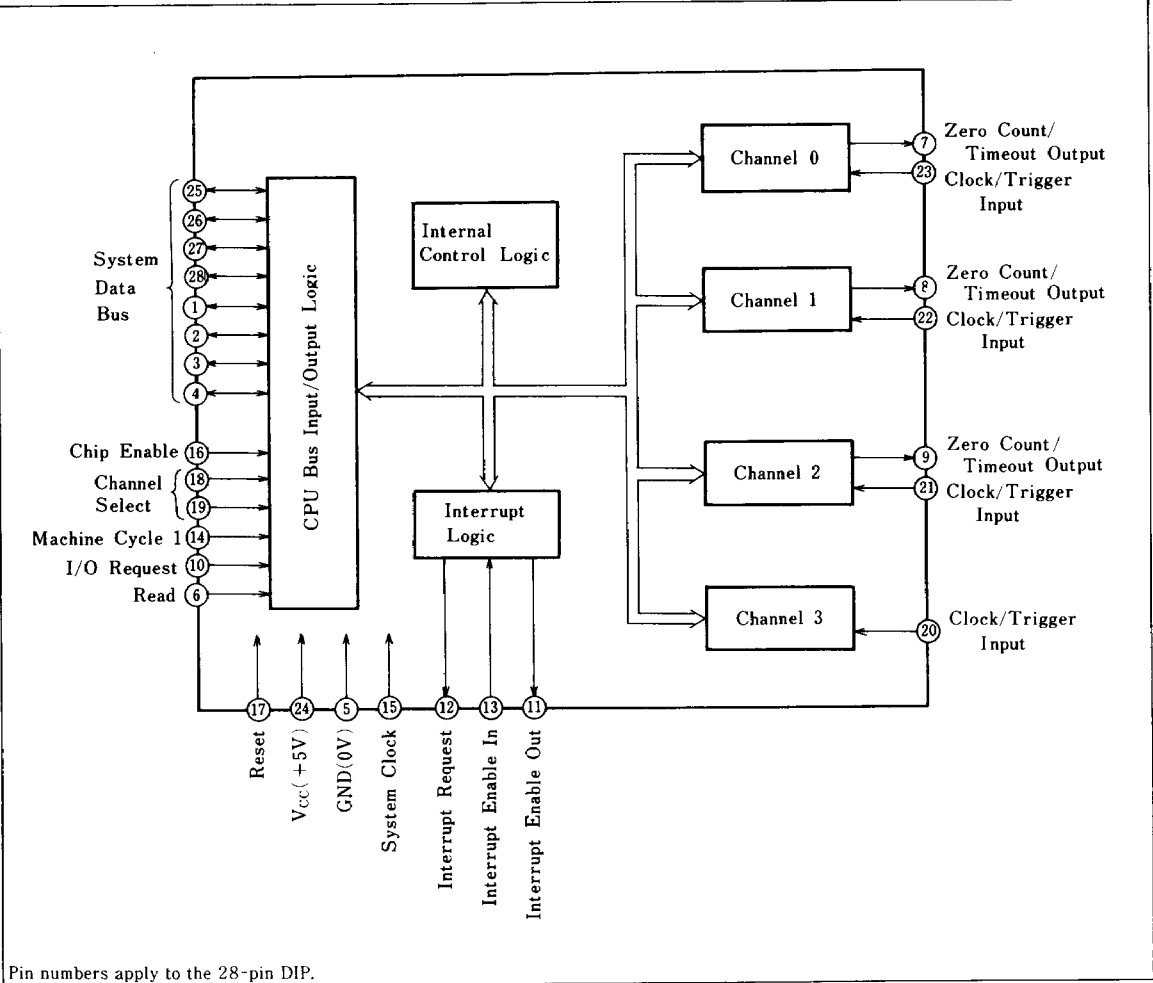
12. All inputs and outputs fully TTL compatible

13. 28-pin DIP (DIP28-P-600)
44-pin QFP (QFP44-P-1010A)
44-pin QFJ (QFJ44-P-S650)

Ordering Information

Product	Z80 CTC	Z80A CTC	Z80B CTC	Z80E CTC	Package	Operating temperature
Clock frequency	2.5MHz	4MHz	6MHz	8MHz		
Model No.	LH0082	LH0082A	LH0082B	LH0082E	28-pin DIP	0°C to +70°C
	LH0082M	LH0082AM			44-pin QFP	0°C to +60°C
	LH0082U	LH0082AU	LH0082BU		44-pin QFJ	0°C to +70°C

Block Diagram



Pin Description

Pin	Meaning	I/O	Function
D ₀ -D ₇	Data bus	Bidirectional 3-state	System data bus.
CS ₀ , CS ₁	Channel select	I	Selects one of the four independent channels.
$\overline{\text{CE}}$	Chip enable	I	Active "Low". A Low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{\text{M1}}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both M1 and IORQ are active.
$\overline{\text{IORQ}}$	I/O request	I	Active "Low". Read operation when RD is active, and write operation when it is not active. Indicates the CPU is acknowledging an interrupt, when both $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ are active.
RD	Read cycle status	I	Active "Low". Read operation when active.
IEI	Interrupt enable in	I	Active "High". Forms a priority-interrupt daisy-chain.
IEO	Interrupt enable out	O	Active "High". Forms a priority-interrupt daisy-chain.
$\overline{\text{INT}}$	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
RESET	Reset	I	Active "Low". Resets the interrupt bits.
CLK/TRG ₀ -CLK/TRG ₃	External clock/timer trigger input	I	Counter/timer input for four independent channels.
ZC/TO ₀ -ZC/TO ₂	External clock/timer trigger out	O	Active "High". 0/1/2 output for four independent channels. No output terminal at channel 3.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V _{IN}	-0.3 to +7.0	V	
Output voltage	V _{OUT}	-0.3 to +7.0	V	
Operating temperature	T _{opr}	0 to +70	°C	1
Storage temperature	T _{stg}	-65 to +150	°C	

Note 1: T_{opr}=0 to +60°C for 44-pin QFP.

DC Characteristics

(V_{CC}=5V±5%, Ta=0 to +70°C^{Note 1})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V _{ILC}		-0.3		0.45	V
Clock input high voltage	V _{IHC}		V _{CC} -0.6		V _{CC} +0.3	V
Input low voltage	V _{IL}		-0.3		0.8	V
Input high voltage	V _{IH}		2.0		V _{CC}	V
Output low voltage	V _{OL}	I _{OL} =2mA			0.4	V
Output high voltage	V _{OH}	I _{OH} =-250μA	2.4			V
Supply current	I _{CC}	t _c =400ns			120	mA
Input leakage current	I _{LI}	0≤V _{IN} ≤V _{CC}			10	μA
3-state output leakage current	I _{LOH}	2.4V≤V _{OUT} ≤V _{CC}			10	μA
3-state output leakage current	I _{LOL}	V _{OUT} =0.4V			10	μA
Darlington drive current	I _{OHD}	V _{OH} =1.5V, R _{EXT} =390Ω	-1.5			mA

Note 1: Ta=0 to +60°C for 44-pin QFP.

Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C _{CLOCK}	Unmeasured pins returned to ground			20	pF
Input capacitance	C _{IN}				5	pF
Output capacitance	C _{OUT}				10	pF

SHARP

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AC Characteristics

($V_{CC} = 5V \pm 5\%$, $T_a = 0$ to $+70^\circ\text{C}$)

No.	Parameter	Symbol	LH0082		LH0082A		LH0082B		LH0082E		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	Clock cycle time	T_{cC}	400	(Note 1)	250	(Note 1)	165	(Note 1)	125	(Note 1)	ns	
2	Clock width (high)	T_{wCh}	170	2000	105	2000	65	2000	55	2000	ns	
3	Clock width (low)	T_{wCl}	170	2000	105	2000	65	2000	55	2000	ns	
4	Clock fall time	T_{fC}		30		30		20		10	ns	
5	Clock rise time	T_{rC}		30		30		20		10	ns	
6	All hold times	T_h	0		0		0		0		ns	
7	CS to clock $\uparrow$ setup time	$T_{sCS} (C)$	250		160		100		80		ns	
8	CE to clock $\uparrow$ setup time	$T_{sCE} (C)$	200		150		100		75		ns	
9	$\text{IORQ} \uparrow$ to clock $\uparrow$ setup time	$T_{sIO} (C)$	250		115		70		60		ns	
10	$\text{RD} \downarrow$ to clock $\uparrow$ setup time	$T_{sRD} (C)$	240		115		70		60		ns	
11	Clock $\uparrow$ to data out delay	$T_{dC} (DO)$		240		200		130		100	ns	2
12	Clock $\downarrow$ to data out float delay	$T_{dC} (DOz)$		230		110		90		75	ns	
13	Data in to clock $\uparrow$ setup time	$T_{sDI} (C)$	60		50		40		30		ns	
14	$M\bar{I}$ to clock $\uparrow$ setup time	$T_{sMI} (C)$	210		90		70		55		ns	
15	$M\bar{I} \downarrow$ to IEO $\downarrow$ delay (interrupt immediately preceding $M\bar{I}$)	$T_{dMI} (IEO)$		300		190		130		90	ns	3
16	$\text{IORQ} \downarrow$ to data out delay (INTA cycle)	$T_{dIO} (DOI)$		340		160		110		80	ns	2
17	$\text{IEI} \downarrow$ to IEO $\downarrow$ delay	$T_{dIEI} (IEOf)$		190		130		100		80	ns	3
18	$\text{IEI} \uparrow$ to IEO $\uparrow$ delay (after ED decode)	$T_{dIEI} (IEOr)$		220		160		110		80	ns	3
19	Clock $\uparrow$ to INT $\downarrow$ delay	$T_{dC} (INT)$		$T_{cC}+200$		$T_{cC}+140$		$T_{cC}+120$		$T_{cC}+100$	ns	4
20	CLK/TRG $\uparrow$ to INT $\downarrow$ delay tsCTR (C) satisfied	$T_{dCLK} (INT)$		$T_{cC}+230$		$T_{cC}+160$		$T_{cC}+130$		$T_{cC}+110$	ns	5
	CLK/TRG $\uparrow$ to INT $\downarrow$ delay tsCTR (C) not satisfied			$2T_{cC}+530$		$2T_{cC}+370$		$2T_{cC}+280$		$2T_{cC}+190$	ns	5
21	CLK/TRG cycle time	T_{sCTR}	$2T_{cC}$		$2T_{cC}$		$2T_{cC}$		$2T_{cC}$		ns	5
22	CLK/TRG rise time	T_{rCTR}		50		50		40		35	ns	
23	CLK/TRG fall time	T_{fCTR}		50		50		40		35	ns	
24	CLK/TRG width (low)	T_{wCTRl}	200		200		120		100		ns	
25	CLK/TRG width (high)	T_{wCTRh}	200		200		120		100		ns	
26	CLK/TRG $\uparrow$ to clock $\uparrow$ setup time for immediate count	$T_{sCTR} (Cs)$	300		210		150		110		ns	5
27	CLK/TRG $\uparrow$ to clock $\uparrow$ setup time for enabling of prescaler on following clock $\uparrow$	$T_{sCTR} (Ct)$	210		210		150		110		ns	4
28	Clock $\uparrow$ to ZC/TO $\uparrow$ delay	$T_{dC} (ZC/TO\uparrow)$		260		190		140		110	ns	
29	Clock $\downarrow$ to ZC/TO $\downarrow$ delay	$T_{dC} (ZC/TO\downarrow)$		190		190		140		110	ns	

$\uparrow$ Rising edge, $\downarrow$ falling edge

$T_a = 0$ to $+60^\circ\text{C}$ for 44-pin QFP

[A] $2.5 T_{cC} > (n-2) T_{dIEI} (IEOf) + T_{dMI} (IEO) + T_{sIEI} (IO) + \text{TTL buffer delay, if any.}$

[B] RESET must be active for a minimum of 3 clock cycles.

Note 1 : $T_{cC} = T_{wCh} + T_{wCl} + T_{rC} + T_{fC}$.

Note 2 : Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines, and 100 pF for control lines.

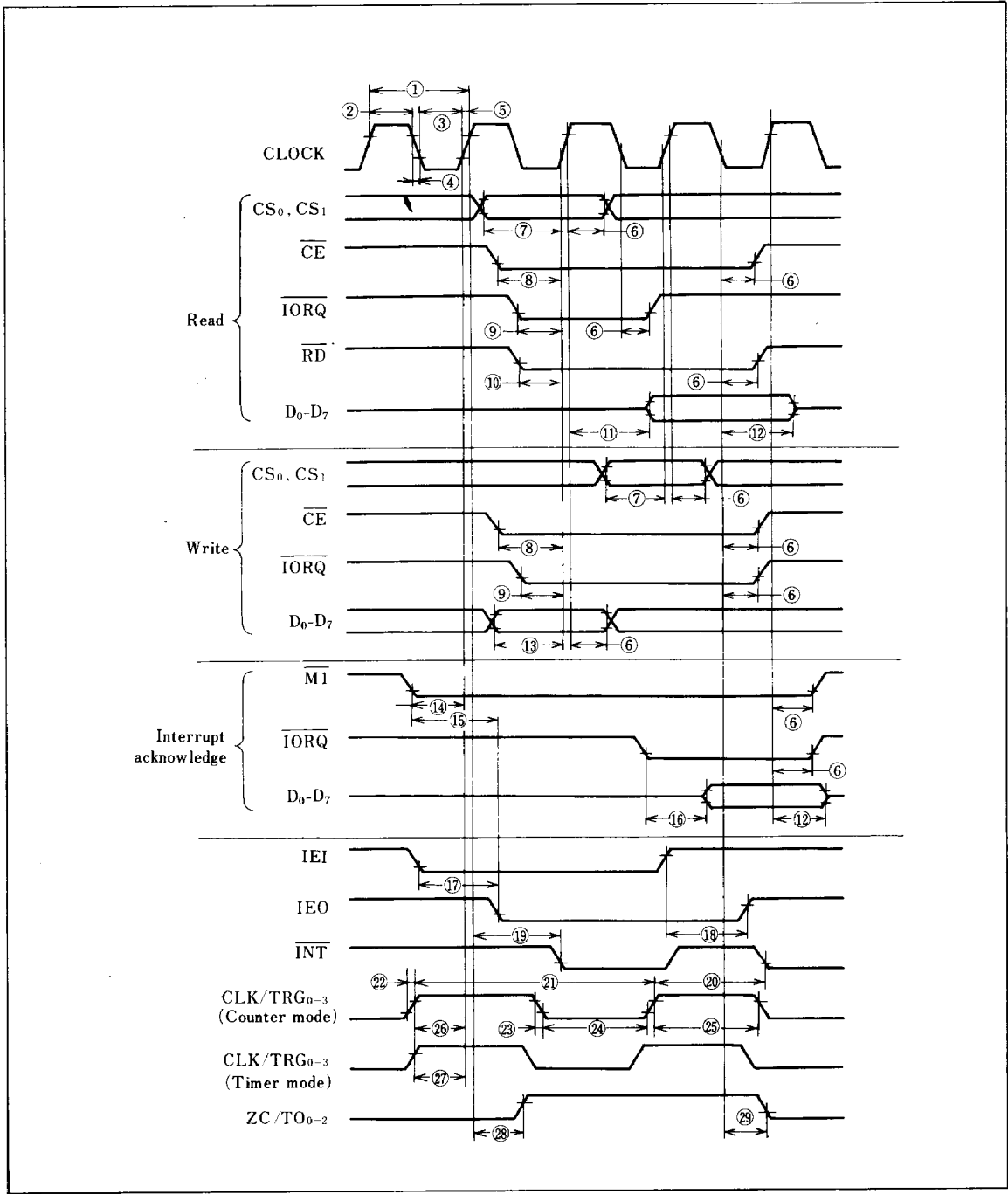
Note 3 : Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum.

Note 4 : Timer mode.

Note 5 : Counter mode.

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AC Timing Chart



5

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■ Programming

(1) Operation mode select

To select a channel operating mode, write a channel control word having bit 0 changed to 1 in the channel control register.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Interrupt enable	Mode	Pre-scaler value	CLK/TRO edge selection	Trigger mode	Time constant mode	Reset	1

D₃ and D₅ are used in timer mode only.

- Bit 7 = 0: Disables a channel interrupt.
- Bit 7 = 1: Enables a channel interrupt each time the down-counter counts down to zero. No interrupt is produced even with bit 7 as 1, after the counter has counted down to zero with bit 7 as 0.
- Bit 6 = 0: Selects the timer mode, having the prescaler output as the down-counter clock. The timer's period comes in $t_c \cdot P \cdot TC$. Where t_c represents system clock period, P has 16 or 256 (divisional scale by the prescaler), and TC means an 8-bit programmable time constant (max. 256).
- Bit 6 = 1: Selects the counter mode, having the external clock (CLK input) signal as the down-counter clock. The prescaler is not used.
- Bit 5 = 0: Used for the timer mode only. The prescaler divides the system clock into 16 sections.
- Bit 5 = 1: Used for the timer mode only. The prescaler divides the system clock into 256 sections.
- Bit 4 = 0: Starts the timer operation at the trigger input falling edge in the timer mode. In the counter mode, the down-counter comes on at the clock input rising edge.
- Bit 4 = 1: Starts the timer operation at the trigger input rising edge in the timer mode. In the counter mode, the down-counter comes on at the clock input rising edge.
- Bit 3 = 0: Effective in the timer mode only. With bit 1=1, the timer starts at the rising edge of the machine cycle T_2 which is next to the write cycle of a time constant. With bit 1=0, the timer starts at the rising edge of the machine cycle T_1 which is next to the write cycle of this control information.
- Bit 3 = 1: Effective in the timer mode only. The timer starts by an external trigger input that is given after the rising of the machine cycle T_2 next to the write cycle of a time constant.

The operation starts at the second clock rising if the trigger input meets the set-up time, and at the third clock rising if it does not. If an external trigger input is given before writing a time constant the condition of bit 3 = 0 is caused.

- Bit 2 = 0: Indicates that there is no time constant written after the channel control word. This bit cannot be 0 for the channel control word to be immediately given when the channel is reset.
- Bit 2 = 1: Indicates that there is a time constant written after the channel control word. When a time constant is written during a down-counter operation, the new constant is set into the time constant register. But the counter keeps on counting. Once the counter counts zero, the new constant is available to use.
- Bit 1 = 0: The channel acts as a down-counter.
- Bit 1 = 1: Stops the operation as a down-counter. With bit 2 = 1, the operation restarts after a time constant is written. With bit 2 = 0, the channel does not act until a new control word is given.

(2) Time constant programming

An 8-bit time constant is written into the time constant register, following the channel control word with bit 2 = 1. "00" (hexadecimal) indicates the time constant 256.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
TC ₇	TC ₆	TC ₅	TC ₄	TC ₃	TC ₂	TC ₁	TC ₀

(3) Interrupt vector programming

If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D₀ of the vector word is always zero, to distinguish the vector from a channel control word. D₁ and D₂ are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector. Channel 0 has the highest priority.

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D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
V ₇	V ₆	V ₅	V ₄	V ₃	V ₂	V ₁	V ₀

D ₂	D ₁	Channel
0	0	0
0	1	1
1	0	2
1	1	3

■ Timing

(1) Write cycle timing

Fig. 1 shows write cycle timing for loading control, time constant or vector words.

The CTC does not have a write signal input, so it generates one internally when the read ($\overline{RD}$) input is High during T_1 . During T_2 $\overline{IORQ}$ and $\overline{CE}$ inputs are Low. $\overline{M1}$ must be High to distinguish a write cycle from an interrupt acknowledge. A 2-bit binary code at inputs CS_1 and CS_0 selects the channel to be addressed, and the word being written is placed on the Z-80 data bus. The data word is latched into the appropriate register with the rising edge of clock cycle T_3 .

(2) Read cycle timing

Fig. 2 shows read cycle timing. This cycle reads the contents of a down-counter without disturbing the count.

During clock cycle T_2 , the Z-80 CPU initiates a read cycle by driving the following inputs Low: $\overline{RD}$, $\overline{IORQ}$, and $\overline{CE}$. A 2-bit binary code at inputs CS_1

and CS_0 selects the channel to be read. $\overline{M1}$ must be High to distinguish this cycle from an interrupt acknowledge. No additional wait states are allowed.

(3) Interrupt acknowledge timing

Fig. 3 shows interrupt acknowledge timing. After an interrupt request, the Z-80 CPU sends an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). All channels are inhibited from changing their interrupt request status when $\overline{M1}$ is active—about two clock cycles earlier than $\overline{IORQ}$. $\overline{RD}$ is High to distinguish this cycle from an instruction fetch.

The CTC interrupt logic determines the highest priority channel requesting an interrupt. If the CTC interrupt enable input ($\overline{IEI}$) is High, the highest priority interrupting channel within the CTC places its interrupt vector on the data bus when $\overline{IORQ}$ goes Low. Two wait states (T_{WA}) are automatically inserted at this time to allow the daisy chain to stabilize. Additional wait states may be added.

(4) Return from interrupt cycle

If a Z-80 peripheral has no interrupt pending and is not under service, then its $\overline{IEO} = \overline{IEI}$. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its $\overline{IEO}$ is always Low, inhibiting lower priority devices from interrupting. If it has an interrupt pending which has not yet been acknowledged, $\overline{IEO}$ is Low unless an "ED" is decoded as the first byte of a 2-byte opcode. In this case, $\overline{IEO}$ goes High until the next opcode byte is decoded, whereupon it goes Low again. If the second byte of the opcode

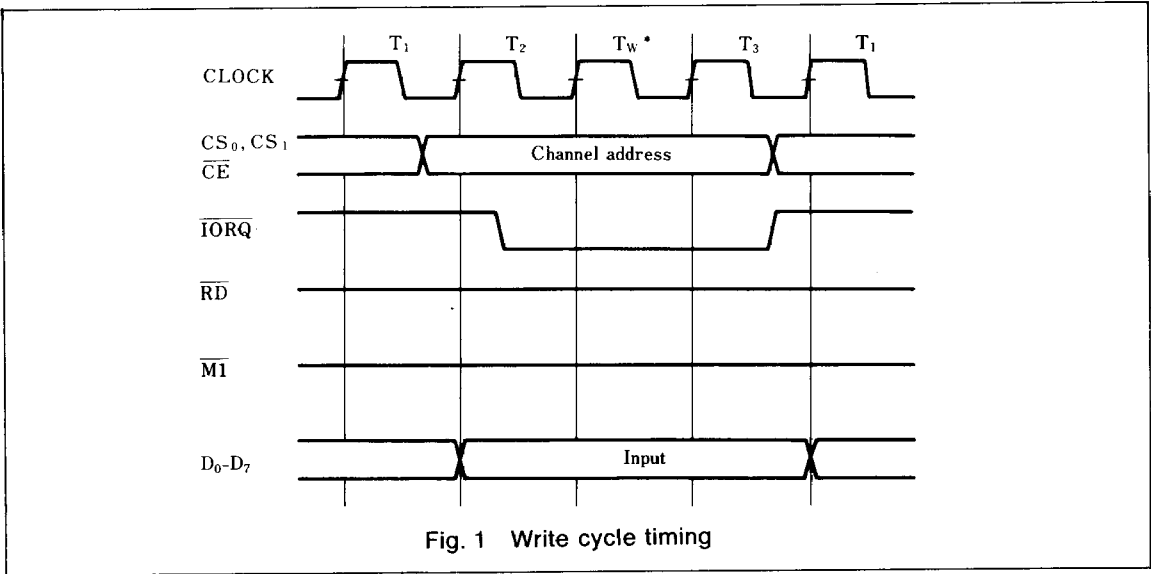


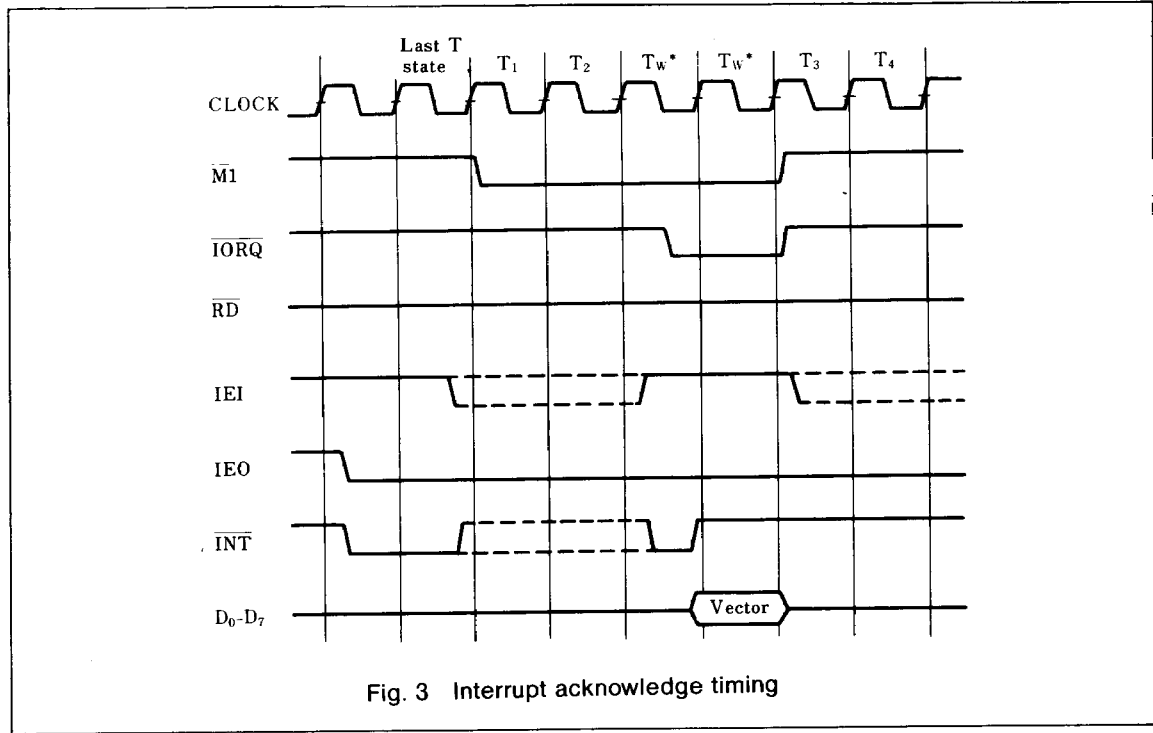
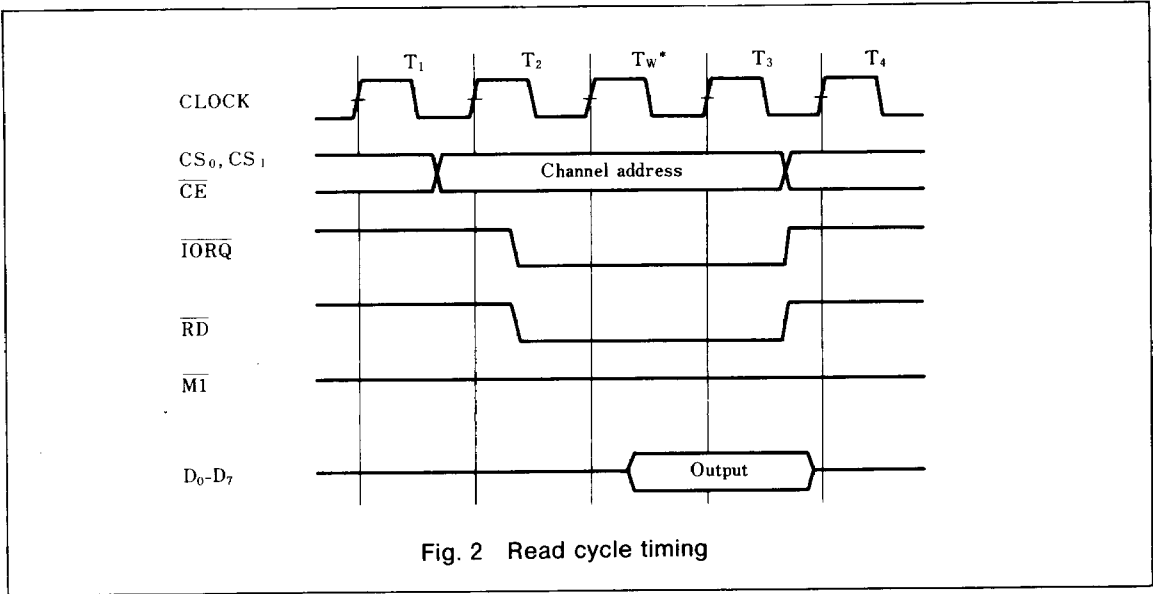
Fig. 1 Write cycle timing

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was a "4D," then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service has its IEI High and its IEO Low. This device is the highest-priority device

in the daisy chain that has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D", this peripheral device resets its "interrupt under service" condition.



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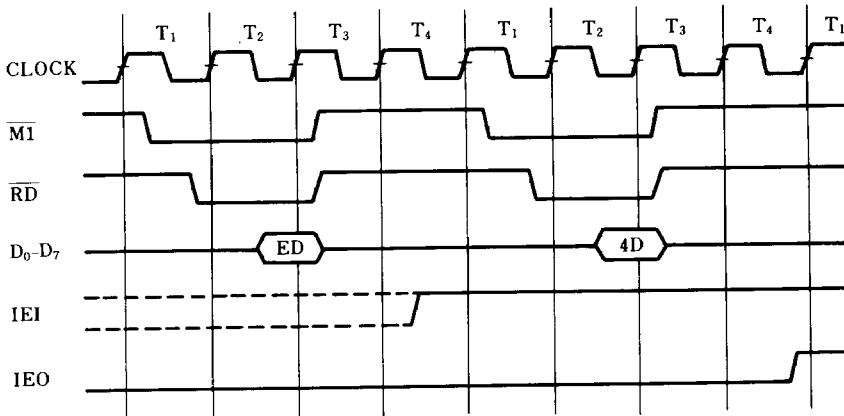


Fig. 4 Return from interrupt cycle

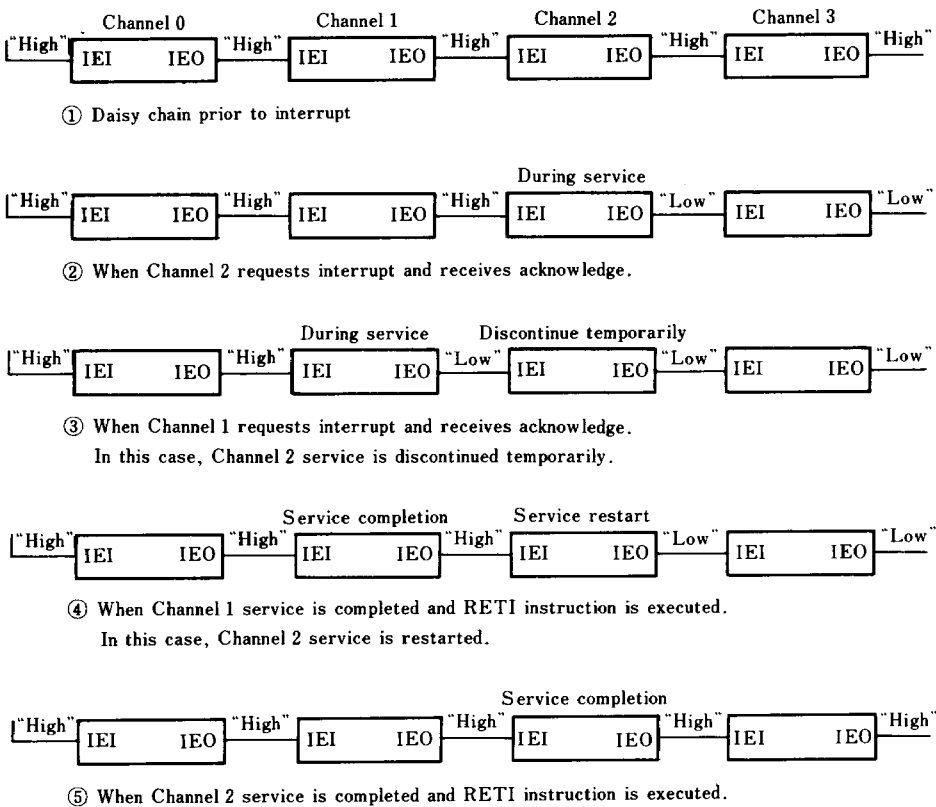


Fig. 5 Daisy-chain interrupt service

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(5) Daisy-chain interrupt service

Fig. 5 shows a typical nested interrupt order with the CTC. Channel 2 first requests an interrupt to be serviced. If the higher-priority Channel 1 requests an interrupt while Channel 2 is in service, the Channel 2 service is interrupted and Channel 1 is serviced instead. Now the Channel 1 service routine has been completely executed, an RETI instruction can be given to indicate that Channel 1 has been serviced. At this moment, Channel 2 will be in service again.

(6) Counter operation/timer operation

In the counter mode, the CLK/TRG pulse input decrements the down-counter. The trigger is asynchronous, but the count is synchronized with CLK. For the decrement to occur on the next rising edge of CLK, the trigger edge must precede CLK by a minimum lead time. In the timer mode, a CLK/TRG pulse input starts the timer on the second succeeding rising edge of CLK. The trigger pulse is asynchronous, and it must have a minimum width. A minimum lead time (210 ns) is required between the active edge of the CLK/TRG and the next rising edge of CLK to enable the prescaler on the following clock edge.

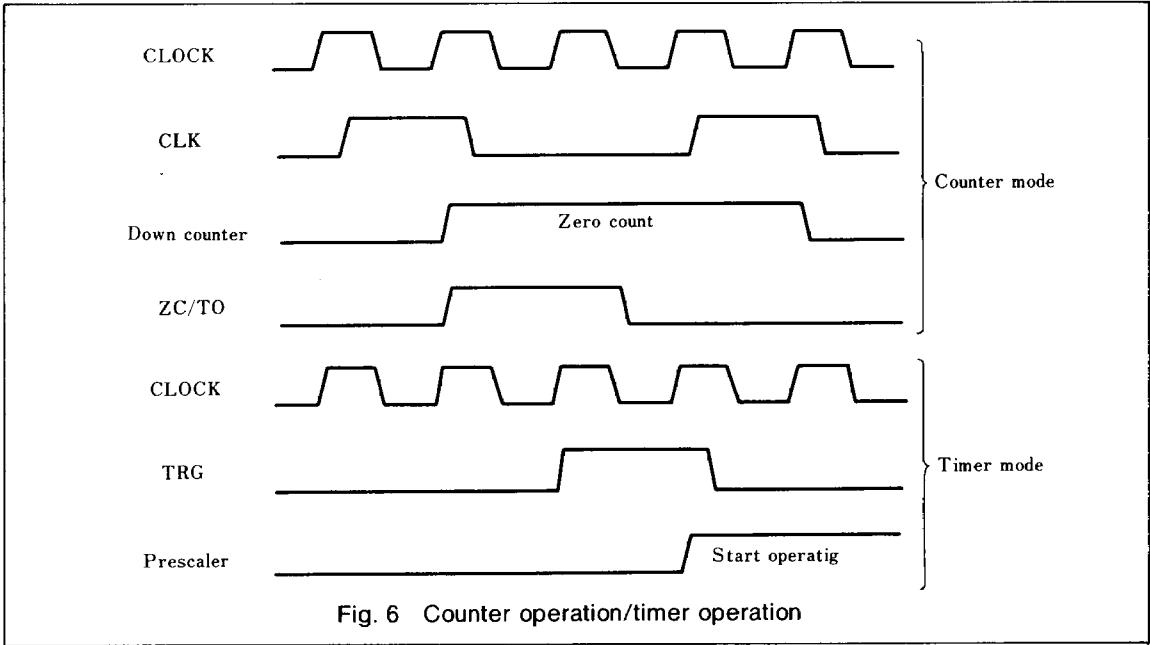


Fig. 6 Counter operation/timer operation