Document Number: MMM7010
Rev. 3.6, 7/2010

# MMM7010

# MMM7010

## GSM/GPRS/EDGE Transceiver

**Package Information**
Plastic Package
Case 1737-02
(5.2 x 6.8 mm)

**Ordering Information**

| Device Marking | Operating Temperature Range | Package |
|---|---|---|
| MMM7010 | -30 °C to 85 °C | LGA |

## 1 Introduction

The MMM7010 is a highly integrated transceiver that supports the GSM, GPRS and EDGE standards and provides antenna-to-digital-bits functionality in a 5.2 mm×6.8 mm land grid array (LGA) package. The transceiver functions include the GSM 850, EGSM 900, DCS 1800, and PCS 1900 transmit and receive frequency bands.

The MMM7010 transceiver includes a very low intermediate frequency (VLIF) receiver architecture with integrated low noise amplifiers (LNAs) and a polar modulation transmit architecture with direct phase modulation of the VCO by a fractional-N synthesizer. Both the Rx and Tx VCOs are fully integrated. The polar architecture allows for a filter-free transmit lineup. An internal layer 1 timing controller generates appropriate timing events for the transmitter calibration and the EDGE/GMSK transmit/receive burst, therefore, limiting the RF hardware dependency of the baseband layer 1 engine software to an absolute minimum. The MMM7010 uses the DigRF standard interface to the baseband processor, allowing maximum industry compatibility.

### Contents

1 Introduction . . . . . 1
2 Functional Block Diagram . . . . . 3
3 Functional Description . . . . . 3
4 Electrical Characteristics . . . . . 5
5 Programming . . . . . 11
6 Signal Descriptions . . . . . 16
7 Package Information . . . . . 19
8 Product Documentation . . . . . 21



freescale™
semiconductor

The MMM7010 transceiver includes the following features:

- Quad-band: GSM850, EGSM900, DCS1800, PCS1900
- EGPRS class 0–12 and 30–39 operation
- 36 $mm^2$ foot print
- Single regulated power supply capable
- High level of integration for extremely low external parts count (less than 5)
- Very low intermediate frequency (VLIF) receiver for EDGE and GPRS
- Simplified layer 1 programming model
- Digital interface with DigRF option
- Polar architecture achieves filter-free Tx lineup
- Frequency corrected clock option
- Auto-calibrated transmitter
- High immunity to remodulation
- Simplified automatic frequency correction (AFC)
- Low battery Tx abort
- Auxiliary serial peripheral interface (SPI) output
- Multiple power amplifier (PA) and switchplexor control options
- Enhanced anti-saturation schemes for GMSK
- No Tx modulation phasing
- Dither clock options for desense mitigation
- Fully programmable Rx selectivity filters for optimum modem performance
- Sensitivity: -109 dBm high band and -110 dBm low band
- Dual transfer mode (DTM) support with extended range Rx ADC
- Fast Rx fine DC offset correction (DCOC) convergence for extended battery life and higher class EGPRS support
- Internal trimmed band-gap reference lessens required tolerance on supply voltages and removes necessity for external reference voltages
- Integrated deep sleep mode (DSM) power management control
- 75 μA DSM current
- SYS_CLK can be provided by the MMM7010 or the baseband processor
- Low power airplane-mode clock generation
- 52 MHz clock reference output option
- Two auxiliary clock outputs
- Low current drain:
  - Rx ~ 78 mA
  - Tx ~ 66 mA, GMSK
  - Tx ~ 83 mA, 8PSK

# 2 Functional Block Diagram

Figure 1 illustrats the block diagram of the MMM7010 transceiver.

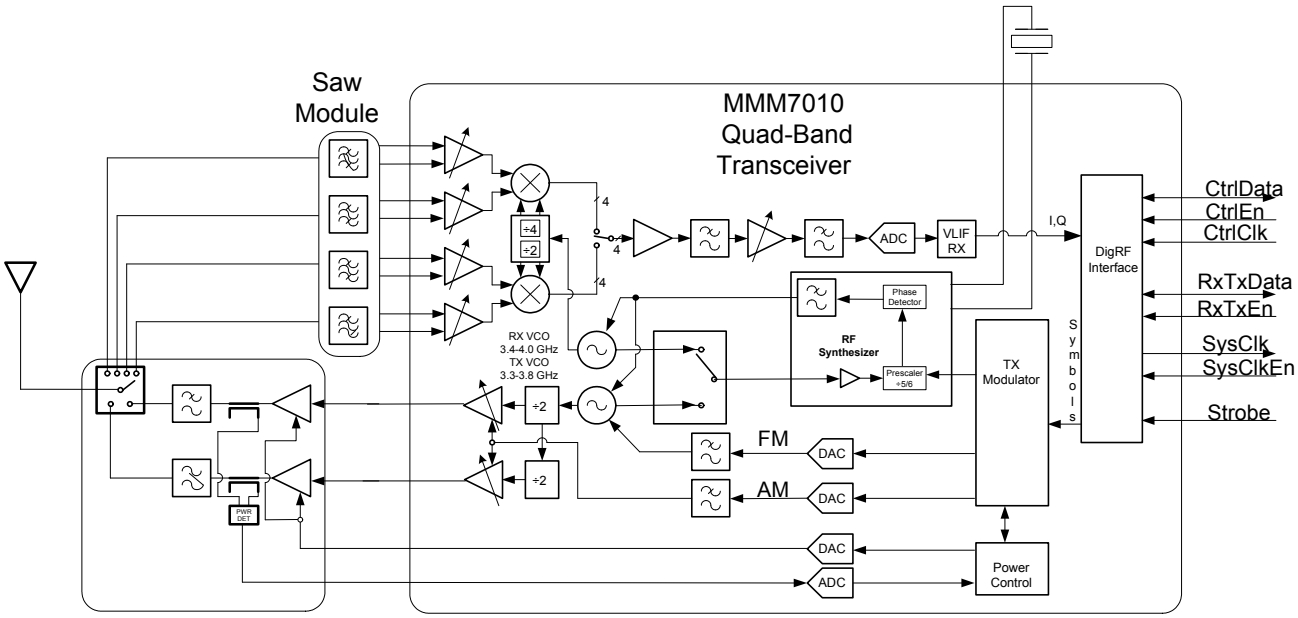



**Figure 1. MMM7010 Block Diagram**

# 3 Functional Description

This section provides an overview of the major subsystems that are integrated in MMM7010. Refer to Figure 1 for the MMM7010 block diagram.

## 3.1 Rx Analog Section

The MMM7010 receiver is a VLIF architecture that integrates the RF, analog baseband, analog-to-digital conversion, and digital baseband with a DigRF-capable interface. The receiver contains a separate input for each of the GSM 850, EGSM 900, DCS 1800, and PCS 1900 frequency bands. The RF input stages have differential inputs and stepped AGC capability with approximately 30 dB of dynamic range. The carefully matched unit elements in the AGC design and the elimination of tuned load elements anticipates elimination of Rx AGC gain step phasing found on previous platforms. Active differential filtering at the mixer output attenuates out-of-band signals reducing IP2 requirements of the later analog baseband filter.

The analog baseband filter (BBF) is a continuous-time filter made up of one bi-quad. Each channel of the analog BBF consists of two active stages. The analog BBF acts both as an anti-aliasing filter (AAF) and eases the dynamic range requirements on the ADC. The analog BBF has both stepped AGC and coarse DC offset correction (DCOC) capability, both adjusted via digital control. The analog-to-digital conversion consists of a sigma-delta modulator (SDM) followed by a sinc filter that incorporates downsampling. The SDM has a full scale differential input of 2 V peak-to-peak. Fine DCOC is applied before the digital image reject mixer which converts the signal to a true zero intermediate frequency. Further AAF filtering occurs to the digital signal before the downsampling. The signal then passes through a programmable channel

filter. Lastly, the signal is passed to the DigRF interface allowing output at both once or twice the symbol rate.

## 3.2 Tx Analog Section

The transmit architecture is a digital polar modulator with phase modulation of the VCO. The module can transmit in GMSK (phase only modulation) or 8PSK (phase and amplitude modulation) mode. In GMSK mode, the dual port Tx VCO is phase modulated by the dual port DAC and synthesizer. The signal is divided and then fed to the power amplifier (PA) input at a fixed level. In 8PSK mode, the additional amplitude modulation is performed via a commuting switch mixer. The mixer core drives a resistive digital step attenuator, which provides 0 to 45 dB of dynamic range in 3 dB steps, allowing the required full dynamic range to encompass all EDGE power steps with only 20 dB of dynamic range from the modulator. Two DACs provide signals to the modulator. One DAC is dedicated to the amplitude component of the 8PSK waveform and the other to the FM drive for the VCO high port input.

## 3.3 Frequency Generation

Both the Rx and Tx VCOs have integrated resonators with 32 states of digital coarse tuning. The frequency synthesizer is a 24-bit third order fractional-N synthesizer with digital AFC and lock time of less than 80 µs. A 52 MHz crystal oscillator provides a stable frequency reference. The VCO output signal runs through a divide-by-two for operation in the DCS/PCS bands and a divide-by-four for operation in the GSM/EGSM bands. For Tx, VCO operation at two or four times the Tx carrier frequency provides excellent immunity to remodulation.

The corrected clock module is a 26-bit digital phase-locked loop used to provide an accurate 26 MHz SYS_CLK reference, synchronized to the GSM system when the system is operated from the uncorrected 52 MHz crystal oscillator reference.

The 52 MHz crystal oscillator reference provides a frequency reference for the major functions in the radio system. The crystal output, or a divided version, can also be routed to two auxiliary reference pins to provide a reference clock for RF transceivers such as Bluetooth®, GPS, and WLAN.

## 3.4 Digital Core

The digital core of the MMM7010 transceiver consists of four major functional blocks:

- Receive coprocessor (RxCPROC)
- DigRF
- Transmit module (TXM)
- Layer 1 timing controller

### 3.4.1 Receive Coprocessor (RxCPROC)

The receive coprocessor is the digital portion of the Rx signal processing chain, consisting of the decimation filters, a digital local oscillator (LO), complex mixers, adjustable channel filters and a DC offset removal module. The initial conversion is achieved by the sigma-delta modulator ADC and the

results are passed into the RxCPROC. Processed signals are sent serially to the baseband processor through the DigRF interface port.

### 3.4.2 DigRF

The DigRF standard specifies the logical, electrical and timing details of the RF-baseband interface. The MMM7010 transceiver complies with version 1.12 of this standard. Figure 2 shows the signals within the DigRF interface. Full details of this standard are available at: www.digrf.com.

Another variation of digital interface is supported by the MMM7010 transceiver, which eliminates the need for bi-directional CMOS signalling.

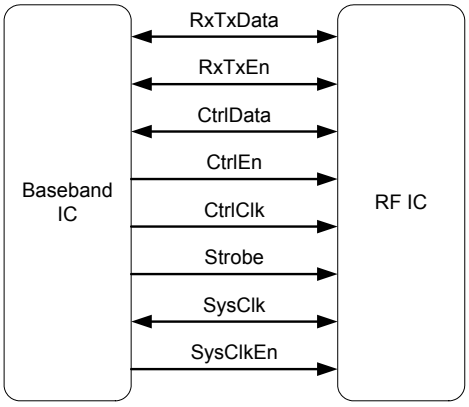



**Figure 2. DigRF Standard RF-Baseband Interface**

### 3.4.3 Transmit Module (TXM)

The digital transmit module (TXM) supports two modulation schemes (GMSK and 8PSK). The output is in polar format.

### 3.4.4 Layer 1 Timing Controller

The MMM7010 internal layer 1 timing controller generates appropriate timing events for the transmitter calibration and the EDGE/GMSK transmit/receive burst, thereby limiting the RF hardware dependency of the layer 1 engine software on the baseband.

# 4 Electrical Characteristics

The MMM7010 can be operated using a single regulated supply[1]. The AVDD_ANA and AVDD_RF pins supply all internal analog and RF supplies respectively. The AVDD_CORE pin supplies the main digital supply. The VDD_DIGIO and VDD_DIGRF supplies determine the interface voltage levels for baseband or other auxiliary ICs that require clock signals from the MMM7010.Table 1 conditions are maximum

1. VDD_DIGIO can be connected to one of the 2.7 V supplies if this is the preferred voltage to the auxiliary circuits interfacing to the VDD_DIGIO pins such as the PA. For PCB level isolation purposes, this should be connected in a “star” configuration if all of the 2.7 V supplies are coming from the same regulator.

ratings so as not to induce permanent device damage. They do not reflect functional operating range. Table 2 lists the operating supply voltage requirements.

**Table 1. Extreme Ratings**

| Characteristic | Pin/Supply Name | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply Voltage | VDD_DIGIO | -0.5 | 3.0 | V | Logic Level for interface voltage to PA/switch plexer control and BT_CLK_EN and AUX_CLK supply voltages. |
| Supply Voltage | VDD_DIGRF | -0.5 | 3.0 | V | Interface voltage for CMOS logic interfacing to BB ICs. |
| Supply Voltage | AVDD_CORE | -0.5 | 3.0 | V | Main Supply |
| Supply Voltage | AVDD_ANA | -0.5 | 3.0 | V | Analog Supply |
| Supply Voltage | AVDD_RF | -0.5 | 3.0 | V | RF Supply Voltage |
| Storage Temperature | — | -55 | +150 | deg C | — |

**Table 2. Operating Supply Voltage Requirements**

| Pin/Supply Name | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| VDD_DIGIO | 1.62 | 2.7 or 1.8 | 2.875 | V | Logic level for interface voltage to PA/switch plexer control and BT_CLK_EN and AUX_CLK supply voltages. Selectable in the range 1.62–2.875. |
| VDD_DIGRF | 1.62 | 2.7 or 1.8 | 2.875 | V | Interface voltage for CMOS logic interfacing to BB ICs. |
| AVDD_CORE | 2.62 | 2.7 | 2.875 | V | Main Supply: Can be connected to AVDD_ANA and AVDD_RF. |
| AVDD_ANA | 2.62 | 2.7 | 2.875 | V | Analog Supply: Recommend that this is connected to AVDD_RF. |
| AVDD_RF | 2.62 | 2.7 | 2.875 | V | 2.7 - 3% to 2.775 + 3.6%. |

## 4.1 Current Drain

Table 3 summarizes the current drain of the MMM7010. The table shows the current drain in various modes. The MMM7010 transceiver supports a mode with minimal current drain supplying BT_CLK clock only.

**Table 3. Current Drain**

| Parameter | Typical Peak Current (mA) |
|---|---|
| Deep Sleep Current | 0.075 |
| Bluetooth Clock Only Active | 2.03 |
| Standby Current, Only System Clk On | 4.30 |
| Rx LB Burst | 79.35 |
| Rx HB Burst | 82.85 |
| LB GMSK Tx | 72.40 |

**Table 3. Current Drain (continued)**

| Parameter | Typical Peak Current (mA) |
|---|---|
| LB GMSK Tx LP[1] | 62.90 |
| HB GMSK Tx | 76.90 |
| HB GMSK Tx LP | 66.10 |
| LB 8PSK Tx | 82.00 |
| HB 8PSK Tx | 82.70 |

1 Low-power mode (LP) defined as closed loop ramp up with a hold mode for the duration of burst as opposed to full closed loop power control in normal mode.

## 4.2 Power-Up Requirements

When the MMM7010 is powered up from an off state, the baseband is required to write up to 16 Kbytes of configuration information through the digital interface and to initiate power-up calibration routines. The programmer's release kit for the MMM7010 provides the start-up configuration as a hex data file. For supported operating modes, the radio integration team does not need to modify the start-up configuration.

## 4.3 Rx Performance

The MMM7010 Rx performance is summarized in Table 4. Faster warm up and warm down time for the MMM7010 receiver can result in a 25% reduction in Rx on time per frame in call mode; see Table 4 for typical values.

**Table 4. Rx Performance**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Total available analog voltage gain[1] | 50 | 52 | 54 | dB |
| Gain variation with temperature (over all gain settings) | -0.6 | — | 0.6 | dB |
| Cascaded GSM noise figure excluding external losses | — | 2.0 | 2.9 | dB |
| Cascaded EGSM noise figure excluding external losses | — | 2.0 | 2.9 | dB |
| Cascaded DCS noise figure excluding external losses | — | 3.0 | 3.9 | dB |
| Cascaded PCS noise figure excluding external losses | — | 3.0 | 3.9 | dB |
| Cascaded GSM sensitivity at the antenna, 6.5 dB SNR, 25 ± 10 °C | — | -109.9 | -109.0 | dBm |
| Cascaded EGSM sensitivity at the antenna, 6.5 dB SNR, 25 ± 10 °C | — | -109.9 | -109.0 | dBm |
| Cascaded DCS sensitivity at the antenna, 6.5 dB SNR, 25 ± 10 °C | — | -108.9 | -108.0 | dBm |
| Cascaded PCS sensitivity at the antenna, 6.5 dB SNR, 25 ± 10 °C | — | -108.9 | -108.0 | dBm |
| Cascaded GSM sensitivity at the antenna, 6.5 dB SNR, -20 °C to +85 °C | — | -108.9 | -108.0 | dBm |
| Cascaded EGSM sensitivity at the antenna, 6.5 dB SNR, -20 °C to +85 °C | — | -108.9 | -108.0 | dBm |
| Cascaded DCS sensitivity at the antenna, 6.5 dB SNR, -20 °C to +85 °C | — | -107.9 | -107.0 | dBm |

**Table 4. Rx Performance (continued)**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Cascaded PCS sensitivity at the antenna, 6.5 dB SNR, -20 °C to +85 °C | — | -107.9 | -107.0 | dBm |
| Intermodulation performance, 2 tone interferer[2], 8 dB CINR, front end loss included. | -49 | -42 | — | dBm |
| Interference performance, 8 dB SNR[3], front end loss included<br>± 200 kHz<br>± 400 kHz<br>± 600 kHz | <br>9<br>41<br>49 | — | — | dBm |
| 1 dB compression point @ maximum RF gain, referred to antenna with front end loss included | -32.7 | — | — | dBm |
| 1 dB compression point @ minimum RF gain, referred to antenna with front end loss included | -6.55 | — | — | dBm |
| Local Oscillator (LO) leakage from MMM7010 measured at antenna port, ARFCN center frequency + and - VLIF frequency. | — | — | -89.8 | dBm |
| RF AGC range | 28.2 | 29.2 | 30.2 | dB |
| Baseband AGC range (analog) | 23.8 | 24.0 | 24.2 | dB |
| In-band blocking:<br>0.6 MHz< [f-fo] < 0.8 MHz<br>0.8 MHz< [f-fo] < 1.6 MHz<br>1.6 MHz< [f-fo] < 3 MHz<br>3 MHz < [f-fo] to band edge<br>3 MHz < [f-fo], EDGE modulated[4], GSM850, EGSM900, measured at the antenna.<br>3MHz < [f-fo], EDGE modulated[4], DCS1800,PCS1900, measured at the antenna. | <br>-43<br>-43<br>-33<br>-23<br>-27<br>-28 | — | — | dBm |
| AM suppression[5], insertion loss included | -31 | — | — | dBm |
| **Note:** Composite channel selectivity bandwidth used = 180 kHz, 8 dB CINR, 2.6 dB insertion loss minimum for GSM850/EGSM900, and 3.1 dB minimum insertion loss for DCS1800/PCS1900. | | | | |

1 80.3 μV/LSB conversion factor at ADC input, 0 dB digital gain, and signal present at baseband/MMM7010 interface.

2 Interferer input level as per 3GPP TS45.005, Para 5.3.

3 Signal input level as per 3GPP TS45.005, Para 6.3.

4 Signal input level as per 3GPP TS45.005, Para 5.1.

5 Signal input level as per 3GPP TS45.005, Para 5.2.

## 4.4 Tx Performance

The MMM7010 Tx performance (excluding PA) is summarized in Table 5.

**Table 5. Tx Performance**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **GMSK** | | | | |
| RMS global phase error | — | — | 2° rms, 7° peak | deg |
| ACP@400 kHz | — | -70 | — | dBref/30 kHz |
| **LB** | | | | |
| Noise at 20 MHz | — | -165 | — | dBc/Hz |
| Noise at 10 MHz | | -156 | — | dBc/Hz |
| Output power | 4 | — | 9 | dBm |
| **HB** | | | | |
| Noise at 20 MHz | — | — | -159 | dBc/Hz |
| Output power | 4 | — | 9 | dBm |
| **8PSK** | | | | |
| EVM | — | — | 3% rms, 7% peak | % |
| ACP@400 kHz | — | — | -64 | dBref/30 kHz |
| **LB** | | | | |
| Noise at 20 MHz | — | — | -159 | dBc/Hz |
| Noise at 10 MHz | — | — | -148 | dBc/Hz |
| Output power @ 2.7 V and 25 °C | -3.15 | — | 2.95 | dBm |
| **HB** | | | | |
| Noise at 20 MHz | — | — | -150 | dBc/Hz |
| Output power @ 2.7 V and 25 °C | -3.75 | — | 2.35 | dBm |

## 4.5 Frequency Generation

### 4.5.1 RF Synthesizer

The MMM7010 RF synthesizer is a 24-bit, third-order fractional-N synthesizer. The VCOs are coarse tuned, minimizing the frequency lock range required of the synthesizer. The VCOs also have Kv (VCO sensitivity, MHz/V) tracking to minimize loop bandwidth variation of the PLL during operation, allowing optimal performance without factory calibration or interaction with the baseband layer 1 software. The AFC range is ± 122 ppm for the MMM7010. The 3GPP ARFCN value is programmed to set the frequency.

### 4.5.2 Clock References

The crystal or TCXO frequency required for use with the MMM7010 is a 52 MHz device. The TCXO input parameters are specified in Table 6. The TCXO input needs to be AC coupled to the XTAL pin through a 1 nF capacitor in the application. The EXTAL is left floating for TCXO applications. Both EXTAL and XTAL pins are used to connect to the crystal unit when used.

**Table 6. TCXO Input Parameter**

| Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Level | — | .8 | — | Vp-p | — |
| Large Signal Input Impedance | 171,11.1 | — | 185,12.4 | ohms/pf | Equivalent impedance is defined as resistor in parallel with capacitor. |

### 4.5.3 Clock Sources

There are three output clock sources available from the MMM7010. The specifications are summarized in Table 7. The clock synthesizer output option is available for SYS_CLK only.

**Table 7. Clock Sources**

| Pin Name | Type | Freq. (MHz) | AFC option | Amplitude |
|---|---|---|---|---|
| BT_CLK | Sine | 26 | No | 200 mV pk-pk |
| AUX_CLK | CMOS Square Wave | 26 or 52 | No | VDD_DIGRF |
| SYS_CLK | CMOS Square Wave | 26 | Option available via clock synthesizer | VDD_DIGRF |

### 4.5.4 Clock Synthesizer

The clock synthesizer is supplied with the same AFC word as the RF synthesizer. The AFC scaling is done internally on the MMM7010. The specifications for the clock synthesizer are summarized in Table 8.

**Table 8. Clock Synthesizer**

| Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Reference Frequency | — | 52 | — | MHz | |
| Output Frequency | — | 26 | — | MHz | SYS_CLK |
| Jitter | — | 0.3 | 1.2 | ns | Pk-Pk, dither disabled, maximum pad drive strength |
| | — | 2.2 | 4 | ns | Pk-Pk, dither enabled, maximum pad drive strength |
| Lock Time | — | — | 100 | μs | To 0.1 ppm frequency resolution |
| Resolution | — | — | .387 | Hz | At SYS_CLK |

# 5 Programming

This section provides some detail on how the baseband can control the MMM7010 transceiver through the digital interface.

## 5.1 MMM7010 Programming Model

The digital architecture the MMM7010 is designed to minimize the dependency of baseband layer 1 timing software on the RF transceiver architecture. No timing critical SPI writes are required to set up the MMM7010 for transmission or reception of a burst; instead all critically timed events including the powering of blocks are normally initiated by the assertion of the DigRF strobe pin. This has the immediate benefit of reducing the amount and complexity of the baseband layer 1 software.

### 5.1.1 MMM7010 Programming Interface

The digital baseband processor communicates to the layer 1 timing controller through the digital interface. The layer 1 timing controller interprets the commands and generates the sequence of signals required, both internally and externally, for timing control of the radio. Figure 3 shows the block diagram of the digital programming interface on the MMM7010.

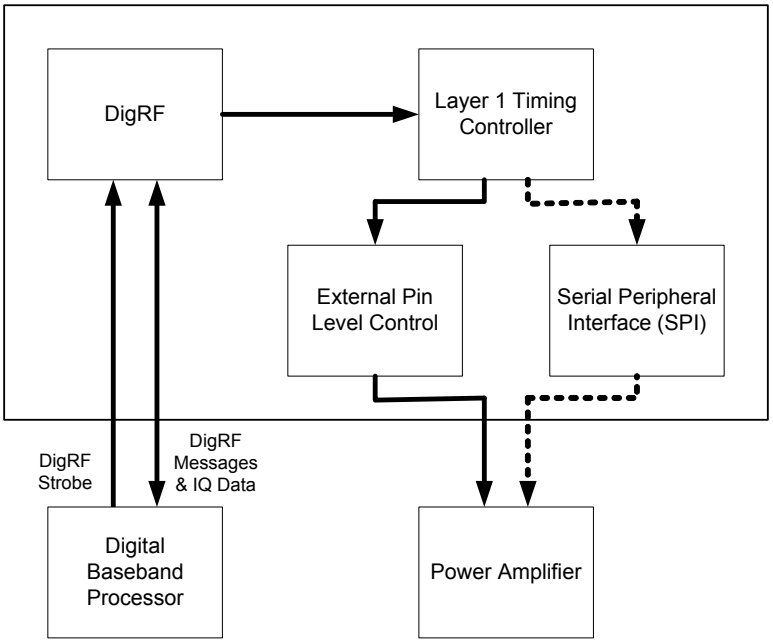



**Figure 3. Block Diagram of the Digital Programming Interface on the MMM7010**

### 5.1.2 Layer 1 Timing Controller Sequencing

The layer 1 timing controller generates precisely timed signal transitions through the external pin level control. The timing of these signals is quarter symbol clock accurate relative to the DigRF strobe. The layer 1 timing controller determines which sequence of signals is required based on configuration information supplied from the digital baseband processor through the digital interface. The digital

baseband processor can configure the layer 1 timing controller on the MMM7010 to generate all the internal and external signal transition sequences necessary for timing control of the radio, from the power-up sequence through the warm-up of the synthesizer and VCO, calibrations when required, handling of a burst, and finally powering down of the radio at the end of a burst if appropriate.

## 5.2 Burst Level Programming

The MMM7010 supports both stream and block Tx data transfers as defined by the DigRF V1.12 standard. In stream mode, data bits are transferred across to the modulator at the symbol rate as four-bit nibbles with a predetermined latency. In block mode, data bits are transferred across as four-bit nibbles by the 26 MHz system clock, and are buffered by a FIFO inside the MMM7010 prior to the start of a burst. From a software perspective, block mode is by far the simplest since it completely decouples the arrival of data from the DigRF strobe that defines the ramp-up of a burst.

The MMM7010 has a few functions timed directly from DigRF writes. All critically timed functions are normally initiated via the DigRF strobe. The RxTxEn is used as a layer 1 signal in stream mode since the data transfer must be quarter symbol accurate. Control register data must be present and correct at the time of the first DigRF strobe initiating a Tx or Rx sequence. All layer 1 functions controlling the PA are derived inside the MMM7010 based on the DigRF strobe, including configuration of the antenna interface.

For multi-slot mode, all slot-dependant control register information is written prior to the first slot. This means that the Tx control registers (MOD_MODE, AOC_PARAM, PAC_POWER and ShutDownDelay) are all replicated for each slot (up to six slots) and applied to the appropriate slot automatically by the layer 1 timing controller. To configure the MMM7010 for a single-slot Tx burst on a traffic channel requires a total of 64 bits written across the digital interface. Each additional slot in the burst requires an additional 48 bits to be written for a maximum total of 304 bits in the case of a six slot burst. To configure the MMM7010 for a typical Rx burst requires two 16-bit control writes.

The complete set of control registers required for burst level programming is summarized in Table 9 and Table 10.

**Table 9. Control Registers for all Tx and Rx Modes**

| | Bit Field | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register Name** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COLDCAL | | | | | | | | | | | | | | | COLDCALSEL | |
| ABORT | ABORT_CMD | | | | | | | | | | | | | | | |
| REGUL_INIT | REGS_CMD | | | | | | | | | | | | | | | |
| RXEND | RXEND_CMD | | | | | | | | | | | | | | | |
| MARSCFG | rxiir_s_wbw | rxiir_k | | | rxcoproc_fdcocsel | | rx_gain_rdbk | iq_swap | loflip_cfg | blkwden | | patype | | | | DPLLEN |
| RXACQ | rx_filt_sel | | loflip | rssi | | | | | | | Reserved | | | rxdither_sysclk | rxdither_path | fir_iir_aaf |
| SYNTHAFC | afcposorneg | afcmag | | | | | | | | | | | | | | |
| CHCFG | rxtx_mode | arfcn | | | | | | | | | | dcspcs | mixed_mode | num_slots | | |

**Table 9. Control Registers for all Tx and Rx Modes (continued)**

| | Bit Field | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register Name** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TXSLOT1_A | pac_power_1 | | | | | | | | | | aoc_param_1 | | | | gmsk_single_port_1 | gmsk_i_pc_mode_1 |
| TXSLOT1_B | Reserved | | | shutdowndelay_1 | | | | | | | | | | mod_mode_1 | dig_pac_lp1 | ta_63_1 |
| TXSLOT1_C | txdither_sysclk | txdither_path | dist_talign_1 | | | numsymbolsperslot_1 | | | | | | | | | | pac_gmsk_sat_en_1 |
| TXSLOT2_A | pac_power_2 | | | | | | | | | | aoc_param_2 | | | | gmsk_single_port_2 | gmsk_i_pc_mode_2 |
| TXSLOT2_B | Reserved | | | shutdowndelay_2 | | | | | | | | | | mod_mode_2 | dig_pac_lp2 | ta_63_2 |
| TXSLOT2_C | Reserved | | | | | numsymbolsperslot_2 | | | | | | | | | | pac_gmsk_sat_en_2 |
| TXSLOT3_A | pac_power_3 | | | | | | | | | | aoc_param_3 | | | | gmsk_single_port_3 | gmsk_i_pc_mode_3 |
| TXSLOT3_B | Reserved | | | shutdowndelay_3 | | | | | | | | | | mod_mode_3 | dig_pac_lp3 | ta_63_3 |
| TXSLOT3_C | Reserved | | | | | numsymbolsperslot_3 | | | | | | | | | | pac_gmsk_sat_en_3 |
| TXSLOT4_A | pac_power_4 | | | | | | | | | | aoc_param_4 | | | | gmsk_single_port_4 | gmsk_i_pc_mode_4 |
| TXSLOT4_B | Reserved | | | shutdowndelay_4 | | | | | | | | | | mod_mode_4 | dig_pac_lp4 | ta_63_4 |
| TXSLOT4_C | Reserved | | | | | numsymbolsperslot_4 | | | | | | | | | | pac_gmsk_sat_en_4 |
| TXSLOT5_A | pac_power_5 | | | | | | | | | | aoc_param_5 | | | | gmsk_single_port_5 | gmsk_i_pc_mode_5 |
| TXSLOT5_B | Reserved | | | shutdowndelay_5 | | | | | | | | | | mod_mode_5 | dig_pac_lp5 | ta_63_5 |
| TXSLOT5_C | Reserved | | | | | numsymbolsperslot_5 | | | | | | | | | | pac_gmsk_sat_en_5 |
| TXSLOT6_A | pac_power_6 | | | | | | | | | | aoc_param_6 | | | | gmsk_single_port_6 | gmsk_i_pc_mode_6 |
| TXSLOT6_B | Reserved | | | shutdowndelay_6 | | | | | | | | | | mod_mode_6 | dig_pac_lp6 | ta_63_6 |
| TXSLOT6_C | Reserved | | | | | numsymbolsperslot_6 | | | | | | | | | | pac_gmsk_sat_en_6 |

**Table 10. Control Register Fields for all Tx and Rx Modes**

| Field | Description |
|---|---|
| rx_filt_sel | Receive filter selection. |
| loflip | Local oscillator injection polarity. |

**Table 10. Control Register Fields for all Tx and Rx Modes (continued)**

| Field | Description |
|---|---|
| rssi | Receive signal strength indicator. |
| rxdither_sysclk | Enable SYS_CLK out dither in Rx mode. |
| rxdither_path | Enable data path dither in Rx mode. |
| afcposneg | Synthesizer AFC sign - calculated AFC fractional correction sign. |
| afcmag | Synthesizer automatic frequency control (AFC) magnitude register - calculated AFC fractional correction value to correct the DPLL and VCO. |
| rxtx_mode | Select Rx or Tx mode. |
| arfcn | Select absolute radio frequency channel number. |
| dcspcs | DCS or PCS band if high band ARFCN is selected (overlapping ARFCNs). |
| pac_power | Power amplifier controller (PAC) power level. |
| aoc_param | Amplifier output control (AOC) parameters used in conjunction with modulation mode to index into PAC RAM. |
| gmsk_single_port | Select single port modulation. Save current with single port modulation in GMSK mode. |
| gmsk_i_pc _mode | GMSK Input Power Control (IPC) mode enable. Enable or disable bit for GMSK IPC mode. |
| mixed_mode | Set to 1 if there are any 8PSK slots in the burst. |
| num_slots | Number of slots in the burst (up to 6). |
| shutdowndelay | In block mode Tx transfer, this is the time between the last symbol and turn of the Tx modulator. |
| mod_mode | Modulation mode – GMSK or 8PSK. |
| dac_pac_lp | Low power GMSK mode enable for PAC. This turns off the FB circuits from the PA once ramped to final value. |
| Ta_63 | Fast PAC ramp down mode used for RAACH followed by TCH close to a 63 symbol timing advance. |
| txdither_sysclk | Enable SYS_CLK out dither in transmit. |
| txdither_path | Enable data path dither in transmit. |
| pac_gmsk_sat_en | Enable saturation detection and correction for GMSK mode (ignored in 8PSK mode slots). |

The MMM7010 radio is configured for block-mode or stream-mode data transfer at power-up. This does not change on a slot-by-slot basis.

In a block-mode multi-slot transfer, all the power amplifier controller information (PAC) for each slot can be sent over prior to the start of transmission.

In a stream-mode multi-slot transfer, all the PAC information for each slot can be sent over prior to the start of transmission or the PAC information for each slot can be updated prior to the beginning of each slot.

## 5.3 Software Programming

This section describes the different modes of operation for the MMM7010. The amount of software programming and the number of bits transferred for each operation are detailed.

### 5.3.1 Power-Up Initialization

At power-up, the digital baseband is required to send initial configuration information to the MMM7010 through the digital interface. This data is provided by Freescale in a file that specifies the addresses and associated data required for the initial configuration of the MMM7010. This data consists of 10,180 x 16-bit words maximum, in hexadecimal format, but this size may vary with revisions of the MMM7010 and software.

After the initial configuration information is set up, the digital baseband must issue a cold calibration command to the MMM7010. This command triggers a calibration sequence for the Tx and Rx chains. If the application requires the MMM7010 to provide a BT_CLK clock, the baseband processor can simply activate the BT_CLK_EN pin after initialization to provide a BT_CLK output.

### 5.3.2 Low Battery Condition

The MMM7010 contains a feature that supports a low battery condition on the radio. If the INT pin is deasserted, MMM7010 terminates a Tx burst and prevents future transmissions until the INT pin is reasserted. If this feature is not required on the platform, then the INT pin should remain unconnected as MMM7010 has a weak pull-up on this pin.

### 5.3.3 Transmit Burst

A transmit burst is configured via DigRF/SPI writes to control registers. A Freescale extension to the DigRF standard allows writes to multiple contiguous registers to be combined into a single DigRF write.

- **For a Normal Single-slot GSM Tx Burst**
  The MMM7010 is configured for a normal single-slot GSM Tx burst by writing to four contiguous 16-bit registers. A DigRF strobe then transitions the system from standby to synthesizer-locked, power ramp-up, data modulation and power ramp down. At the end of this sequence, the transceiver is restored to the standby configuration.
- **For a Normal Multi-slot GSM Tx Burst**
  The MMM7010 is configured for a normal multi-slot GSM Tx burst by writing to seven contiguous 16-bit registers plus an additional three contiguous 16-bit words for each slot after the first slot. A DigRF strobe then initiates the same sequence as for a single slot burst except that the power ramp-up, data modulation and power ramp-down phase is repeated for each slot. At the end of this sequence, the transceiver is restored to the standby configuration.

### 5.3.4 Receive Burst

For a normal GSM Rx burst, the MMM7010 is configured by writing to two, 16-bit registers: RXACQ and CHCFG. These registers are non-contiguous, so two control writes are required. A DigRF strobe activates

the receiver, runs the DC adapt algorithm, and initiates the DigRF transfer. A receive burst is ended by a strobe or an RXEND command via DigRF/SPI and the transceiver is restored to the standby configuration.

### 5.3.5 AFC Updates

AFC updates are performed by writing to a single, 16-bit register. This register is contiguous with the registers that need to be written for Tx and Rx bursts, and so the AFC update can be concatenated on to a single control write. The AFC word is scaled internally for all frequency channels in all bands.

For Rx, the AFC register is located between the two registers that need to be written for Rx burst configuration, making this a contiguous block of three registers. As such, an Rx burst with AFC can be configured in a single DigRF SPI write, one less than is required for an Rx burst without AFC.

The ppm error is digitized and not derived from a frequency pulling code for reference oscillator. A dynamic range of ± 122.067 ppm is capable of frequency correction.

# 6 Signal Descriptions

Table 11 defines the MMM7010 transceiver signals.

**Table 11. MMM7010 Signal Description Table**

| Pin ID | Pin Name | Description |
|---|---|---|
| 1 | GROUND | Ground |
| 2 | XTAL | Crystal input |
| 3 | EXTAL | Crystal input |
| 4 | GROUND | Ground |
| 5 | AVDD_ANA | Analog supply |
| 6 | GROUND | Ground |
| 7 | VRAMP | PAC bias control |
| 8 | VDETECT | Power amplifier detect feedback |
| 9 | GROUND | Ground |
| 10 | ATST_PRI_N | Analog test primary negative |
| 11 | ATST_PRI_P | Analog test primary positive |
| 12 | GROUND | Ground |
| 13 | LB_OUT | Low band transmit output |
| 14 | GROUND | Ground |
| 15 | HB_OUT | High band transmit output |
| 16 | GROUND | Ground |
| 17 | GROUND | Ground |
| 18 | AVDD_RF | RF supply |

**Table 11. MMM7010 Signal Description Table (continued)**

| Pin ID | Pin Name | Description |
|---|---|---|
| 19 | GROUND | Ground |
| 20 | GROUND | Ground |
| 21 | PCS_P | PCS 1900 positive receive input |
| 22 | PCS_N | PCS 1900 negative receive input |
| 23 | DCS_P | DCS 1800 positive receive input |
| 24 | DCS_N | DCS 1800 negative receive input |
| 25 | EGSM_P | EGSM 900 positive receive input |
| 26 | EGSM_N | EGSM 900 negative receive input |
| 27 | CELL_P | GSM 850 positive receive input |
| 28 | CELL_N | GSM 850 negative receive input |
| 29 | GROUND | Ground |
| 30 | CTRL_DATA | DigRF control data input/output |
| 31 | GROUND | Ground |
| 32 | AVDD_CORE | Digital Core Supply |
| 33 | GROUND | Ground |
| 34 | RXTX_DATA | DigRF Rx/Tx data input/output |
| 35 | SYS_CLK | DigRF system clock input/output |
| 36 | VDD_DIG_1P2 | 1.2 V input/output |
| 37 | VDD_DIGRF | DigRF I/O supply |
| 38 | VDD_DIGIO | Digital I/O supply |
| 39 | GROUND | Ground |
| 40 | DVMUX_FRAME | Digital visible multiplexer frame signal output |
| 41 | CTRL_CLK | DigRF control clock input |
| 42 | AUX_CLK | Auxiliary clock output |
| 43 | STROBE | DigRF strobe input |
| 44 | GROUND | Ground |
| 45 | PA_WAKE | Power amplifier activation output |
| 46 | ALT_SPI_CE | High band/low band control signal/alternate SPI enable input/output |
| 47 | GROUND | Ground |
| 48 | GROUND | Ground |
| 49 | ATST_SEC_N | Analog test secondary negative input/output |
| 50 | SPI_CE | Power amplifier digital control signal output |
| 51 | SPI_DATA | Serial peripheral interface data output |

**Table 11. MMM7010 Signal Description Table (continued)**

| Pin ID | Pin Name | Description |
|---|---|---|
| 52 | CTRL_EN | DigRF control enable input |
| 53 | GROUND | Ground |
| 54 | ATST_SEC_P | Analog test secondary positive input/output |
| 55 | SPI_CLK | Serial peripheral interface clock output |
| 56 | DVMUX_CLK | Digital visible multiplexer clock/background debug mode output |
| 57 | GROUND | Ground |
| 58 | GROUND | Ground |
| 59 | INT | Baseband processor interrupt pin/low battery pin input/output |
| 60 | GROUND | Ground |
| 61 | DVMUX_DATA | Digital visible multiplexer data output |
| 62 | RXTX_EN | DigRF Rx/Tx data enable input/output |
| 63 | GROUND | Ground |
| 64 | GROUND | Ground |
| 65 | BT_CLK_EN | Bluetooth clock enable input |
| 66 | SYS_CLK_EN | DigRF system clock enable input |
| 67 | GROUND | Ground |
| 68 | GROUND | Ground |
| 69 | GROUND | Ground |
| 70 | BT_CLK | Bluetooth clock output |
| 71 | GROUND | Ground |
| 72 | RESET_B | Active low master device reset input |
| 73 | GROUND | Ground |

# 7 Package Information

The MMM7010 is a 73-pin I/O, Land Grid Array (LGA), 5.2 mm × 6.8 mm × 1.1 mm module. Figure 4 and Figure 5 show the package outline. Figure 6 shows the MMM7010 pin positions.

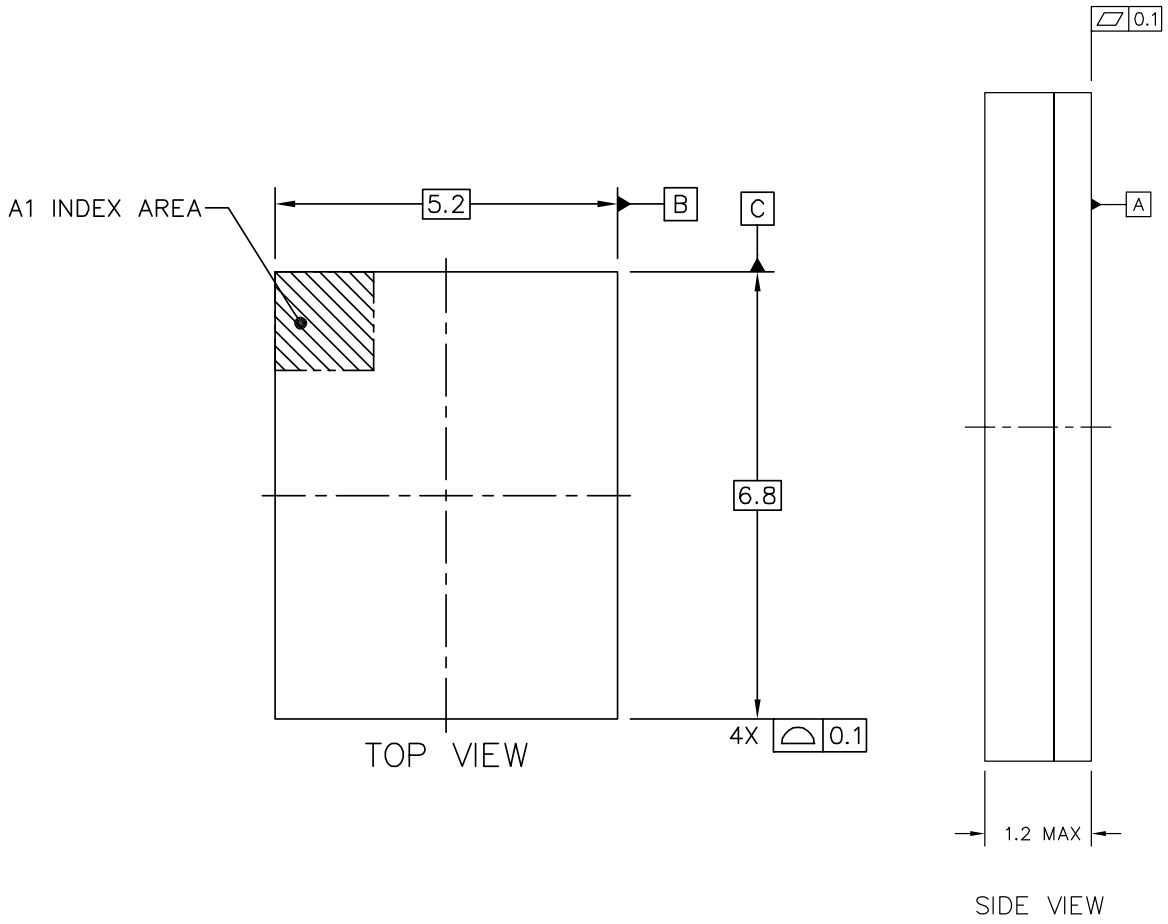
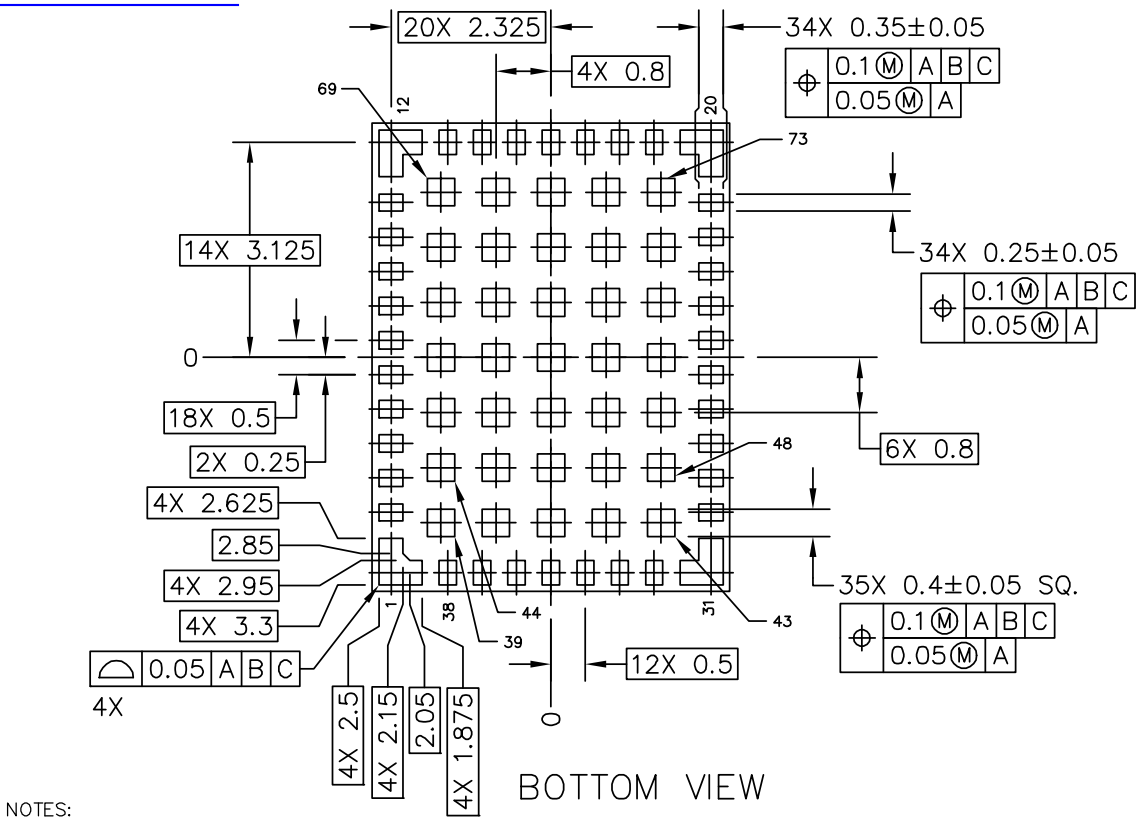



**Figure 4. Package Outline - Top and Side View**




NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

**Figure 5. Package Outline - Bottom View**

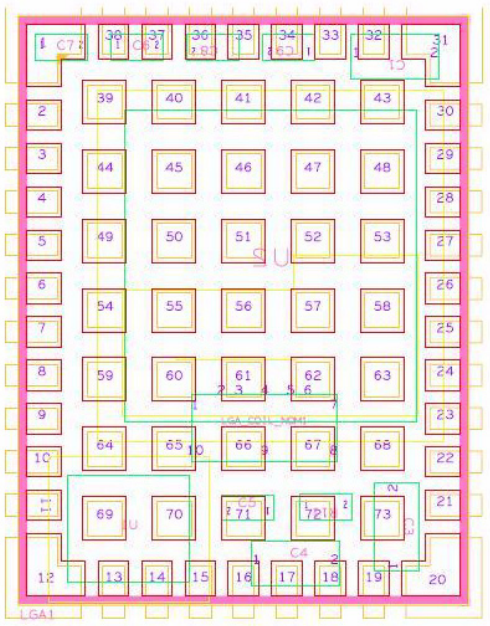


**Figure 6. MMM7010 Pin Positions**

# 8 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com on the documentation page.

Table 12 summarizes revisions made to this document since the previous release (Rev. 3.5).

**Table 12. Revision History**

| Location | Revision |
|---|---|
| Throughout | Clarified introduction and made other non-technical content changes. |

***How to Reach Us:***

**Home Page:**
www.freescale.com

**Web Support:**
http://www.freescale.com/support

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

***For Literature Requests Only:***
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MMM7010
Rev. 3.6
7/2010