



Not recommended for new designs –  
Please use 93LC76C or 93LC86C.

# 93LC76/86

## 8K/16K 2.5V Microwire Serial EEPROM

### Features:

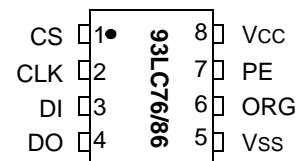
- Single supply with programming operation down to 2.5V
- Low-power CMOS technology
  - 1 mA active current typical
  - 5  $\mu$ A standby current (typical) at 3.0V
- ORG pin selectable memory configuration
  - 1024 x 8 or 512 x 16 bit organization (93LC76)
  - 2048 x 8 or 1024 x 16 bit organization (93LC86)
- Self-timed erase and write cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during erase/write cycles
- Sequential read function
- 1,000,000 erase/write cycles ensured
- Data retention > 200 years
- 8-pin PDIP/SOIC package
- Temperature ranges available
  - Commercial (C) 0°C to +70°C
  - Industrial (I) -40°C to +85°C

### Description:

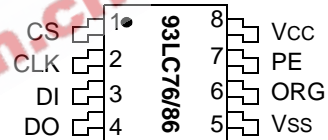
The Microchip Technology Inc. 93LC76/86 are 8K and 16K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. These devices also have a Program Enable (PE) pin to allow the user to write-protect the entire contents of the memory array. The 93LC76/86 is available in standard 8-pin PDIP and 8-pin surface mount SOIC packages.

### Package Types

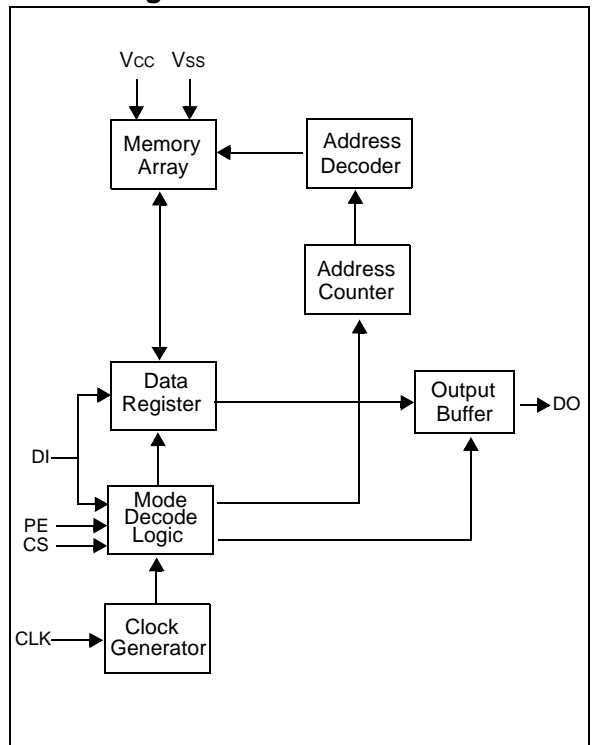
#### PDIP Package



#### SOIC Package



### Block Diagram



# 93LC76/86

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

VCC.....	7.0V
All inputs and outputs w.r.t. Vss .....	-0.6V to Vcc + 1.0V
Storage temperature .....	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
Soldering temperature of leads (10 seconds) .....	+300°C
ESD protection on all pins.....	4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### 1.1 AC Test Conditions

AC Waveform:

VLO = 2.0V

VHI = Vcc - 0.2V      **(Note 1)**

VHI = 4.0V for      **(Note 2)**

Timing Measurement Reference Level

Input                    0.5 Vcc

Output                   0.5 Vcc

**Note 1:** For Vcc ≤ 4.0V

**2:** For Vcc > 4.0V

**TABLE 1-1: DC CHARACTERISTICS**

DC CHARACTERISTICS Applicable over recommended operating ranges shown below unless otherwise noted: V <sub>CC</sub> = +2.5V to +6.0V Commercial (C): TA = 0°C to +70°C Industrial (I): TA = -40°C to +85°C					
Parameter	Symbol	Min.	Max.	Units	Conditions
High-level input voltage	V <sub>IH1</sub>	2.0	V <sub>CC</sub> + 1	V	V <sub>CC</sub> ≥ 2.7V
	V <sub>IH2</sub>	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 1	V	V <sub>CC</sub> < 2.7V
Low-level input voltage	V <sub>IL1</sub>	-0.3	0.8	V	V <sub>CC</sub> ≥ 2.7V
	V <sub>IL2</sub>	-0.3	0.2 V <sub>CC</sub>	V	V <sub>CC</sub> < 2.7V
Low-level output voltage	V <sub>OL1</sub>	—	0.4	V	I <sub>OL</sub> = 2.1 mA; V <sub>CC</sub> = 4.5V
	V <sub>OL2</sub>	—	0.2	V	I <sub>OL</sub> = 100 μA; V <sub>CC</sub> = V <sub>CC</sub> Min.
High-level output voltage	V <sub>OH1</sub>	2.4	—	V	I <sub>OH</sub> = -400 μA; V <sub>CC</sub> = 4.5V
	V <sub>OH2</sub>	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA; V <sub>CC</sub> = V <sub>CC</sub> Min.
Input leakage current	I <sub>LI</sub>	-10	10	μA	V <sub>IN</sub> = 0.1V to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	-10	10	μA	V <sub>OUT</sub> = 0.1V to V <sub>CC</sub>
Pin capacitance (all inputs/outputs)	C <sub>INT</sub>	—	7	pF	<b>(Note 1)</b> TA = +25°C, F <sub>CLK</sub> = 1 MHz
Operating current	I <sub>CC</sub> write	—	3	mA	V <sub>CC</sub> = 5.5V
	I <sub>CC</sub> read	—	1 500	mA μA	F <sub>CLK</sub> = 3 MHz; V <sub>CC</sub> = 5.5V F <sub>CLK</sub> = 1 MHz; V <sub>CC</sub> = 3.0V
Standby current	I <sub>CCS</sub>	—	100	μA	CLK = CS = 0V; V <sub>CC</sub> = 5.5V
			30	μA	CLK = CS = 0V; V <sub>CC</sub> = 3.0V DI = PE = V <sub>SS</sub> ORG = V <sub>SS</sub> or V <sub>CC</sub>

**Note 1:** This parameter is periodically sampled and not 100% tested.

# 93LC76/86

**TABLE 1-2: AC CHARACTERISTICS**

<b>AC CHARACTERISTICS</b>		Applicable over recommended operating ranges shown below unless otherwise noted: V <sub>CC</sub> = +2.5V to +6.0V Commercial (C): T <sub>A</sub> = 0°C to +70°C Industrial (I): T <sub>A</sub> = -40°C to +85°C			
<b>Parameter</b>	<b>Symbol</b>	<b>Min.</b>	<b>Max.</b>	<b>Units</b>	<b>Conditions</b>
Clock frequency	F <sub>CLK</sub>	—	3	MHz	4.5V ≤ V <sub>CC</sub> ≤ 6.0V
			2	MHz	2.5V ≤ V <sub>CC</sub> < 4.5V
Clock high time	T <sub>CKH</sub>	200 300	—	ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V
			—	ns	2.5V ≤ V <sub>CC</sub> < 4.5V
Clock low time	T <sub>CKL</sub>	100 200	—	ns	4.5V ≥ V <sub>CC</sub> ≤ 6.0V
			—	ns	2.5V ≤ V <sub>CC</sub> < 4.5V
Chip select setup time	T <sub>CSS</sub>	50 100	—	ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK
			—	ns	2.5V ≤ V <sub>CC</sub> < 4.5V, Relative to CLK
Chip select hold time	T <sub>CSH</sub>	0	—	ns	—
Chip select low time	T <sub>CSL</sub>	250	—	ns	Relative to CLK
Data input setup time	T <sub>DIS</sub>	50 100	—	ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK
			—	ns	2.5V ≤ V <sub>CC</sub> < 4.5V, Relative to CLK
Data input hold time	T <sub>DIH</sub>	50 100	—	ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, Relative to CLK
			—	ns	2.5V ≤ V <sub>CC</sub> < 4.5V, Relative to CLK
Data output delay time	T <sub>PD</sub>	—	100	ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V, C <sub>L</sub> = 100 pF
			250	ns	2.5V ≤ V <sub>CC</sub> < 4.5V, C <sub>L</sub> = 100 pF
Data output disable time	T <sub>CZ</sub>	—	100	ns	4.5V ≤ V <sub>CC</sub> ≤ 6.0V
			500	ns	2.5V ≤ V <sub>CC</sub> < 4.5V <b>(Note 1)</b>
Status valid time	T <sub>SV</sub>	—	200	ns	4.5V ≥ V <sub>CC</sub> ≤ 6.0V, C <sub>L</sub> = 100 pF
			300	ns	2.5V ≤ V <sub>CC</sub> < 4.5V, C <sub>L</sub> = 100 pF
Program cycle time	T <sub>WC</sub>	—	5	ms	Erase/Write mode
	T <sub>EC</sub>	—	15	ms	ERAL mode
	T <sub>WL</sub>	—	30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, V <sub>CC</sub> = 5.0V, Block mode <b>(Note 2)</b>

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at [www.microchip.com](http://www.microchip.com).

**TABLE 1-3: INSTRUCTION SET FOR 93LC76: ORG=1 (1X16 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	X A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

**TABLE 1-4: INSTRUCTION SET FOR 93LC76: ORG=0 (X8 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	14
ERASE	1	11	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	14

**TABLE 1-5: INSTRUCTION SET FOR 93LC86: ORG=1 (X16 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

**TABLE 1-6: INSTRUCTION SET FOR 93LC86: ORG=0 (X8 ORGANIZATION)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	14
ERASE	1	11	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	14

# 93LC76/86

---

## 2.0 PRINCIPLES OF OPERATION

When the ORG pin is connected to Vcc, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an erase/write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-impedance state on the falling edge of the CS.

### 2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL and WRAL). As soon as CS is high, the device is no longer in the Standby mode.

An instruction following a Start condition will only be executed if the required amount of opcode, address and data bits for any particular instruction are clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become "don't care" bits until a new Start condition is detected.

### 2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

## 2.3 Erase/Write Enable and Disable (EWEN, EWDS)

The 93LC76/86 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

## 2.4 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

## 3.0 DEVICE OPERATION

### 3.1 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16-bit (x16 organization) or 8-bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay ( $T_{PD}$ ). Sequential read is possible when CS is held high and clock transitions continue. The memory address pointer will automatically increment and output data sequentially.

### 3.2 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of CLK as the last address bit (A0) is clocked in. At this point, the CLK, CS and DI inputs become "don't cares".

The DO pin indicates the Ready/ $\overline{\text{Busy}}$  status of the device if the CS is high. The Ready/ $\overline{\text{Busy}}$  status will be displayed on the DO pin until the next Start bit is received as long as CS is high. Bringing the CS low will place the device in Standby mode and cause the DO pin to enter the high-impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The erase cycle takes 3 ms per word (typical).

### 3.3 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of CLK as the last data bit (D0) is clocked in. At this point, the CLK, CS and DI inputs become "don't cares".

The DO pin indicates the Ready/ $\overline{\text{Busy}}$  status of the device if the CS is high. The Ready/ $\overline{\text{Busy}}$  status will be displayed on the DO pin until the next Start bit is received as long as CS is high. Bringing the CS low will place the device in Standby mode and cause the DO pin to enter the high-impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written and the device is ready for another instruction.

The write cycle takes 3 ms per word (typical).

### 3.4 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the erase cycle except for the different opcode. The ERAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the Least Significant 8 or 9 address bits are "don't care" bits, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is ensured at  $V_{CC} = +4.5V$  to  $+6.0V$ .

The DO pin indicates the Ready/ $\overline{\text{Busy}}$  status of the device if the CS is high. The Ready/ $\overline{\text{Busy}}$  status will be displayed on the DO pin until the next Start bit is received as long as CS is high. Bringing the CS low will place the device in Standby mode and cause the DO pin to enter the high-impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been erased and is ready for another instruction.

The ERAL cycle takes 15 ms maximum (8 ms typical).

### 3.5 Write All (WRAL)

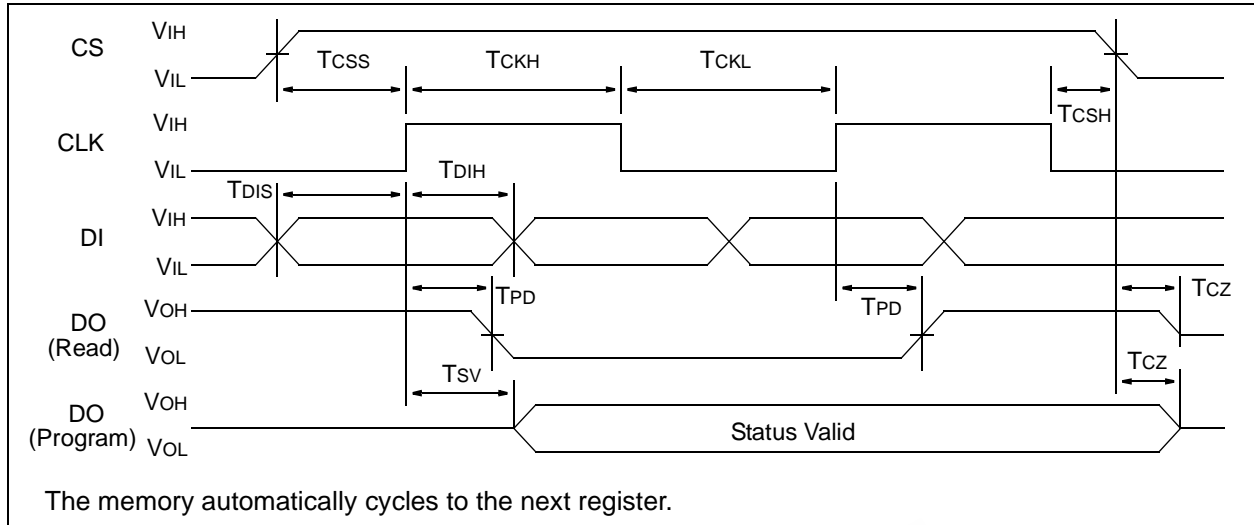
The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the Least Significant 8 or 9 address bits are "don't cares", depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is ensured at  $V_{CC} = +4.5V$  to  $+6.0V$ .

The DO pin indicates the Ready/ $\overline{\text{Busy}}$  status of the device if the CS is high. The Ready/ $\overline{\text{Busy}}$  status will be displayed on the DO pin until the next Start bit is received as long as CS is high. Bringing the CS low will place the device in Standby mode and cause the DO pin to enter the high-impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been written and is ready for another instruction.

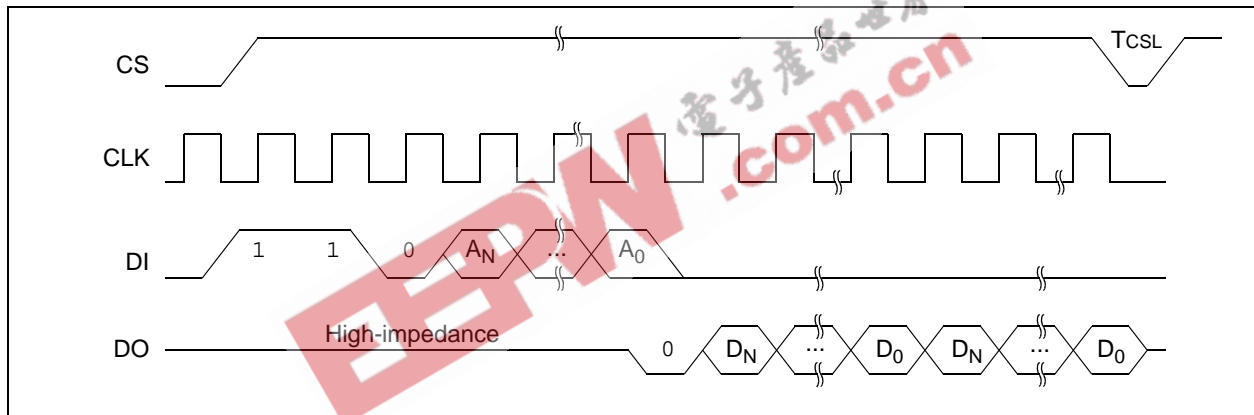
The WRAL cycle takes 30 ms maximum (16 ms typical).

# 93LC76/86

**FIGURE 3-1: SYNCHRONOUS DATA TIMING**



**FIGURE 3-2: READ**



**FIGURE 3-3: EWEN**

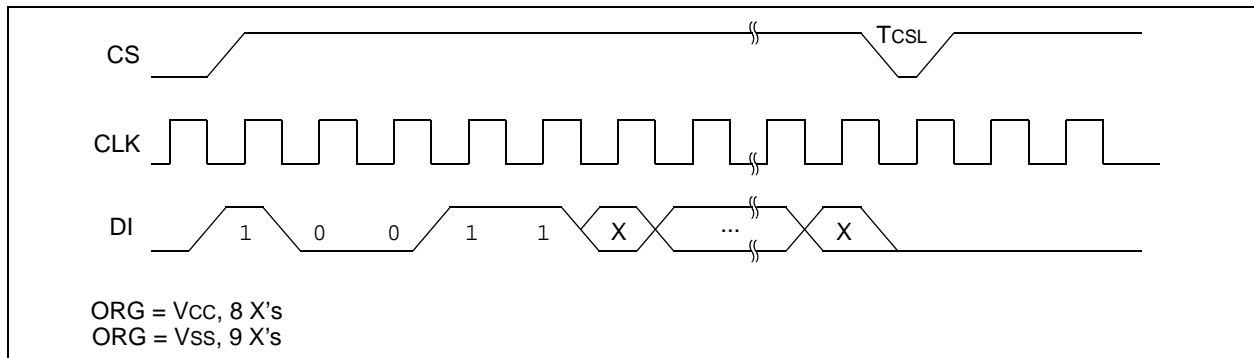




FIGURE 3-4: EWDS

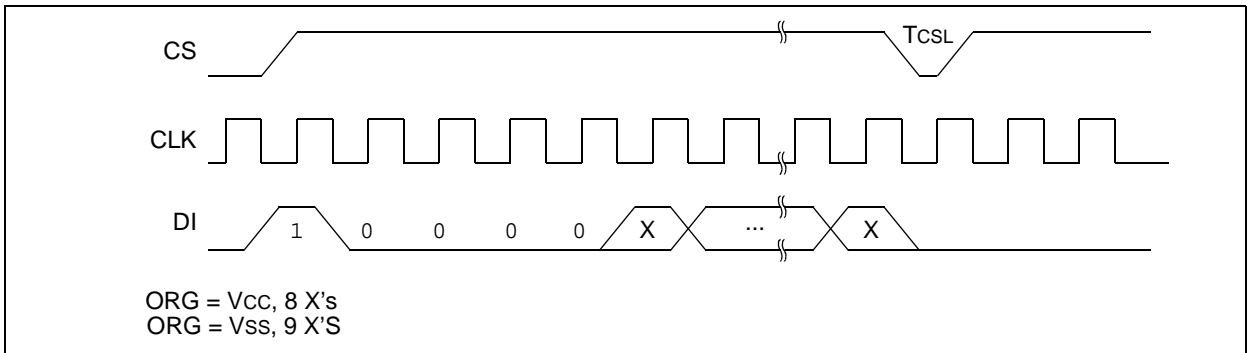


FIGURE 3-5: WRITE

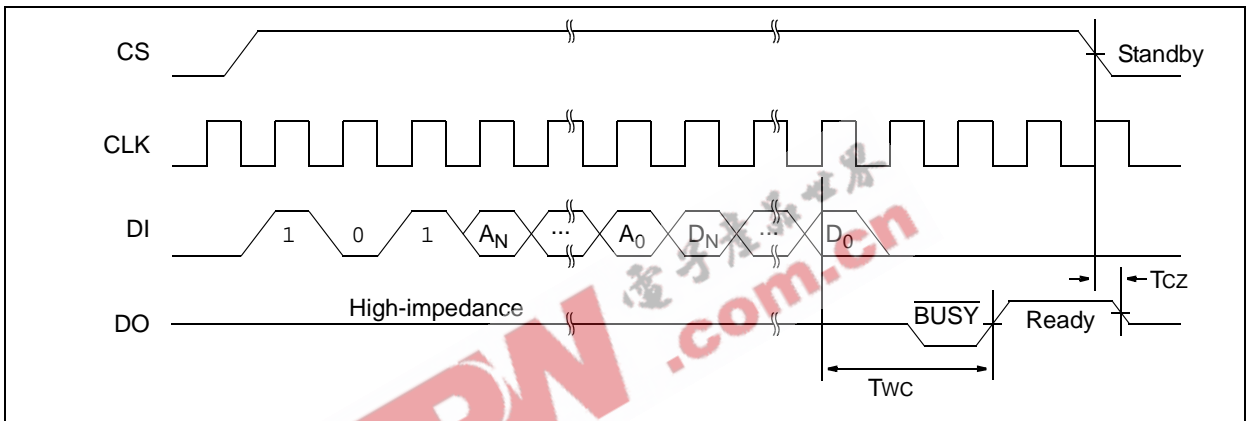
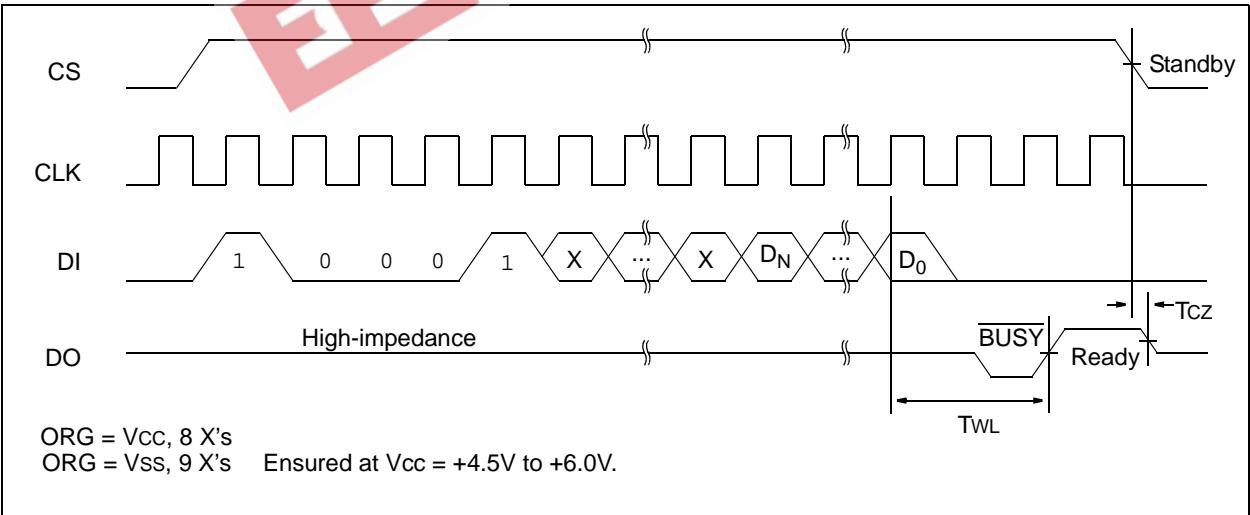
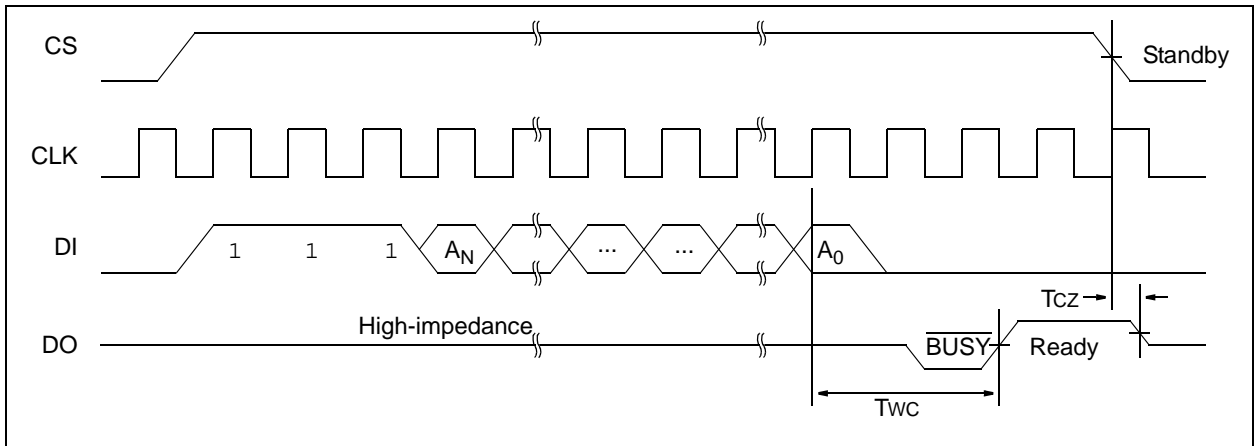


FIGURE 3-6: WRAL

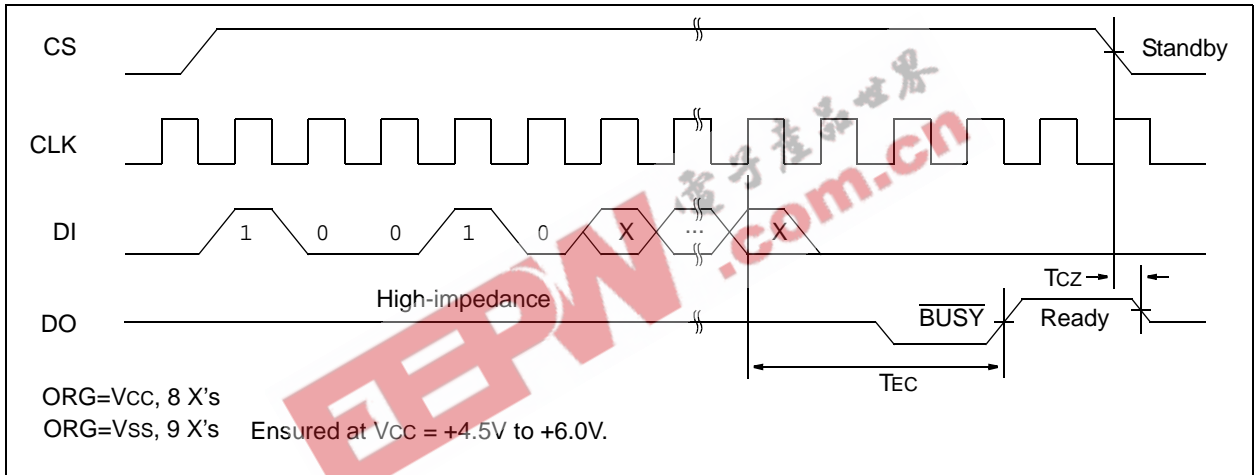


# 93LC76/86

**FIGURE 3-7: ERASE**



**FIGURE 3-8: ERAL**



## 4.0 PIN DESCRIPTIONS

TABLE 4-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
PE	Program Enable
Vcc	Power Supply

### 4.1 Chip Select (CS)

A high level selects the device. A low level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated will be completed, regardless of the CS input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum ( $T_{CSL}$ ) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

### 4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LC76/86. Opcode, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time ( $T_{CKH}$ ) and clock low time ( $T_{CKL}$ ). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "don't care" if CS is low (device deselected). If CS is high, but Start condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for Start condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all opcode, address, and data bits before an instruction is executed (see Table 1-3 through Table 1-6 for more details). CLK and DI then become don't care inputs waiting for a new Start condition to be detected.

**Note:** CS must go low between consecutive instructions, except when performing a sequential read (Refer to **Section 3.1 "READ"** for more detail on sequential reads).

### 4.3 Data In (DI)

Data In is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

### 4.4 Data Out (DO)

Data Out is used in the Read mode to output data synchronously with the CLK input ( $T_{PD}$  after the positive edge of CLK).

This pin also provides Ready/Busy status information during erase and write cycles. Ready/Busy status information is available when CS is high. It will be displayed until the next Start bit occurs as long as CS stays high.

### 4.5 Organization (ORG)

When ORG is connected to Vcc, the x16 memory organization is selected. When ORG is tied to Vss, the x8 memory organization is selected. There is an internal pull-up resistor on the ORG pin that will select x16 organization when left unconnected.

### 4.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is floated or tied to Vcc, the device can be programmed. If the PE pin is tied to Vss, programming will be inhibited. There is an internal pull-up on this device that enables programming if this pin is left floating.

# 93LC76/86

---

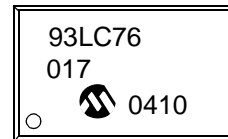
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

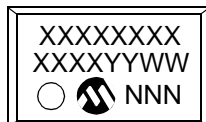
8-Lead PDIP



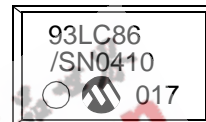
Example



8-Lead SOIC (.150")

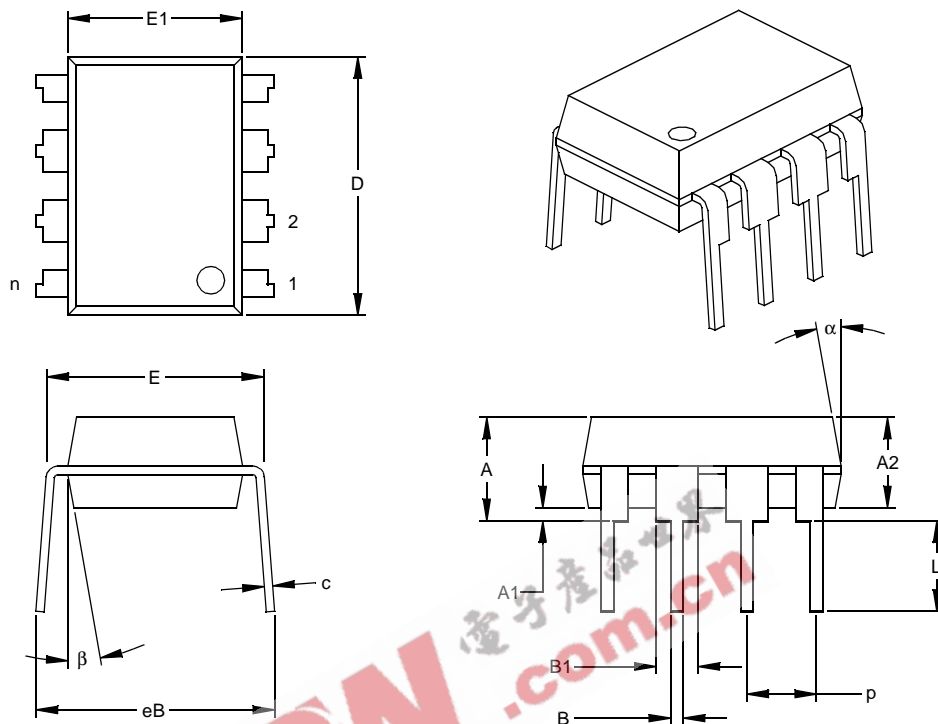


Example



EEPW 电子产业网 .com.cn

## 8-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



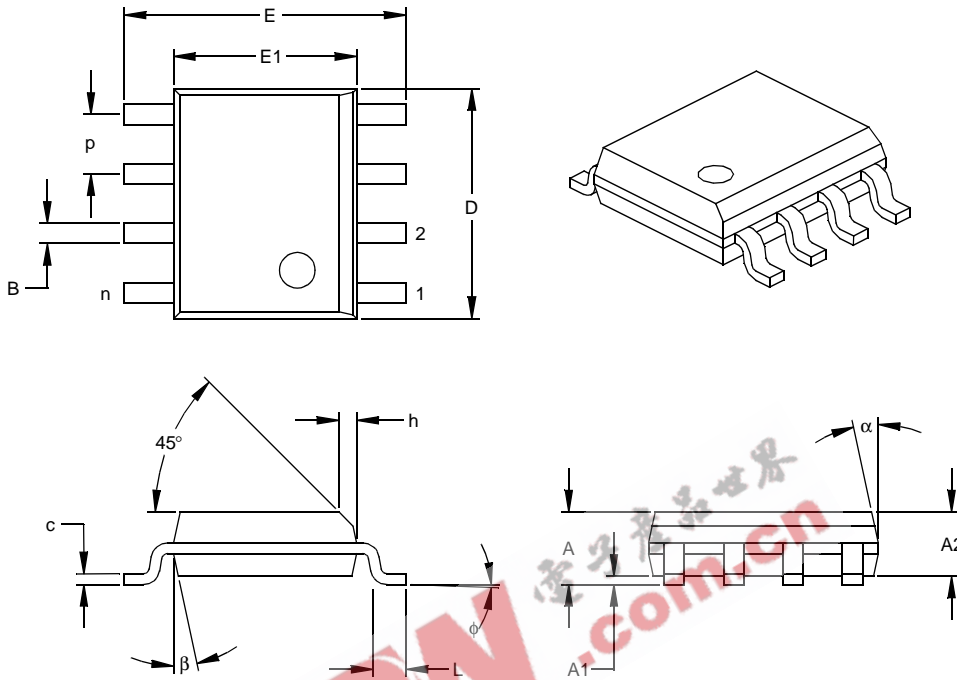
Dimension	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	P		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-001  
 Drawing No. C04-018

# 93LC76/86

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil Body (SOIC)



Dimension	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	P		.050		1.27		
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-012  
 Drawing No. C04-057

## APPENDIX A: REVISION HISTORY

### Revision E

Added note to page 1 header (Not recommended for new designs).

Added Section 5.0: Package Marking Information.

Added On-line Support page.

Updated document format.

EEPW 电子產品世界  
.com.cn

[查询"93LC76T-I/SN"供应商](#)

# 93LC76/86

---

---

NOTES:

EEPW 电子產品世界  
.com.cn



## ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

### Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

**[www.microchip.com](http://www.microchip.com)**

The file transfer site is available by using an FTP service to connect to:

**<ftp://ftp.microchip.com>**

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

## SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

042003

# 93LC76/86

---

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager Total Pages Sent \_\_\_\_\_  
RE: Reader Response  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: 93LC76/86

Literature Number: DS21131E

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this document easy to follow? If not, why?

---

---

4. What additions to the document do you think would enhance the structure and subject?

---

---

5. What deletions from the document could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device	93LC76/86: Microwire Serial EEPROM 93LC76T/86T: Microwire Serial EEPROM (Tape and Reel)		
Temperature Range	Blank = 0°C to +70°C I = -40°C to +85°C		
Package	P = Plastic DIP (300 mil Body), 8-lead SN = Plastic SOIC (150 mil Body), 8-lead		

## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

### New Customer Notification System

Register on our web site ([www.microchip.com/cn](http://www.microchip.com/cn)) to receive the most current information on our products.

[查询"93LC76T-I/SN"供应商](#)

# 93LC76/86

---

---

NOTES:

EEPW 电子产品世界  
.com.cn

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

**Trademarks**

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICTail, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rPICDEM, Select Mode, Smart Serial, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: www.microchip.com

#### Atlanta

3780 Mansell Road, Suite 130  
Alpharetta, GA 30022  
Tel: 770-640-0034  
Fax: 770-640-0307

#### Boston

2 Lan Drive, Suite 120  
Westford, MA 01886  
Tel: 978-692-3848  
Fax: 978-692-3821

#### Chicago

333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

4570 Westgrove Drive, Suite 160  
Addison, TX 75001  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

2767 S. Albright Road  
Kokomo, IN 46902  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888  
Fax: 949-263-1338

#### San Jose

1300 Terra Bella Avenue  
Mountain View, CA 94043  
Tel: 650-215-1444  
Fax: 650-961-0286

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Unit 706B  
Wan Tai Bei Hai Bldg.  
No. 6 Chaoyangmen Bei Str.  
Beijing, 100027, China  
Tel: 86-10-85282100  
Fax: 86-10-85282104

#### China - Chengdu

Rm. 2401-2402, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-86766200  
Fax: 86-28-86766599

#### China - Fuzhou

Unit 28F, World Trade Plaza  
No. 71 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7503506  
Fax: 86-591-7503521

#### China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Shanghai

Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700  
Fax: 86-21-6275-5060

#### China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza  
No. 5022 Binhe Road, Futian District  
Shenzhen 518033, China  
Tel: 86-755-82901380  
Fax: 86-755-8295-1393

#### China - Shunde

Room 401, Hongjian Building, No. 2  
Fengxiangnan Road, Ronggui Town, Shunde  
District, Foshan City, Guangdong 528303, China  
Tel: 86-757-28395507 Fax: 86-757-28395571

#### China - Qingdao

Rm. B505A, Fullhope Plaza,  
No. 12 Hong Kong Central Rd.  
Qingdao 266071, China  
Tel: 86-532-5027355 Fax: 86-532-5027205

#### India

Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaughnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-22290061 Fax: 91-80-22290062

#### Japan

Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

#### Korea

168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or  
82-2-558-5934

#### Singapore

200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-6334-8870 Fax: 65-6334-8850

#### Taiwan

Kaohsiung Branch  
30F - 1 No. 8  
Min Chuan 2nd Road  
Kaohsiung 806, Taiwan  
Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan

Taiwan Branch  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Austria

Durisolstrasse 2  
A-4600 Wels  
Austria  
Tel: 43-7242-2244-399  
Fax: 43-7242-2244-393

#### Denmark

Regus Business Centre  
Lautrup hoy 1-3  
Ballerup DK-2750 Denmark  
Tel: 45-4420-9895 Fax: 45-4420-9910

#### France

Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany

Steinheilstrasse 10  
D-85737 Ismaning, Germany  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy

Via Quasimodo, 12  
20025 Legnano (MI)  
Milan, Italy  
Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands

Waegenburghtplein 4  
NL-5152 JR, Drunen, Netherlands  
Tel: 31-416-690399  
Fax: 31-416-690340

#### United Kingdom

505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820