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TLC59213A SLVS867A – MAY 2009–REVISED MARCH 2010

TLC59213

8-BIT PARALLEL IN/OUT DARLINGTON SOURCE DRIVER WITH LATCH

Check for Samples: TLC59213, TLC59213A

FEATURES

- Output Current on Each Channel (I_{OUT} Max = -500 mA)
- V_{CE(sus)} = 13.2 V
- Input Compatible With TTL/5-V CMOS
- Clear (CLR) and Clock (CLK) TTL/CMOS Control Inputs
- CLR Control Input to Off the Output
- Darlington Source Driver
- Clock Input Up to 1 MHz
- Enhanced Hold Time (t_h) on TLC59213A
- Temperature Range: –40°C to 85°C

APPLICATIONS

- Lamp and Display (LED)
- Hammer
- Relay

Displa	ay (LED)		
NO	OR PW PAG	СКА	GE
	(TOP VIE	W)	
CLR [1 0	20	□ ^v cc
D1 🗌	2	19	_ Y1
D2 [3	18] Y2
D3 🗌	4	17] Y3
D4 🗌	5	16] Y4
D5 🗌	6	15] Y5
D6 🗌	7	14] Y6
D7 🗌	8	13] Y7
D8 [9	12] Y8
CLK [10	11	GND

DESCRIPTION

The TLC59213 and TLC59213A are 8-bit source drivers with input latch with CLK input and $\overline{\text{CLR}}$ to set the output OFF. The TLC59213 and TLC59213A have large output source currents up to 500 mA with Darlington transistor and collectors tied to V_{CC}. These feature make the device optimum level of driving the matrix of ink jet printer head, LEDs, and the scan-side of resistor's matrix. The TLC59213 and TLC59213A differ only in the Data Hold Time Specification (t_h).

The clamp diode is between output and ground for switching inductive load.

All inputs are TTL/CMOS, which enable to any logic-level inputs such as MCU, CPU or SN74LV594 (serial to parallel) and the output enable LED matrix display. It can also be used with another device sink driver such as TLC59210, TLC59211 and TLC59212.

T _A	P	ACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
- 10	PDIP – N	Tube of 20	TLC59213IN	TLC59213IN
	TSSOP – PW	Reel of 2000	TLC59213IPWR	Y59213
-40°C to 85°C	PDIP – N	Tube of 20	TLC59213AIN	TLC59213AIN
	TSSOP – PW	Reel of 2000	TLC59213AIPWR	V/500404
	1550P - PW	Reel of 250	TLC59213AIPWT	- Y59213A

ORDERING INFORMATION⁽¹⁾

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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FUNCTION TABLE (EACH LATCH)⁽¹⁾

	INPUTS	OUTPUT	
CLR	CLK	D	Y
L	Х	Х	Z (OFF)
н	Ť	L	Z (OFF)
н	Ť	Н	H (ON)
н	L	Х	Y ₀
Н	\downarrow	Х	Y ₀

(1) L: Low-level

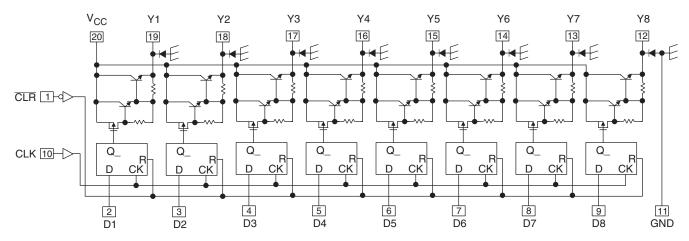
H: High-level

X: Irrelevant

↑: Rising edge

↓: Falling edge Z : High-impedance (off)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{DD}	Supply voltage range			-0.5	15	V
VI	Input voltage range	Input voltage range				V
	Collector-emitter voltage				15	V
I _O	Peak output current				-500	mA
I _{IK}	Input clamp current	V ₁ < 0 V			-20	mA
I _{OK}	Output clamp current	V _O < 0 V			-500	mA
0	Deckage thermal impedance ⁽²⁾	N package			69	°C/W
θ_{JA}	Package thermal impedance ⁽²⁾	PW package			83	°C/VV
T _{stg}	Storage temperature range				150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.



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RECOMMENDED OPERATING CONDITIONS

			CONDITIONS	MIN	MAX	UNIT
V _{CC}	Supply voltage			4.5	13.2	V
VIH	High-level input voltage			2		V
VIL	Low-level input voltage				0.8	V
		N package	Duty cycle < 10%		400	
	Output ourport (0, choose all)		Duty cycle < 50%		200	mA
I _O	Output current (8 channel)		Duty cycle < 10%		350	
		PW package	Duty cycle < 50%		170	
T _A	Operating free-air temperature				85	°C

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT	
I _{CEX}	Output leakage current	V _{CC} = 13.2 V, Outputs	off			2	μA	
		I _{OUT} = -350 mA				2.35		
V _{CE(sus)} Output saturation voltage	I _{OUT} = -225 mA			2.15	V			
		I _{OUT} = -100 mA				1.96		
II.	Input current	$V_{CC} = 13.2 \text{ V}, \text{ V}_{I} = 0 \text{ o}$	r 13.2 V			1	μA	
V _f	Clamp forward voltage	I _f = -350 mA		-2			V	
	Current current	V _{CC} = 13.2 V,	All outputs OFF	4.6		13		
ICC	Supply current	$V_{I} = 0 \text{ or } 13.2 \text{ V}$	or 13.2 V All outputs ON		4.8	13	mA	
CI	Input capacitance		·			10	pF	

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted), see Figure 3

	P	ARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
+	Sotup time	D before CLK ↑			50		ns
t _{su} Setup time		CLR high before	e CLK ↑		50		ns
		TLC59213, TLC59213A		$T_A = -40^{\circ}C \text{ to } 85^{\circ}C$	50		
t _h	Hold time		TLC59213	$T_A = 0^{\circ}C$ to $70^{\circ}C$	25		ns
			TLC59213A	$T_A = 0^{\circ}C$ to 70°C, $V_{CC} = 4.5$ V to 5.5 V	15	15	
			TLC59213A	T_{A} = 0°C to 70°C, V_{CC} = 10.8 V to 13.2 V	19		
tw	Pulse width	CLK, CLR			100		ns

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted), see Figure 3

	PARAMETER	FROM TO		TEST	T _A = 25°C	$T_A = -40^{\circ}C \text{ to } 85^{\circ}C$	UNIT
	PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS	MIN TYP MAX	MIN MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high level output	CLK	Y	RL = 25 Ω, C _L = 15 pF	107 200	250	ns
t _{PHL}	Propagation delay time,	CLK	Y	RL = 25 Ω,	111 200	250	20
t _{PHLR}	high-to-low level output	CLR	Y	C _L = 15 pF	104 200	250	ns

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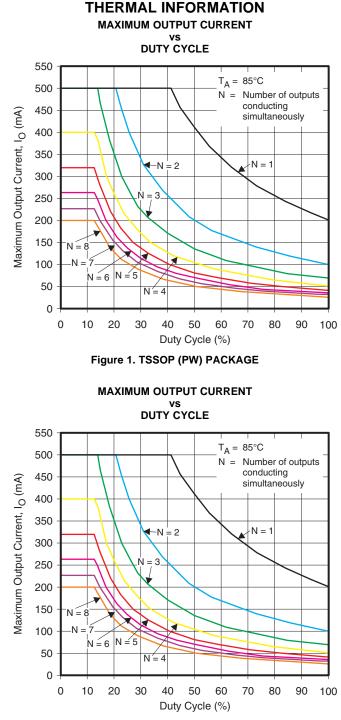
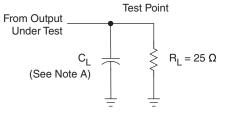


Figure 2. DIP (N) PACKAGE

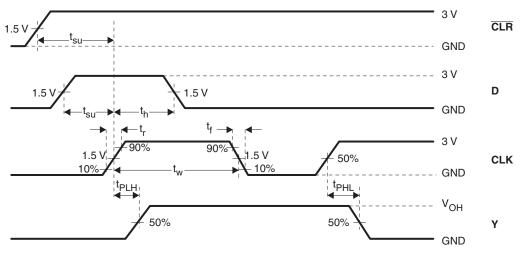
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PARAMETER MEASUREMENT INFORMATION







VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z₀ = 50 Ω , t_r \leq 3 ns, and t_f \leq 3 ns.
- C. The outputs are measured one at a time with one transition per measurement.

Figure 3. Test Circuit and Voltage Waveforms

6

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APPLICATION INFORMATION

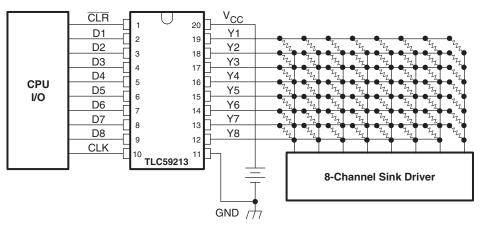


Figure 4. Example of LED Display Connection

16-Apr-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC59213AIN	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC59213AIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC59213AIPWT	PREVIEW	TSSOP	PW	20	250	TBD	Call TI	Call TI
TLC59213IN	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC59213IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

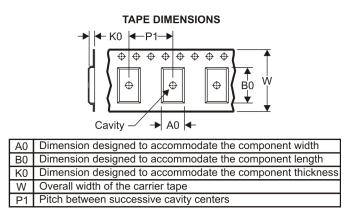
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

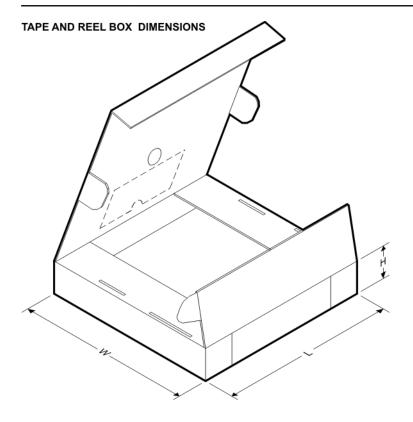


*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59213AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC59213AIPWT	TSSOP	PW	20	250	180.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC59213IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

20-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59213AIPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
TLC59213AIPWT	TSSOP	PW	20	250	190.5	212.7	31.8
TLC59213IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0

MECHANICAL DATA

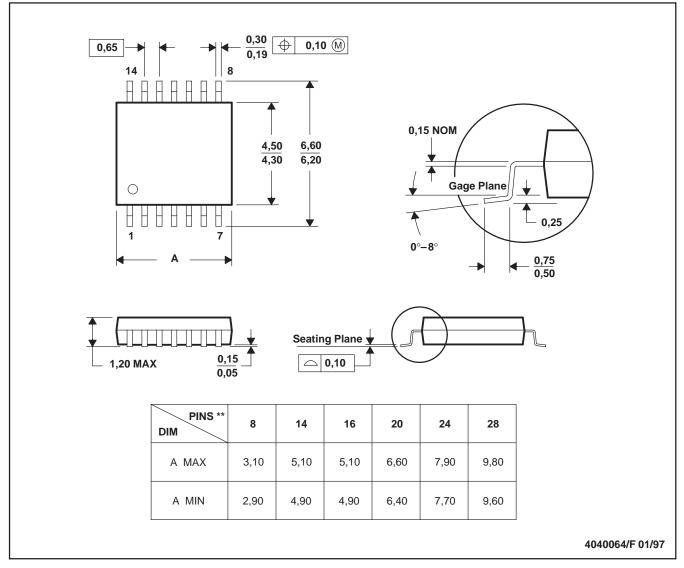
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PW (R-PDSO-G**)

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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