19-4014; Rev 1; 9/06

EVALUATION KIT AVAILABLE

Dual-Output (+ and -) DC-DC Converters for CCD

General Description

The MAX8614A/MAX8614B dual-output step-up DC-DC converters generate both a positive and negative supply voltage that are each independently regulated. The positive output delivers up to 50mA while the inverter supplies up to 100mA with input voltages between 2.7V and 5.5V. The MAX8614A/MAX8614B are ideal for powering CCD imaging devices and displays in digital cameras and other portable equipment.

The MAX8614A/MAX8614B generate an adjustable positive output voltage up to +24V and a negative output down to 16V below the input voltage. The MAX8614B has a higher current limit than the MAX8614A. Both devices operate at a fixed 1MHz frequency to ease noise filtering in sensitive applications and to reduce external component size.

Additional features include pin-selectable power-on sequencing for use with a wide variety of CCDs, True Shutdown™, overload protection, fault flag, and internal soft-start with controlled inrush current.

The MAX8614A/MAX8614B are available in a space-saving 3mm x 3mm 14-pin TDFN package and are specified over the -40°C to +85°C extended temperature range.

Applications

CCD Bias Supplies and OLED Displays

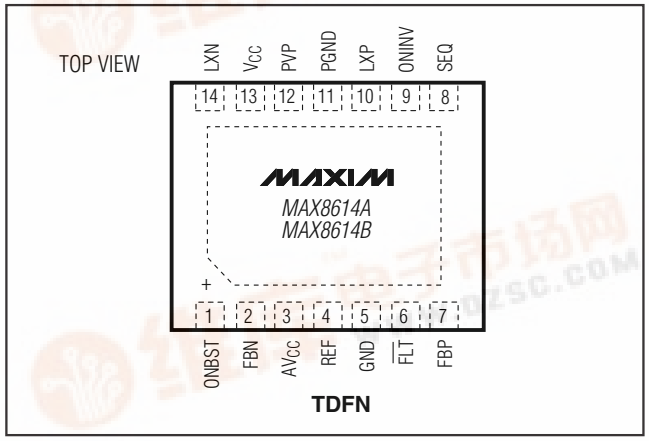
Digital Cameras

Camcorders and Portable Multimedia

PDAs and Smartphones

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Pin Configuration



Features

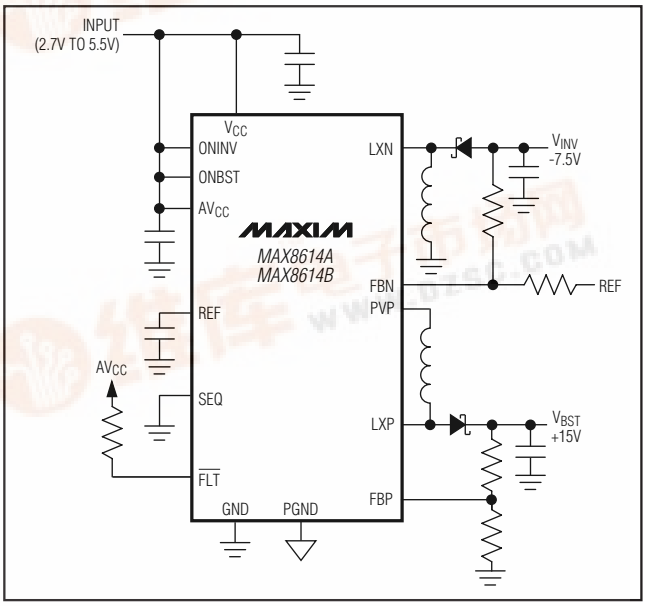
- Dual Output Voltages (+ and -)
- Adjustable Up to +24V and Down to -10V at 5.5V$_{IN}$
- Output Short/Overload Protection
- True Shutdown on Both Outputs
- Controlled Inrush Current During Soft-Start
- Selectable Power-On Sequencing
- Up to 90% Efficiency
- 1µA Shutdown Current
- 1MHz Fixed-Frequency PWM Operation
- Fault-Condition Flag
- Thermal Shutdown
- Small, 3mm x 3mm, 14-Pin TDFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	ILIM BST/ INV	PKG CODE
MAX8614AETD+	-40°C to +85°C	14 TDFN 3mm x 3mm (T1433-2)	ABG	0.44/ 0.33	T1433+
MAX8614BETD+	-40°C to +85°C	14 TDFN 3mm x 3mm (T1433-2)	ABH	0.8/ 0.75	T1433+

+Denotes lead-free package.

Typical Operating Circuit



Dual-Output (+ and -) DC-DC Converters for CCD

ABSOLUTE MAXIMUM RATINGS

V_{CC}, AV_{CC} to GND .....-0.3V to +6V
LXN to V_{CC} .....-18V to +0.3V
LXP to PGND .....-0.3V to +33V
REF, ONINV, ONBST, SEQ, FBN, FBP
$\overline{FLT}$ to GND .....-0.3V to (AV_{CC} + 0.3)V
PVP to GND .....-0.3V to (V_{CC} + 0.3)V
AV_{CC} to V_{CC} .....-0.3V to +0.3V
PGND to GND .....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C Multilayer Board)
14-Pin 3mm x 3mm TDFN (derate 18.2mW/°C above T_A = +70°C) 1454.4mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{AVCC} = V_{ONINV} = V_{ONBST} = 3.6V, PGND = SEQ = GND, C6 = 0.22µF, C1 = 2.2µF, C2 = 4.7µF, Figure 1, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AV_{CC} and V_{CC} Voltage Range	(Note 1)	2.7		5.5	V
UVLO Threshold	V_{CC} rising	2.42	2.55	2.66	V
UVLO Hysteresis			25		mV
Step-Up Output Voltage Adjust Range		V_{AVCC}		24	V
Inverter Output Voltage Adjust Range	V_{INV} - V_{CC} (Note 2)	-16		0	V
LXP Current Limit	MAX8614B	0.7	0.8	0.9	A
	MAX8614A	0.34	0.44	0.52	
LXP Short-Circuit Current Limit	MAX8614B	0.90	1.05	1.20	A
	MAX8614A	0.52	0.61	0.70	
LXN Current Limit	MAX8614B	0.65	0.75	0.85	A
	MAX8614A	0.28	0.33	0.38	
LXN On-Resistance	V_{CC} = 3.6V		0.6	1.1	Ω
LXP On-Resistance	V_{CC} = 3.6V		0.625		Ω
PVP On-Resistance	V_{CC} = 3.6V		0.15	0.3	Ω
Maximum Duty Cycle	Step-up and inverter	82	90		%
Quiescent Current (Switching, No Load)	I_{AVCC}		0.75	1.4	mA
	I_{VCC}		2	3	
Quiescent Current (No Switching, No Load)	I_{AVCC}		400	800	µA
	I_{VCC}		8	15	
Shutdown Supply Current	T_A = +25°C		0.1	5	µA
	T_A = +85°C		0.1		
FBP Line Regulation	V_{CC} = 2.7V to 5.5V		-20		mV/D
FBN Line Regulation	V_{CC} = 2.7V to 5.5V		20		mV/(D - 0.5)

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{AVCC} = V_{ONINV} = V_{ONBST} = 3.6V, PGND = SEQ = GND, C6 = 0.22µF, C1 = 2.2µF, C2 = 4.7µF, Figure 1, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FBP Load Regulation	I_{LXP} = $I_{ILIMMIN}$, MAX8614B			-15		mV/A
	I_{LXP} = $I_{ILIMMIN}$, MAX8614A			-35		
FBN Load Regulation	I_{LXN} = $I_{ILIMMIN}$, MAX8614B			17.5		mV/A
	I_{LXN} = $I_{ILIMMIN}$, MAX8614A			65		
Oscillator Frequency			0.93	1	1.07	MHz
Soft-Start Interval	Step-up and inverter			10		ms
Overload-Protection Fault Delay				100		ms
FBP, FBN, REFERENCE						
REF Output Voltage	No load		1.24	1.25	1.26	V
REF Load Regulation	0µA < I_{REF} < 50µA			10		mV
REF Line Regulation	3.3V < V_{AVCC} < 5.5V			2	5	mV
FBP Threshold Voltage	No load		0.995	1.010	1.025	V
FBN Threshold Voltage	No load		-10	0	+10	mV
FBP Input Leakage Current	V_{FBP} =1.025V	T_A = +25°C	-50	+5	+50	nA
		T_A = +85°C		+5		
FBN Input Leakage Current	FBN = -10mV	T_A = +25°C	-50	+5	+50	nA
		T_A = +85°C		+5		
LXN Input Leakage Current	V_{LXN} = -12V	T_A = +25°C	-5	+0.1	+5	µA
		T_A = +85°C		+0.1		
LXP Input Leakage Current	V_{LXP} = 23V	T_A = +25°C	-5	+0.1	+5	µA
		T_A = +85°C		+0.1		
PVP Input Leakage Current	V_{PVP} = 0V	T_A = +25°C	-5	+0.1	+5	µA
		T_A = +85°C		+0.1		
$\overline{FLT}$ Input Leakage Current	$V_{\overline{FLT}}$ = 3.6V	T_A = +25°C	-1	+0.1	+1	µA
		T_A = +85°C		+0.1		
$\overline{FLT}$ Input Resistance	Fault mode, T_A = +25°C			10	20	Ω
ONINV, ONBST, SEQ LOGIC INPUTS						
Logic-Low Input	2.7V < V_{AVCC} < 5.5V				0.5	V
Logic-High Input	2.7V < V_{AVCC} < 5.5V		1.6			V
Bias Current	T_A = +25°C			0.1	1	µA

Dual-Output (+ and -) DC-DC Converters for CCD

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{AVCC} = V_{ONINV} = V_{ONBST} = V_{EN} = 3.6V, PGND = SEQ = GND, C6 = 0.22µF, C1 = 2.2µF, C2 = 6.7µF, Figure 1, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
A_{VCC} = V_{CC} Voltage Range	(Note 1)	3		5.5	V
UVLO Threshold	V_{CC} rising	2.42		2.82	V
Step-Up Output Voltage Adjust Range		V_{AVCC}		24	V
Inverter Output Voltage Adjust Range	V_{INV} - V_{CC} (Note 2)	-16		0	V
LXP Current Limit	MAX8614B	0.7		0.9	A
	MAX8614A	0.34		0.52	
LXP Short-Circuit Current Limit	MAX8614B	0.9		1.2	A
	MAX8614A	0.52		0.70	
LXN Current Limit	MAX8614B	0.65		0.85	A
	MAX8614A	0.28		0.38	
LXN On-Resistance	V_{CC} = 3.6V			1.1	Ω
PVP On-Resistance	V_{CC} = 3.6V			0.3	Ω
Maximum Duty Cycle	Step-up and inverter	82			%
Quiescent Current (Switching, No Load)	I_{AVCC}			1.4	mA
	I_{VCC}			3	
Quiescent Current (No Switching, No Load)	I_{AVCC}			800	µA
	I_{VCC}			15	
Oscillator Frequency		0.93		1.07	MHz
FBP, FBN, REFERENCE					
REF Output Voltage	No load	1.235		1.260	V
FBP Threshold Voltage	No load	0.995		1.025	V
FBN Threshold Voltage	No load	-10		+10	mV
ONINV, ONBST SEQ LOGIC INPUTS					
Logic-Low Input	2.7V < V_{AVCC} < 5.5V			0.5	V
Logic-High Input	2.7V < V_{AVCC} < 5.5V	1.6			V

Note 1: Output current and on-resistance are specified at 3.6V input voltage. The IC operates to 2.7V with reduced performance.

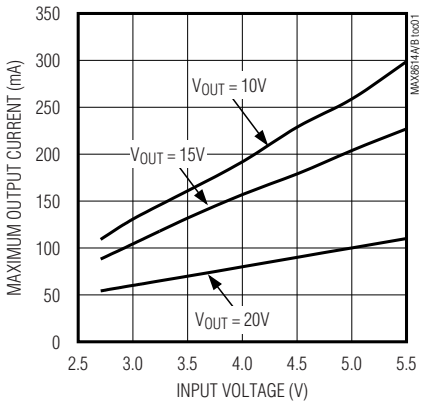
Note 2: The specified maximum negative output voltage is referred to V_{CC}, and not to GND. With V_{CC} = 3.3V, the maximum negative output is then -12.7V.

Note 3: Specifications to -40°C are guaranteed by design, not production tested.

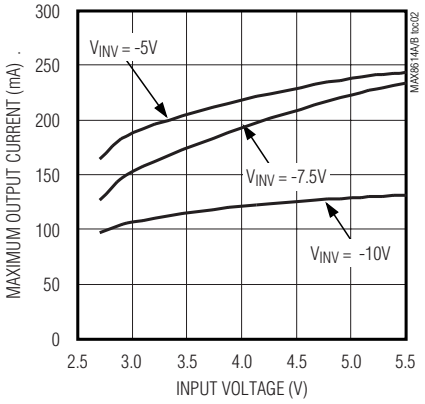
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = V_{AVCC} = 3.6V, SEQ = GND, Figure 1, unless otherwise noted.)

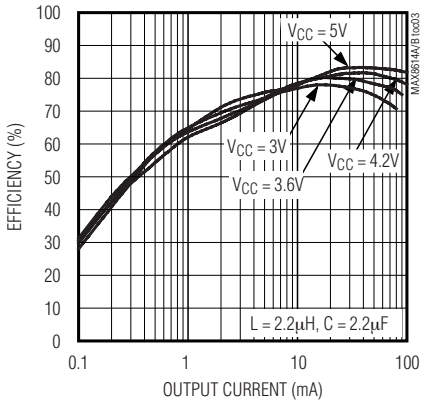
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



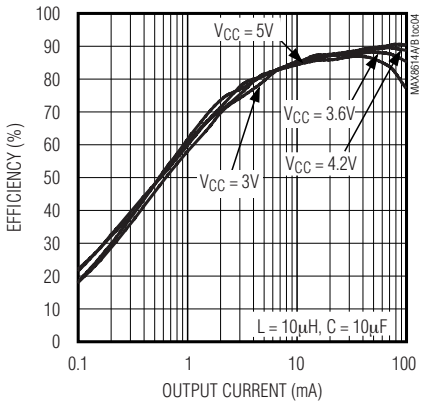
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



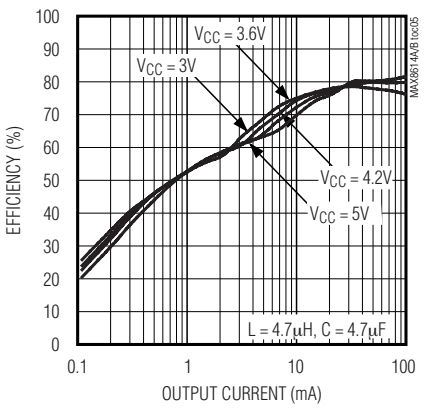
POSITIVE OUTPUT EFFICIENCY vs. OUTPUT CURRENT



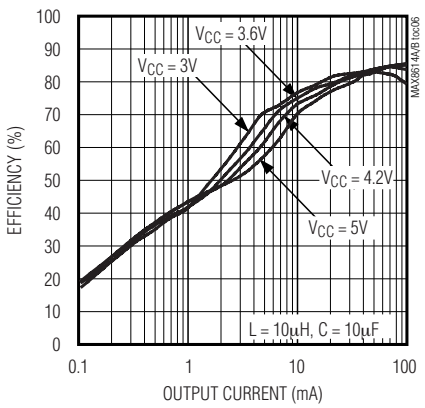
POSITIVE OUTPUT EFFICIENCY vs. OUTPUT CURRENT



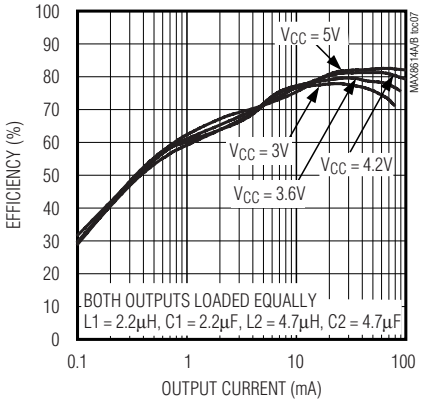
NEGATIVE OUTPUT EFFICIENCY vs. OUTPUT CURRENT



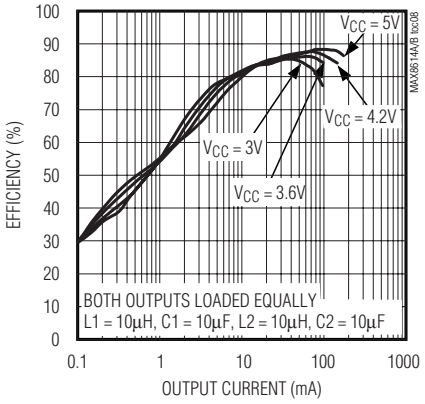
NEGATIVE OUTPUT EFFICIENCY vs. OUTPUT CURRENT



OUTPUT EFFICIENCY vs. OUTPUT CURRENT



OUTPUT EFFICIENCY vs. OUTPUT CURRENT

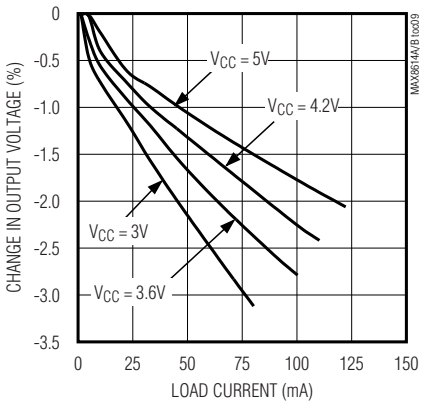


Dual-Output (+ and -) DC-DC Converters for CCD

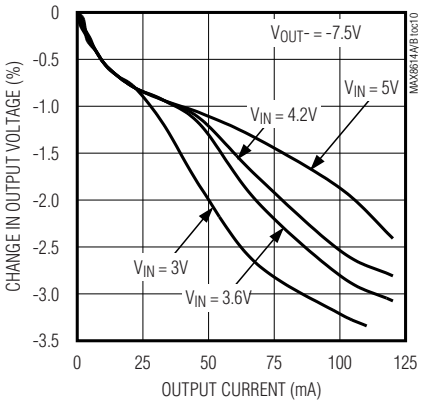
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = V_{AVCC} = 3.6V, SEQ = GND, Figure 1, unless otherwise noted.)

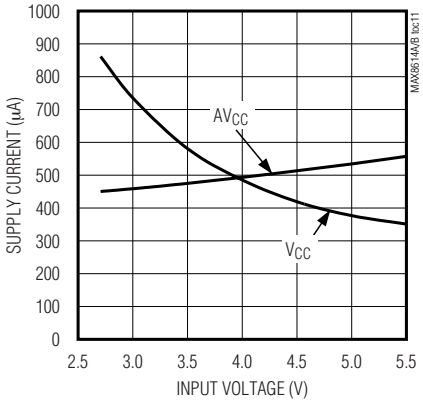
CHANGE IN OUTPUT VOLTAGE vs. LOAD CURRENT (POSITIVE OUTPUT)



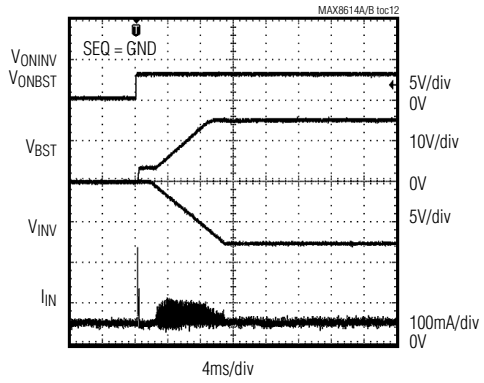
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT (NEGATIVE OUTPUT)



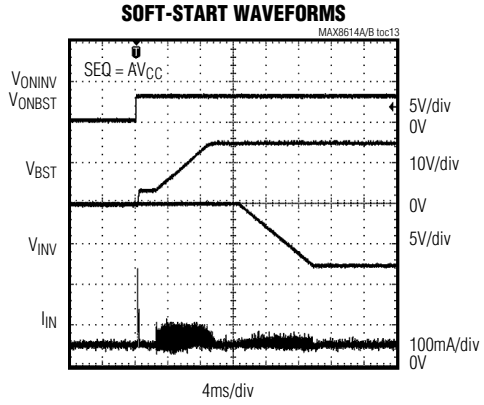
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



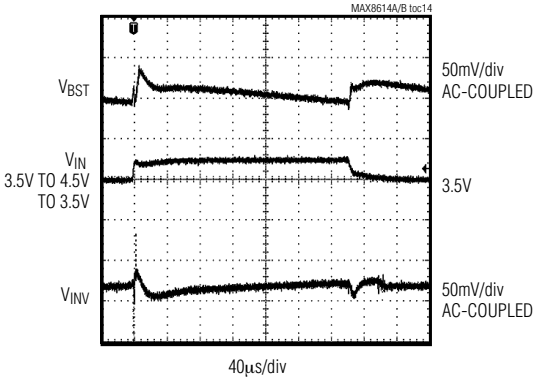
SOFT-START WAVEFORMS



SOFT-START WAVEFORMS



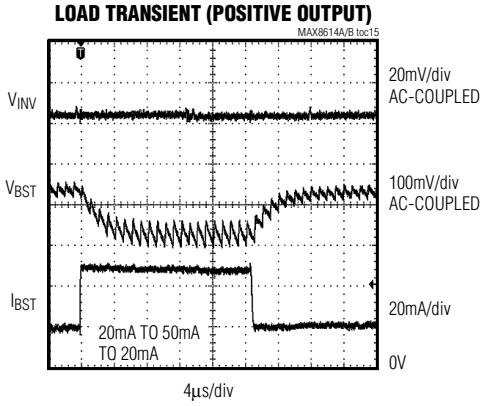
LINE TRANSIENT



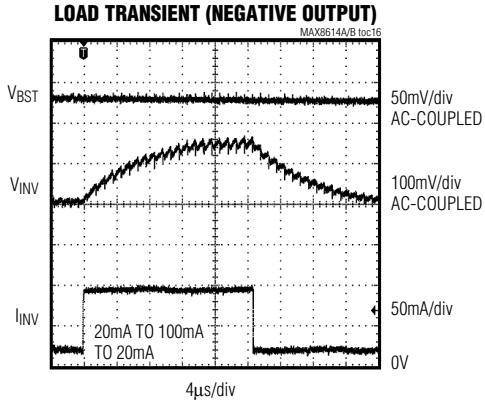
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = V_{AVCC} = 3.6V, SEQ = GND, Figure 1, unless otherwise noted.)

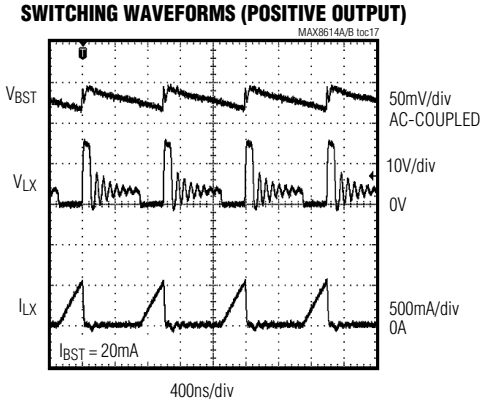
LOAD TRANSIENT (POSITIVE OUTPUT)



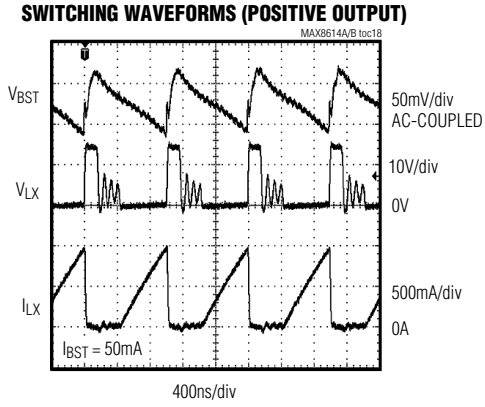
LOAD TRANSIENT (NEGATIVE OUTPUT)



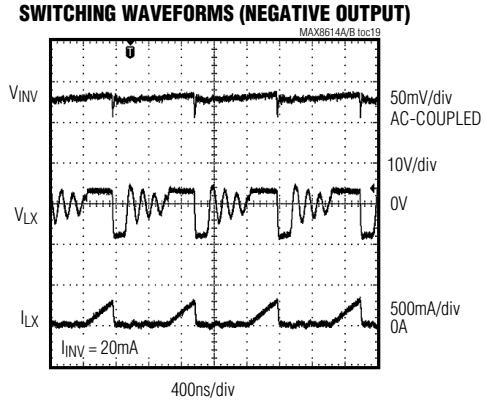
SWITCHING WAVEFORMS (POSITIVE OUTPUT)



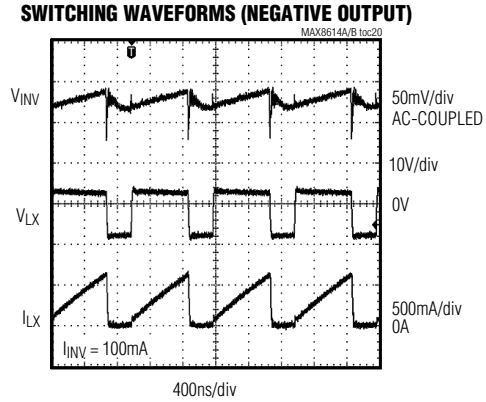
SWITCHING WAVEFORMS (POSITIVE OUTPUT)



SWITCHING WAVEFORMS (NEGATIVE OUTPUT)



SWITCHING WAVEFORMS (NEGATIVE OUTPUT)

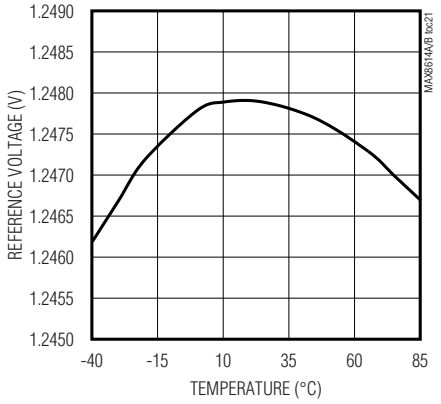


Dual-Output (+ and -) DC-DC Converters for CCD

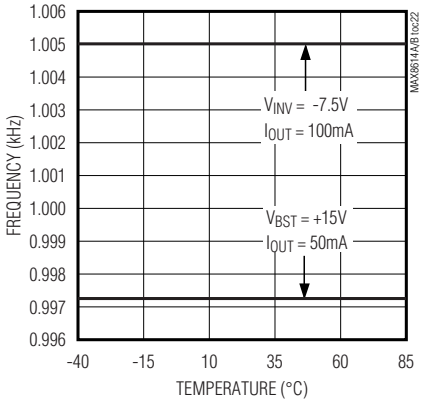
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = V_{AVCC} = 3.6V, SEQ = GND, Figure 1, unless otherwise noted.)

REFERENCE VOLTAGE vs. TEMPERATURE



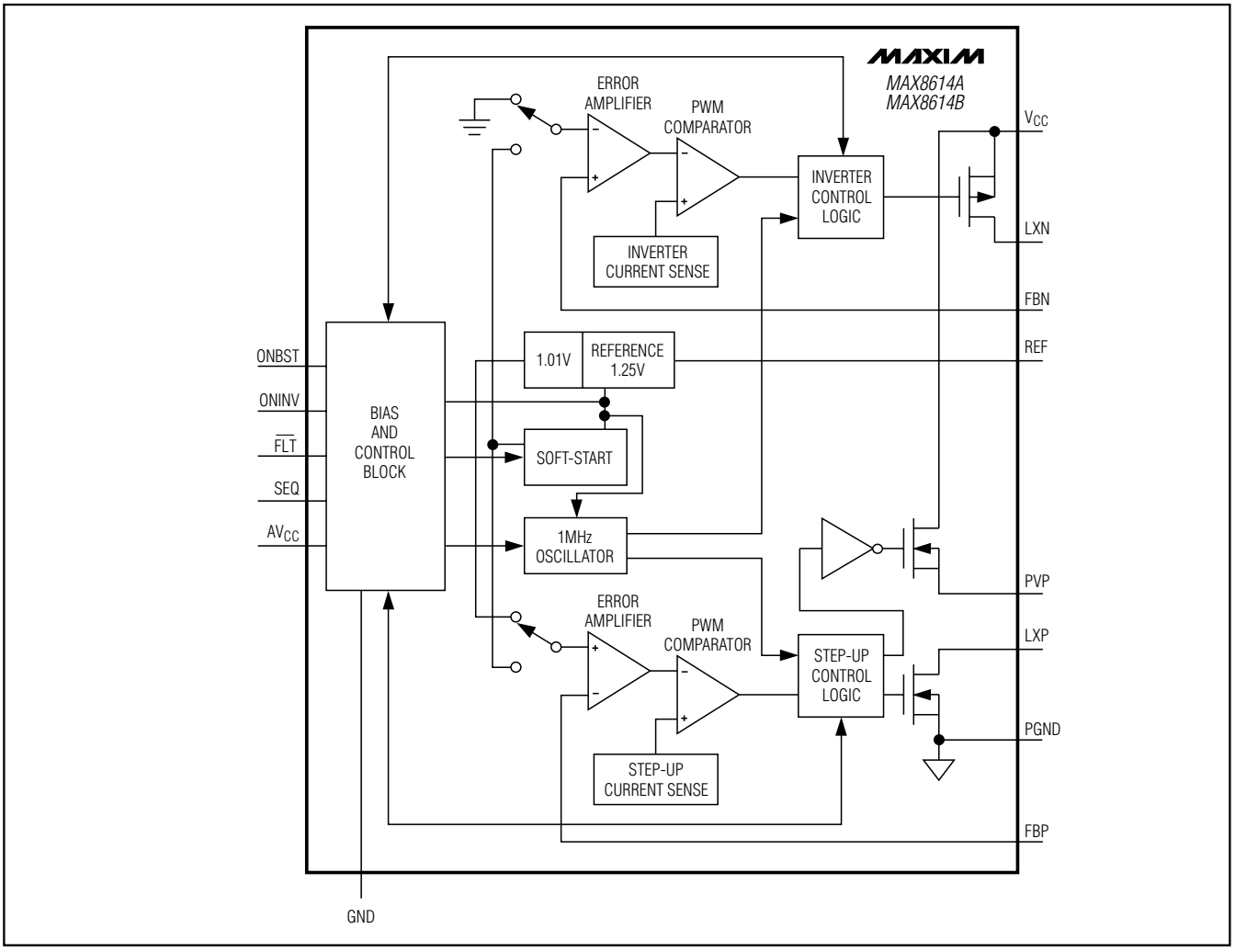
SWITCHING FREQUENCY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	ONBST	Enable Logic Input. Connect ONBST to AV_{CC} for automatic startup of the step-up converter, or use ONBST as an independent control of the step-up converter.
2	FBN	Negative Output Feedback Input. Connect a resistor-divider between the negative output and REF with the center to FBN to set the negative output voltage.
3	AV_{CC}	Bias Supply. AV_{CC} powers the IC. **AV_{CC} must be connected to V_{CC}.**
4	REF	1.25V Reference Voltage Output. Bypass with a 0.22µF ceramic capacitor to GND.
5	GND	Ground. Connect GND to PGND with a short trace.
6	$\overline{FLT}$	Fault Open-Drain Output. Connect a 100kΩ resistor from $\overline{FLT}$ to AV_{CC}. $\overline{FLT}$ is active low during a fault event and is high impedance in shutdown.
7	FBP	Positive Output-Voltage Feedback Input. Connect a resistor-divider between the positive output and GND with the center to FBP to set the positive output voltage. FBP is high impedance in shutdown.
8	SEQ	Sequence Logic Input. When SEQ = low, power-on sequence can be independently controlled by ONBST and ONINV. When SEQ = high, the positive output powers up before the negative output.
9	ONINV	Enable Logic Input. Connect ONINV to AV_{CC} for automatic startup of the inverter, or use ONINV as an independent control of the inverter.
10	LXP	Positive Output Switching Inductor Node. LXP is high impedance in shutdown.
11	PGND	Power Ground. Connect PGND to GND with a short trace.
12	PVP	True-Shutdown Load Disconnect Switch. Connect one side of the inductor to PVP and the other side to LXP. PVP is high impedance in shutdown.
13	V_{CC}	Power Input Supply. V_{CC} supplies power for the step-up and inverting DC-DC converters. **V_{CC} must be connected to AV_{CC}.**
14	LXN	Negative Output Switching Inductor Node. LXN is high impedance in shutdown.
—	EP	Exposed Pad. Connect exposed paddle to ground.

Functional Diagram



Detailed Description

The MAX8614A/MAX8614B generate both a positive and negative output voltage by combining a step-up and an inverting DC-DC converter on one IC. Both the step-up converter and the inverter share a common clock. Each output is independently regulated.

Each output is separately controlled by a pulse-width-modulated (PWM) current-mode regulator. This allows the converters to operate at a fixed frequency (1MHz) for use in noise-sensitive applications. The 1MHz switching rate allows for small external components. Both converters are internally compensated and are optimized for fast transient response (see the *Load-Transient Response/Voltage Positioning* section).

Step-Up Converter

The step-up converter generates a positive output voltage up to 24V. An internal power switch, internal True-Shutdown load switch (PVP), and external catch diode allow conversion efficiencies as high as 90%. The internal load switch disconnects the battery from the load by opening the battery connection to the inductor, providing True Shutdown. The internal load switch stays on at all times during normal operation. The load switch is used in the control scheme for the converter and cannot be bypassed.

Dual-Output (+ and -) DC-DC Converters for CCD

Inverter

The inverter generates output voltages down to -16V below V_{CC}. An internal power switch and external catch diode allow conversion efficiencies as high as 85%.

Control Scheme

Both converters use a fixed-frequency, PWM current-mode control-scheme. The heart of the current-mode PWM controllers is a comparator that compares the error-amp voltage-feedback signal against the sum of the amplified current-sense signal and a slope-compensation ramp. At the beginning of each clock cycle, the internal power switch turns on until the PWM comparator trips. During this time the current in the inductor ramps up, storing energy in the inductor's magnetic field. When the power switch turns off, the inductor releases the stored energy while the current ramps down, providing current to the output.

Fault Protection

The MAX8614A/MAX8614B have robust fault and overload protection. After power-up the device is set to detect an out-of-regulation state that could be caused by an overload or short condition at either output. If either output remains in overload for more than 100ms, both converters turn off and the $\overline{FLT}$ flag asserts low. During a short-circuit condition longer than 100ms on the positive output, foldback current limit protects the output. During a short-circuit condition longer than 100ms on the negative output, both converters turn off and the $\overline{FLT}$ flag asserts low. The converters then remain off until the device is reinitialized by resetting the controller.

The MAX8614A/MAX8614B also have thermal shutdown. When the device temperature reaches +170°C (typ) the device shuts down. When it cools down by 20°C (typ), the converters turn on.

Enable (ONBST/ONINV)

Applying a high logic-level signal to ONBST/ONINV turns on the converters using the soft-start and power-on sequencing described below. Pulling ONBST/ONINV low puts the IC in shutdown mode, turning off the internal circuitry. When ONBST/ONINV goes high (or if power is applied with ONBST/ONINV high), the power-on sequence is set by SEQ. In shutdown, the device consumes only 0.1µA and both output loads are disconnected from the input supply.

Soft-Start and Inrush Current

The step-up converter and inverter in the MAX8614A/MAX8614B feature soft-start to limit inrush current and minimize battery loading at startup. This is accomplished by ramping the reference voltage at the input of each error amplifier. The step-up reference is ramped from 0 to 1V (where 1V is the desired feedback voltage for the step-up converter) while the inverter reference is ramped down from 1.25V to 0 (where 0 is the desired feedback voltage for the inverter).

During startup, the step-up converter True-Shutdown load switch turns on before the step-up-converter reference voltage is ramped up. This effectively limits inrush current peaks to below 500mA during startup.

Undervoltage Lockout (UVLO)

The MAX8614A/MAX8614B feature undervoltage-lockout (UVLO) circuitry, which prevents circuit operation and MOSFET switching when AV_{CC} is less than the UVLO threshold (2.55V, typ). The UVLO comparator has 25mV of hysteresis to eliminate chatter due to the source supply output impedance.

Power-On Sequencing (SEQ)

The MAX8614A/MAX8614B have pin-selectable internally programmed power-on sequencing. This sequencing covers all typical sequencing options required by CCD imagers.

When SEQ = 0, power-on sequence can be independently controlled by ONINV and ONBST. When SEQ = 0 and ONINV and ONBST are pulled high, both outputs reach regulation simultaneously. The inverter is held off while the step-up True-Shutdown switch slowly turns on to pull PVP to V_{CC}. The positive output rises to a diode drop below V_{CC}. Once the step-up output reaches this voltage, the step-up and the inverter then ramp their respective references over a period of 7ms. This brings the two outputs into regulation at approximately the same time.

When SEQ = 1 and ONBST and ONINV are pulled high, the step-up output powers on first. The inverter is held off until the step-up completes its entire soft-start cycle and the positive output is in regulation. Then the inverter starts its soft-start cycle and achieves regulation in about 7ms.

True Shutdown

The MAX8614A/MAX8614B completely disconnect the loads from the input when in shutdown mode. In most step-up converters the external rectifying diode and inductor form a DC current path from the battery to the output. This can drain the battery even in shutdown if a load is connected at the step-up converter output. The MAX8614A/MAX8614B have an internal switch between the input V_{CC} and the inductor node, PVP. When this switch turns off in shutdown there is no DC path from the input to the output of the step-up converter. This load disconnect is referred to as "True Shutdown." At

the inverter output, load disconnect is implemented by turning off the inverter's internal power switch.

Current-Limit Select

The MAX8614B allows an inductor current limit of 0.8A on the step-up converter and 0.75A on the inverter. The MAX8614A allows an inductor current limit of 0.44A on the step-up converter and 0.33A on the inverter. This allows flexibility in designing for higher load-current applications or for smaller, more compact designs when less power is needed. Note that the currents listed above are peak inductor currents and not output currents. The MAX8614B output current is 50mA at +15V and 100mA at -7.5V. The MAX8614A output current is 25mA at +15V and 50mA at -7.5V.

Load Transient/Voltage Positioning

The MAX8614A/MAX8614B match the load regulation to the voltage droop seen during load transients. This is sometimes called voltage positioning. This results in minimal overshoot when a load is removed and minimal voltage drop during a transition from light load to full load.

The use of voltage positioning allows superior load-transient response by minimizing the amplitude of overshoot and undershoot in response to load transients. DC-DC converters with high control-loop gains maintain tight DC load regulation but still allow large voltage drops of 5% or greater for several hundred microseconds during transients. Load-transient variations are seen only with an oscilloscope (see the *Typical Operating Characteristics*). Since DC load regulation is read with a voltmeter, it does not show how the power supply reacts to load transients.

Applications Information

Adjustable Output Voltage

The positive output voltage is set by connecting FBP to a resistive voltage-divider between the output and GND (Figure 1). Select feedback resistor R2 in the 30kΩ to 100kΩ range. R1 is then given by:

$$R1 = R2 \left(\frac{V_{BST}}{V_{FBP}} - 1 \right)$$

where V_{FBP} = 1.01V.

The negative output voltage is set by connecting FBN to a resistive voltage-divider between the output and REF (Figure 1). Select feedback resistor R4 in the 30kΩ to 100kΩ range. R3 is then given by:

$$R3 = R4 \times \left(\frac{V_{FBN} - V_{IMV}}{V_{REF} - V_{FBN}} \right)$$

where V_{REF} = 1.25V and V_{FBN} = 0V.

Inductor Selection

The MAX8614A/MAX8614B high switching frequency allows for the use of a small inductor. The 4.7µH and 2.2µH inductors shown in the *Typical Operating Circuit* is recommended for most applications. Larger inductances reduce the peak inductor current, but may result in skipping pulses at light loads. Smaller inductances require less board space, but may cause greater peak current due to current-sense comparator propagation delay.

Use inductors with a ferrite core or equivalent. Powder iron cores are not recommended for use with high switching frequencies. The inductor's incremental saturation rating must exceed the selected current limit. For highest efficiency, use inductors with a low DC resistance (under 200mΩ); however, for smallest circuit size, higher resistance is acceptable. See Table 1 for a representative list of inductors and Table 2 for component suppliers.

Diode Selection

The MAX8614A/MAX8614B high switching frequency demands a high-speed rectifier. Schottky diodes, such as the CMHSH5-2L or MBR0530L, are recommended. Make sure that the diode's peak current rating exceeds the selected current limit, and that its breakdown voltage exceeds the output voltage. Schottky diodes are preferred due to their low forward voltage. However, ultrahigh-speed silicon rectifiers are also acceptable. Table 2 lists component suppliers.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. These requirements can be balanced by appropriate selection of the current limit.

For stability, the positive output filter capacitor, C1, should satisfy the following:

$$C1 > (6L\ I_{BSTMAX}) / (R_{CS}\ D+\ V_{BST}^2)$$

where R_{CS} = 0.015 (MAX8614B), and 0.035 (MAX8614A). D+ is 1 minus the step-up switch duty cycle and is:

$$D+ = V_{CC} / V_{BST}$$

Dual-Output (+ and -) DC-DC Converters for CCD

Table 1. Inductor Selection Guide

OUTPUT VOLTAGES AND LOAD CURRENT	INDUCTOR	L (µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (mm)
15V, 50mA -7.5V, 100mA	TOKO DB3018C, 1069AS-2R0	2.0	72	1.4	3 x 3 x 1.8
	TOKO DB3018C, 1069AS-4R3	4.3	126	0.97	3 x 3 x 1.8
	TOKO S1024AS-4R3M	4.3	47	1.2	4 x 4 x 1.7
	Sumida CDRH2D14-4R7	4.7	170	1	3.2 x 3.2 x 1.55
	TOKO S1024AS-100M	10	100	0.8	4 x 4 x 1.7
15V, 20mA -7.5V, 40mA	Sumida CDRH2D11-100	10	400	0.35	3.2 x 3.2 x 1.2
	Sumida CDRH2D14-100	10	295	0.46	3.2 x 3.2 x 1.55
	Murata LQH32CN100K33	10	300	0.45	3.2 x 2.5 x 2

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
INDUCTORS		
Murata	770-436-1300	www.murata.com
Sumida	847-545-600	www.sumida.com
TOKO	847-297-0070	www.tokoam.com
DIODES		
Central Semiconductor (CMHSH5-2L)	631-435-1110	www.centralsemi.com
Motorola (MBR0540L)	602-303-5454	www.motorola.com
CAPACITORS		
Taiyo Yuden	408-573-4150	www.t-yuden.com
TDK	888-835-6646	www.TDK.com

For stability, the inverter output filter capacitor, C2, should satisfy the following:

$$C2 > (6L\ V_{REF}\ I_{INVMAX}) / (R_{CS}\ D- (V_{REF} - V_{INV})\ V_{INV})$$

where R_{CS} = 0.0175 (MAX8614B), and 0.040 (MAX8614A). D- is 1 minus the inverter switch duty cycle and is:

$$D- = V_{CC} / V_{INV}$$

Table 2 lists representative low-ESR capacitor suppliers.

Input Bypass Capacitor

Although the output current of many MAX8614A/MAX8614B applications may be relatively small, the input must be designed to withstand current transients equal to the inductor current limit. The input bypass capacitor reduces the peak currents drawn from the voltage source, and reduces noise caused by the MAX8614A/MAX8614B switching action. The input source impedance determines the size of the capacitor required at the input. As with the output filter capacitor, a low-ESR capacitor is recommended. A 22µF, low-ESR capacitor is adequate for most applications, although smaller bypass capacitors may also be acceptable with low-impedance sources or if the source supply is already well filtered. Bypass AV_{CC} separately from V_{CC} with a 1.0µF ceramic capacitor placed as close as possible to the AV_{CC} and GND pins.

PCB Layout and Routing

Proper PCB layout is essential due to high-current levels and fast-switching waveforms that radiate noise. Breadboards or protoboards should never be used when prototyping switching regulators.

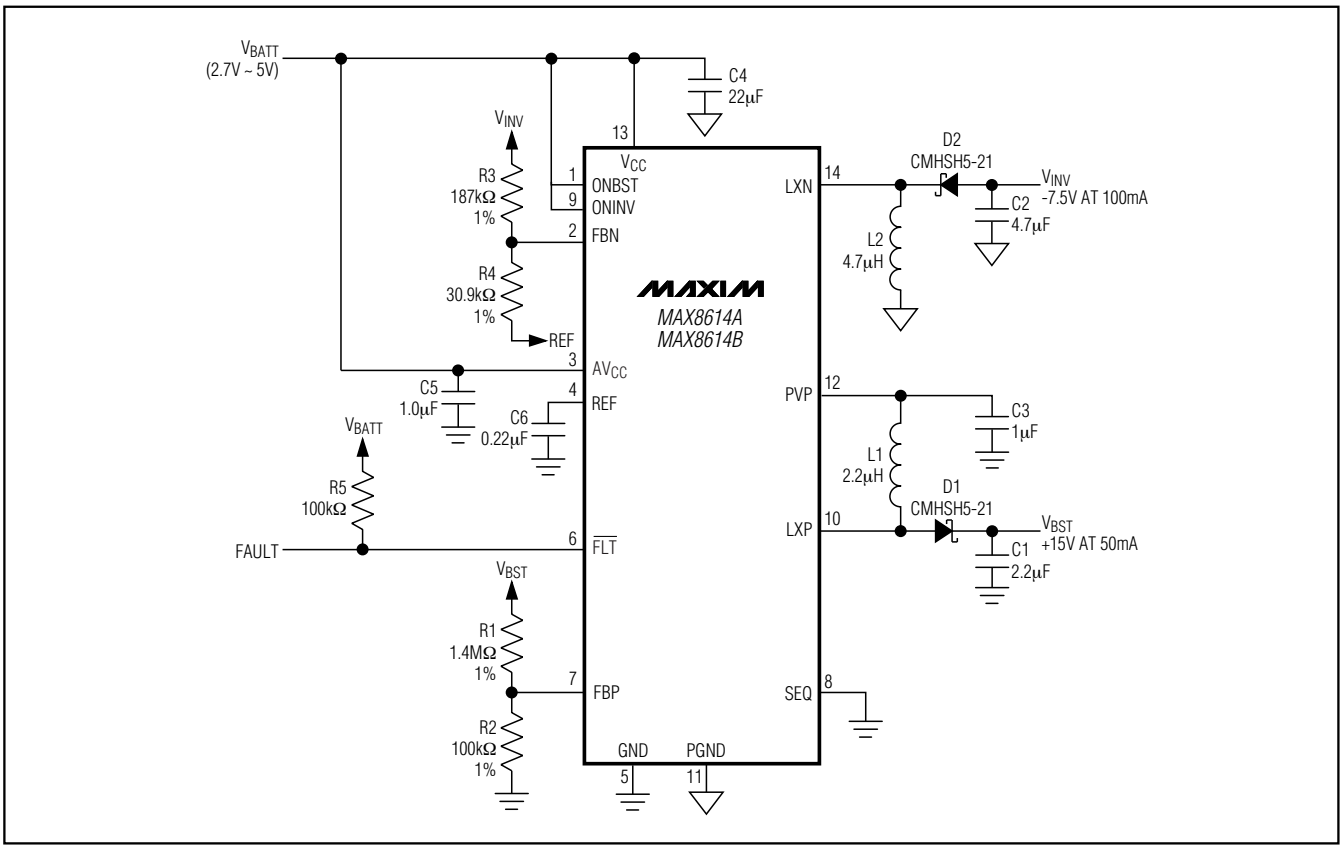


Figure 1. Typical Application Circuit

It is important to connect the GND pin, the input bypass-capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration) to minimize ground noise and improve regulation. Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise, with preference given to the feedback circuit, the ground circuit, and LX_. Place feedback resistors R1–R4 as close to their respective feedback pins as possible. Place the input bypass capacitor as close as possible to AV_{CC} and GND.

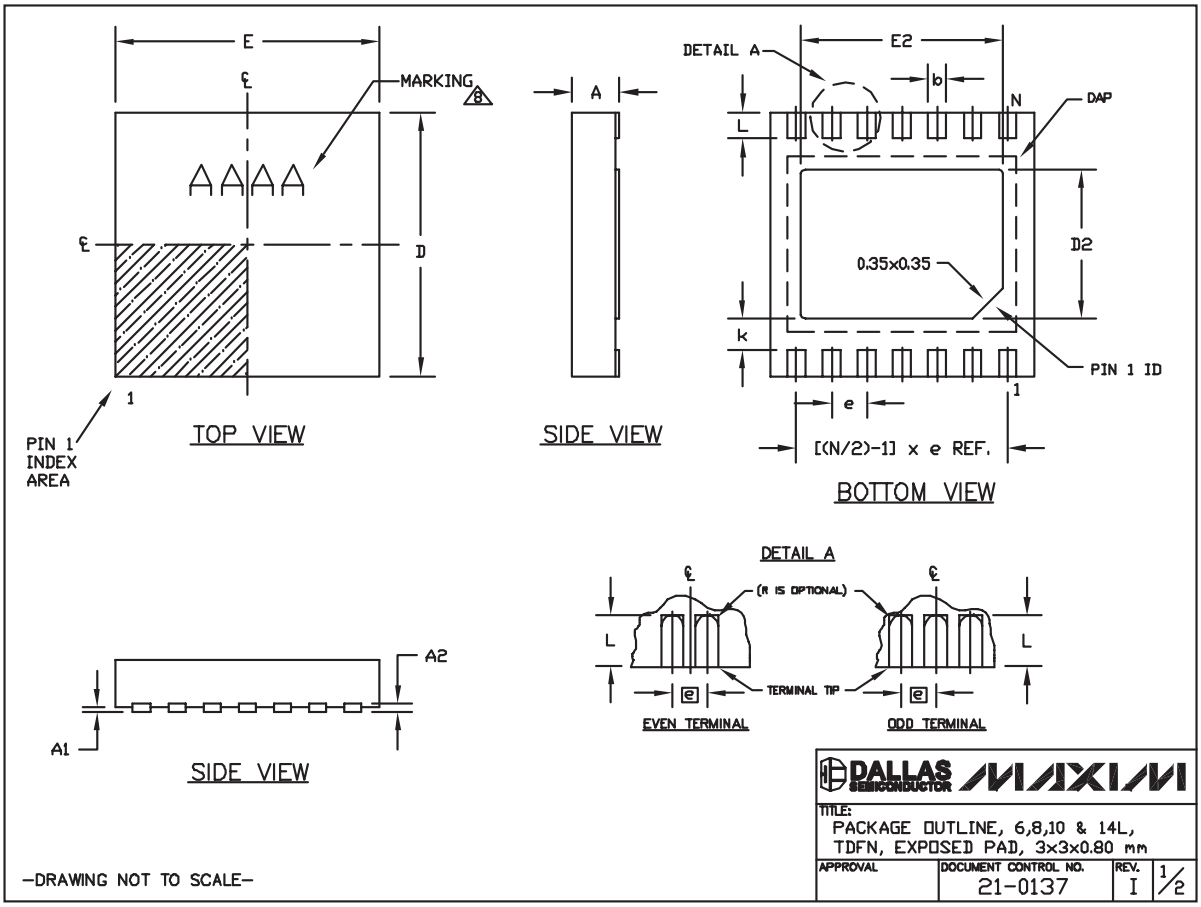
Chip Information

PROCESS: BiCMOS

Dual-Output (+ and -) DC-DC Converters for CCD

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-2	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-3	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1033-2	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1433-1	14	1.70–0.10	2.30–0.10	0.40 BSC	- - - -	0.20–0.05	2.40 REF
T1433-2	14	1.70–0.10	2.30–0.10	0.40 BSC	- - - -	0.20–0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

-DRAWING NOT TO SCALE-

Revision History

Pages changed at Rev 1: 1, 12, 14, 15