Triple 2-channel analog multiplexer/demultiplexer 74LV4053

FEATURES

- Optimized for low voltage applications: 1.0 to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low typ "ON" resistance:
  100 Ω at $V_{cc} - V_{EE}$ = 4.5 V
  150 Ω at $V_{cc} - V_{EE}$ = 3.0 V
  240 Ω at $V_{cc} - V_{EE}$ = 2.0 V
- Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4053 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4053.

The 74LV4053 is a triple 2-channel analog multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY_0 to nY_1), a common input/output (nZ) and three digital select inputs (S_1 to S_3).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_1 to S_3 With $\overline{E}$ HIGH, all switches are in the high impedance OFF-states, independent of S_1 and S_3.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_1, to S_3, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (nY_0, to nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} S_n to V_{OS}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	 16 20	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} S_n to V_{OS}		 17 16	
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	See Notes 1 and 2	36	
C_S	Maximum switch capacitance independent (Y) common (Z)		5 8	

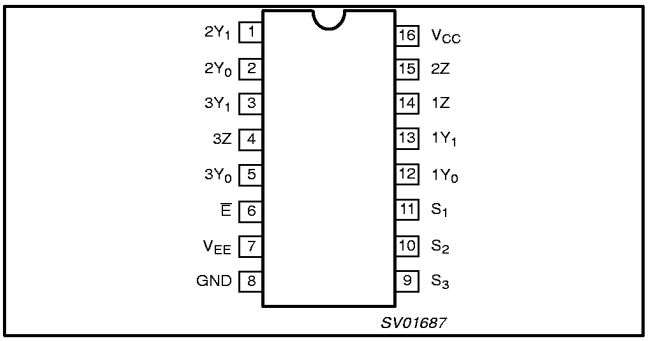
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4053 N	74LV4053 N	SOT38-1
16-Pin Plastic SO	–40°C to +125°C	74LV4053 D	74LV4053 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4053 DB	74LV4053 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4053 PW	74LV4053PW DH	SOT403-1

PIN CONFIGURATION

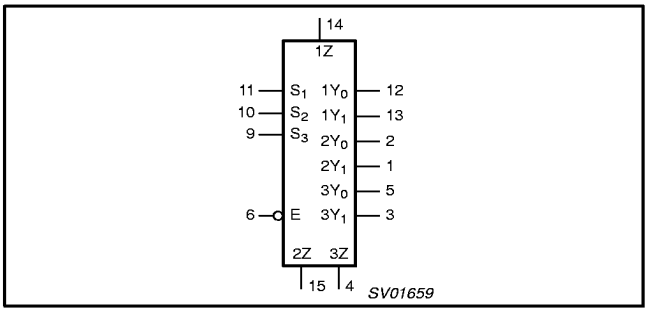


PIN DESCRIPTION

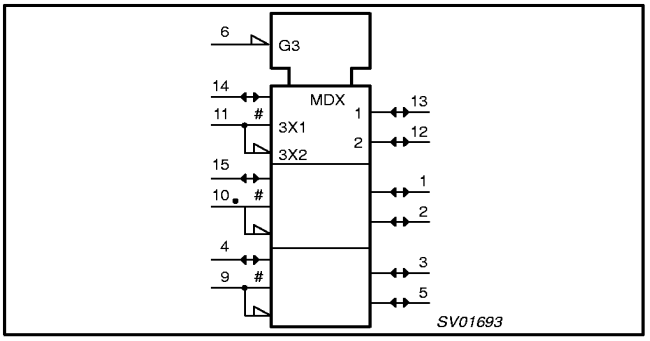
PIN NUMBER	SYMBOL	FUNCTION
2, 1	$2Y_0$, $2Y_1$	Independent inputs/outputs
5, 3	$3Y_0$, $3Y_1$	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0 V)
11, 10, 9	S_1 to S_3	Select inputs
12, 13	$1Y_0$, $1Y_1$	Independent inputs/outputs
14, 15, 4	1Z to 3Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

Triple 2-channel analog multiplexer/demultiplexer 74LV4053

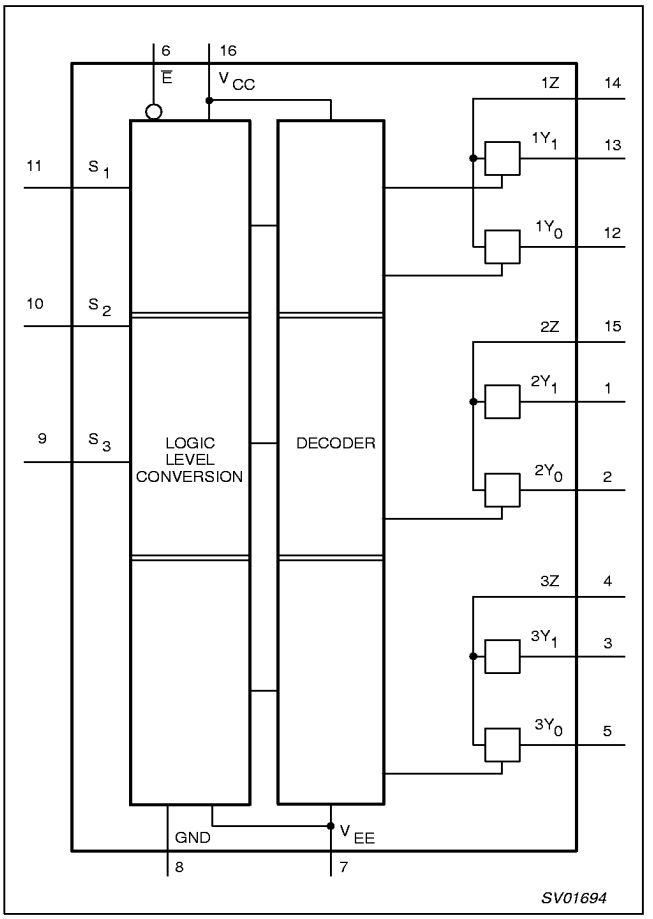
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM

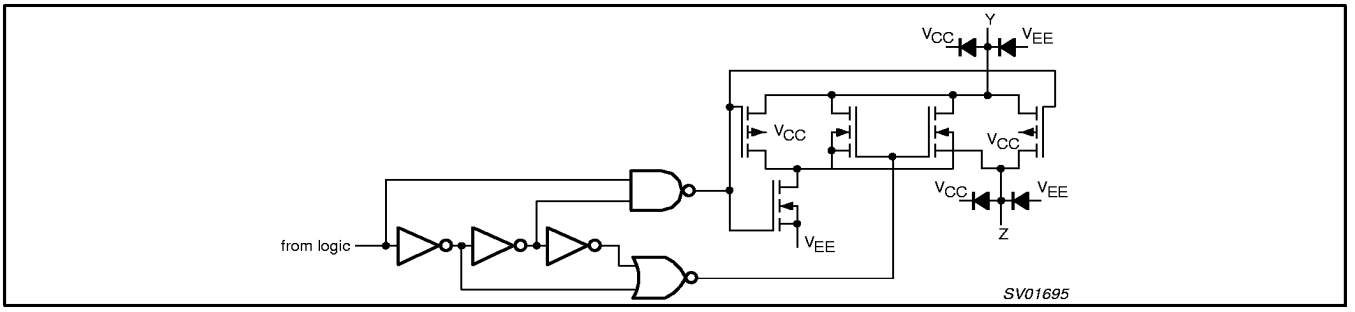


FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	Sn	
L	L	$nY_0 - nZ$
L	H	$nY_1 - nZ$
H	X	None

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

SCHEMATIC DIAGRAM (ONE SWITCH)



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{SK}$	DC switch diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V	20	mA
$\pm I_S$	DC switch current	-0.5 V $< V_S < V_{CC} + 0.5$ V	25	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1 and Figure 5	1.0	3.3	6.0	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 6.0V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V		0.9			0.9		V
		V_{CC} = 2.0 V		1.4			1.4		
		V_{CC} = 2.7 to 3.6 V		2.0			2.0		
		V_{CC} = 4.5 V		3.15			3.15		
		V_{CC} = 6.0 V		4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V				0.3		0.3	V
		V_{CC} = 2.0 V				0.6		0.6	
		V_{CC} = 2.7 to 3.6 V				0.8		0.8	
		V_{CC} = 4.5 V				1.35		1.35	
		V_{CC} = 6.0 V				1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6	V_I = V_{CC} or GND			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\|V_S\|$ = V_{CC} - GND (See Figure 2)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch ON-state current	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\|V_S\|$ = V_{CC} - GND (See Figure 3)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V	V_I = V_{CC} or GND; V_{IS} = GND or V_{CC}; V_{OS} = V_{CC} or GND			20.0		40	µA
		V_{CC} = 6.0 V				40.0		80	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 to 3.6 V	V_I = V_{CC} – 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V	I_S = 100 µA; V_{IS} = V_{CC} to GND; V_I = V_{IH} or V_{IL}						Ω
		V_{CC} = 2.0 V	I_S = 1000 µA; V_{IS} = V_{CC} to GND; V_I = V_{IH} or V_{IL}		180	365		435	
		V_{CC} = 2.7 V			115	225		270	
		V_{CC} = 3.0 to 3.6 V			100	200		245	
		V_{CC} = 4.5 V			75	150		180	
		V_{CC} = 6.0 V			70	140		165	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	I_S = 100 µA; V_{IS} = GND; V_I = V_{IH} or V_{IL}		250				Ω
		V_{CC} = 2.0 V	I_S = 1000 µA; V_{IS} = GND; V_I = V_{IH} or V_{IL}		120	280		325	
		V_{CC} = 2.7 V			75	170		195	
		V_{CC} = 3.0 to 3.6 V			70	155		180	
		V_{CC} = 4.5 V			50	120		135	
		V_{CC} = 6.0 V			45	105		120	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = V_{CC}		350				Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = V_{CC}		170	340		400	
		V_{CC} = 2.7 V			105	210		250	
		V_{CC} = 3.0 to 3.6 V			95	190		225	
		V_{CC} = 4.5 V			70	140		165	
		V_{CC} = 6.0 V			65	125		150	

DC ELECTRICAL CHARACTERISTICS (*Continued*)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; V_{IS} = V_{CC} to GND						Ω
		V_{CC} = 2.0 V			5				
		V_{CC} = 2.7 V			4				
		V_{CC} = 3.0 to 3.6 V			4				
		V_{CC} = 4.5 V			3				
		V_{CC} = 6.0 V			2				

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

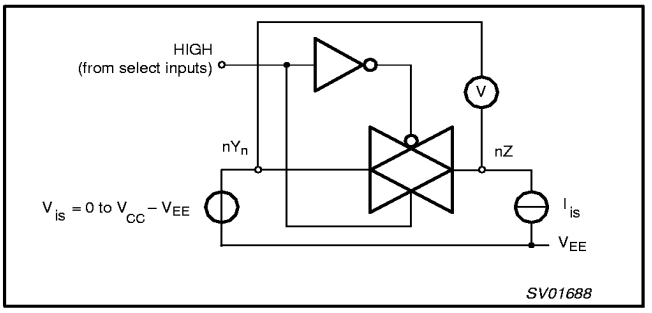


Figure 1. Test circuit for measuring ON-resistance (R_{ON}).

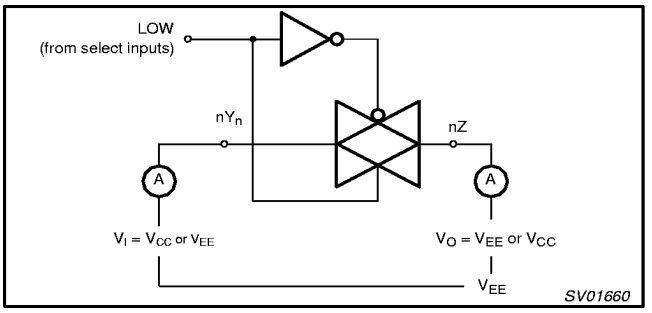


Figure 2. Test circuit for measuring OFF-state current.

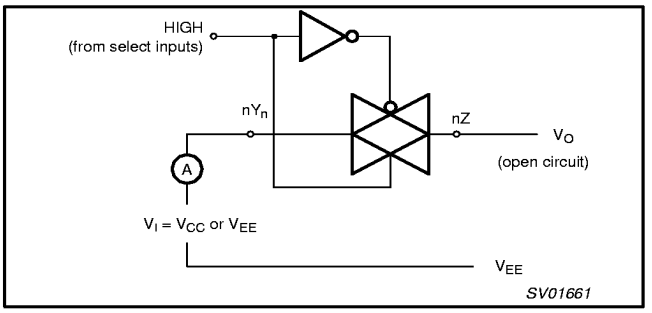


Figure 3. Test circuit for measuring ON-state current.

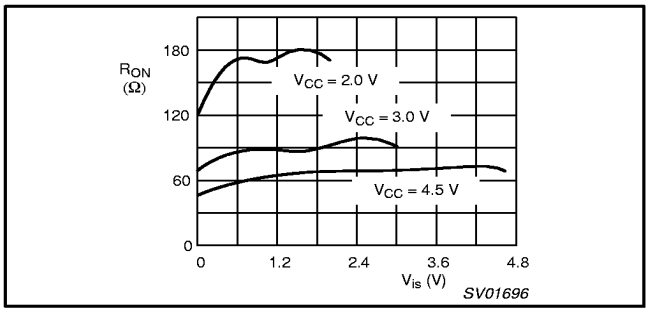


Figure 4. Typical ON-resistance (R_{on}) as a function of input voltage (V_{is}) for V_{is} = 0 to $V_{CC} - V_{EE}$.

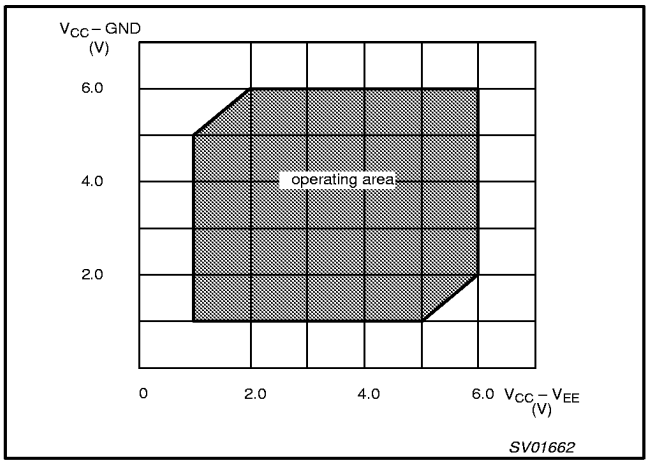


Figure 5. Guaranteed operating area as a function of the supply voltages.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	CONDITION		LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
		V_{CC} (V)	OTHER	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os}	1.2	$R_L = \infty$; $C_L = 50$ pF Figure 12		25				ns
		2.0			9	17		20	
		2.7			6	13		15	
		3.0 to 3.6			5[2]	10		12	
		4.5			4	9		10	
		6.0			3	7		8	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$ to V_{os}	1.2	$R_L = 1$kΩ; $C_L = 50$ pF Figures 13 and 1		100				ns
		2.0			34	65		77	
		2.7			25	48		56	
		3.0 to 3.6			19[2]	38		45	
		4.5			17	32		38	
		6.0			13	25		29	
t_{PZH}/t_{PZL}	Turn-on time S_n to V_{os}	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 13 and 1		125				ns
		2.0			43	82		97	
		2.7			31	60		71	
		3.0 to 3.6			24[2]	48		57	
		4.5			21	41		48	
		6.0			16	31		37	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$ to V_{os}	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 13 and 1		95				ns
		2.0			34	61		73	
		2.7			26	46		54	
		3.0 to 3.6			20[2]	37		44	
		4.5			18	32		38	
		6.0			15	25		30	
t_{PHZ}/t_{PLZ}	Turn-off time Sn to V_{os}	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 13 and 1		90				ns
		2.0			32	59		70	
		2.7			24	44		52	
		3.0 to 3.6			19[2]	36		42	
		4.5			17	31		36	
		6.0			14	24		28	

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values
GND = 0 V; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figures 9 and 10
	Sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figures 9 and 10
	Switch "OFF" signal feed through	–50 –50	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figures 5 and 11
	Crosstalk between any two switches/multiplexers	–60 –60	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figure 8
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 120	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pf; f= 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND $t_r = t_f$ = 6 ns) Figure 8
f_{max}	Minimum frequency response (–3 dB)	180 200	MHz	3.0 6.0	Note 2	R_L = 50 Ω; C_L = 50 pF Figures 6, 8 and 9
C_S	Maximum switch capacitance	5	pf			

GENERAL NOTES:

V_{is} is the input voltage at nY_n or nZ terminal, whichever is assigned as an input.
V_{OS} is the output voltage at nY_n or nZ terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

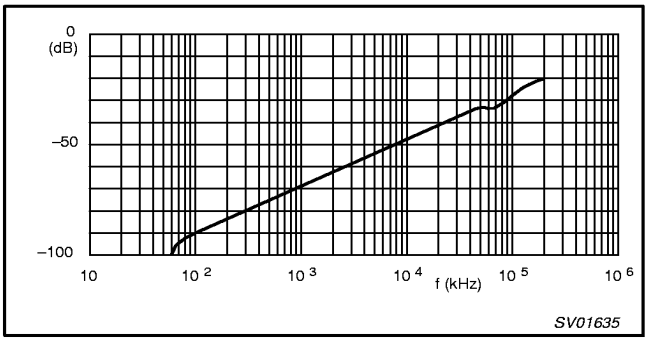


Figure 6. Typical switch "OFF" signal feed-through as a function of frequency.

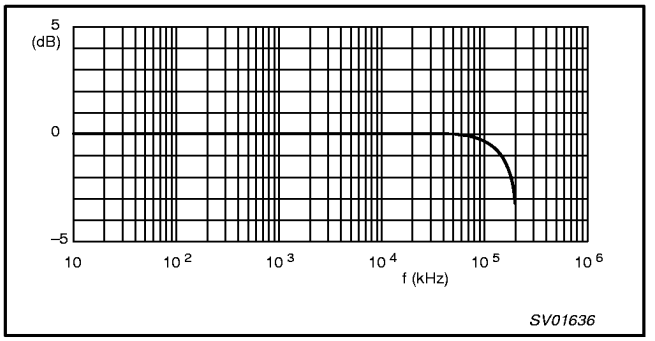


Figure 7. Typical frequency response.

NOTES TO FIGURES 6 AND 7:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = -3.0V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

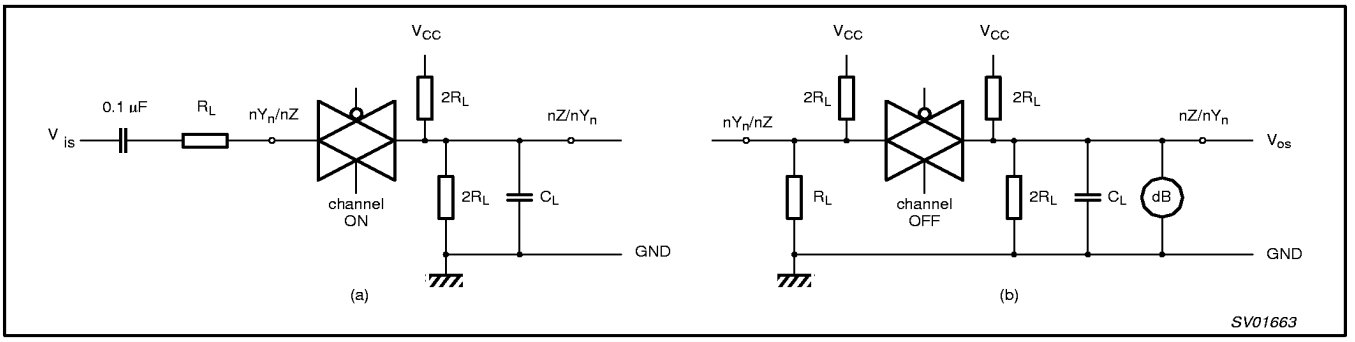
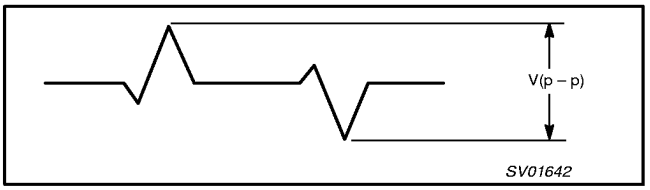


Figure 8. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

NOTE TO FIGURE 8:
The crosstalk is defined as follows (oscilloscope output):



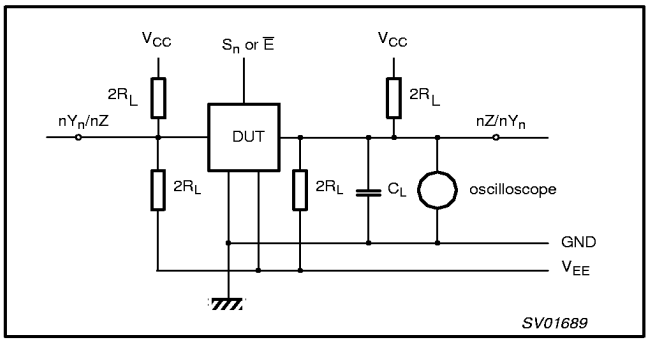


Figure 9. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 9:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

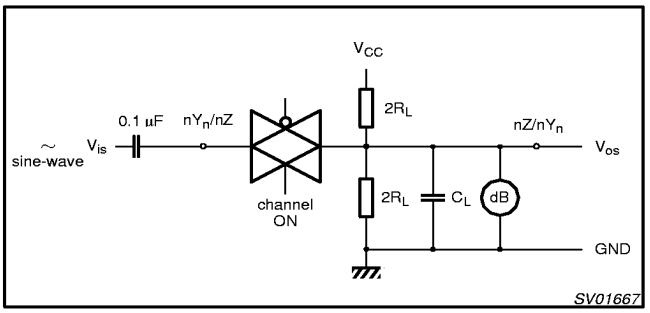


Figure 10. Test circuit for measuring minimum frequency response.

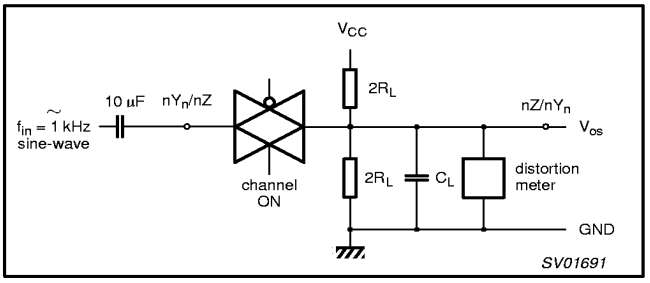


Figure 11. Test circuit for measuring sine-wave distortion.

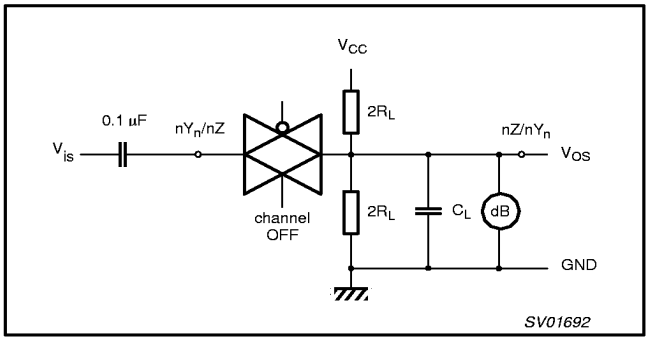


Figure 12. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_M = 0.5 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
V_x = V_{OL} + 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_X = V_{OL} + 0.1 × V_{CC} at 2.7 V >V_{CC} > 3.6 V
V_Y = V_{OH} − 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_Y = V_{OH} − 0.1 × V_{CC} at 2.7 V >V_{CC} > 3.6 V

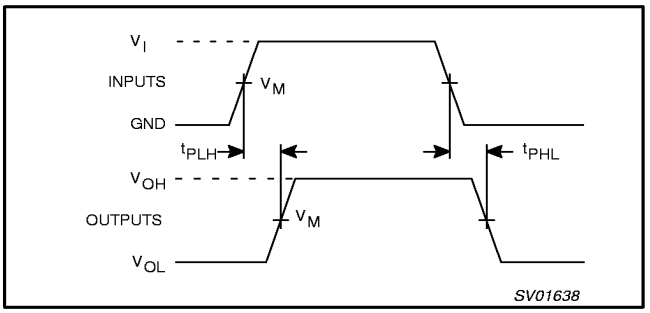


Figure 13. Input (V_{is}) to output (V_{os}) propagation delays.

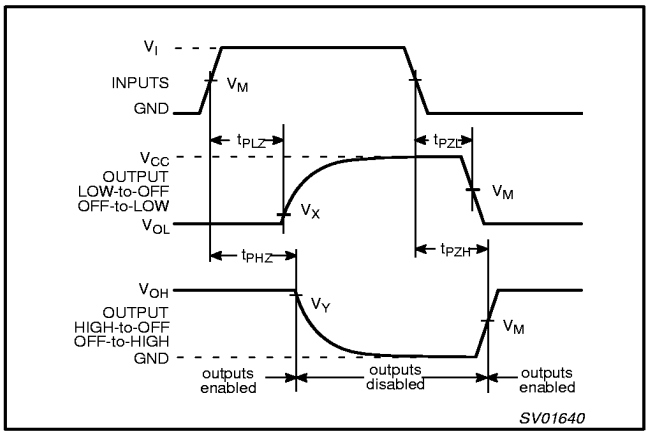
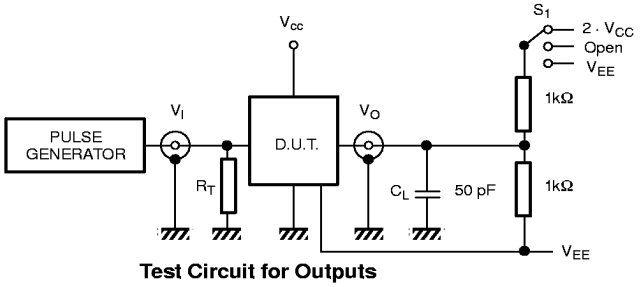
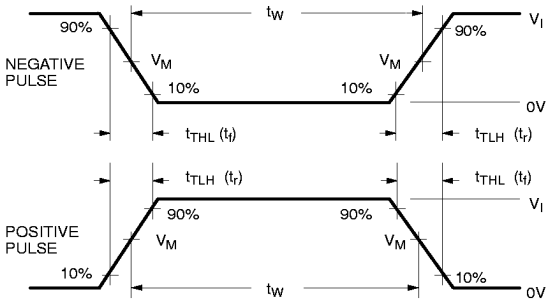


Figure 14. Turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{os}).

TEST CIRCUIT



Test Circuit for Outputs



V_{CC}	V_I
< 2.7V	V_{CC}
2.7 - 3.6V	2.7V
> 3.6 V	V_{CC}

Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	2 · V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_I

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

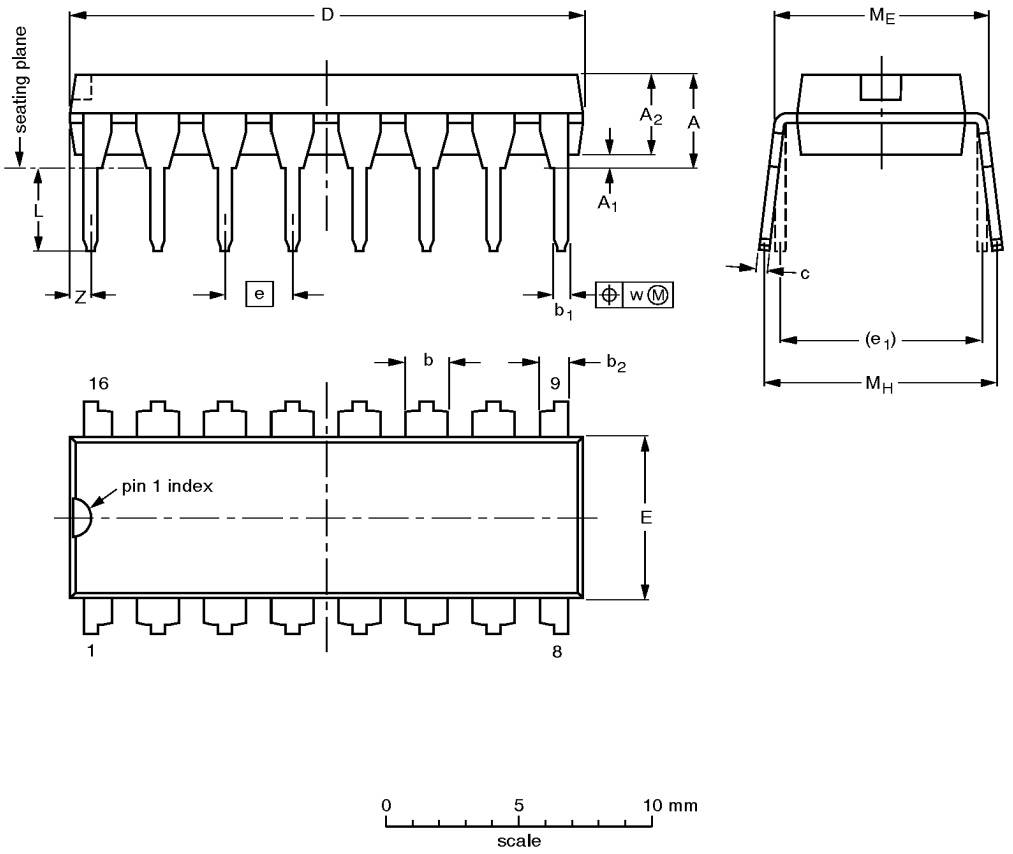
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_r = t_f =6ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

SY01738

Figure 15. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

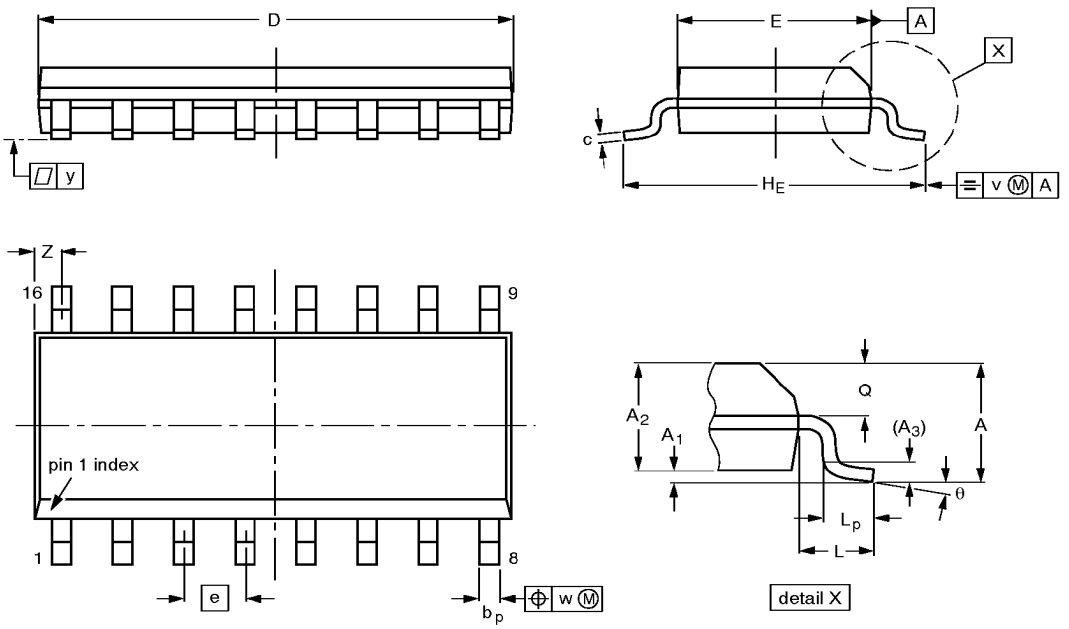
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

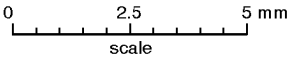
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

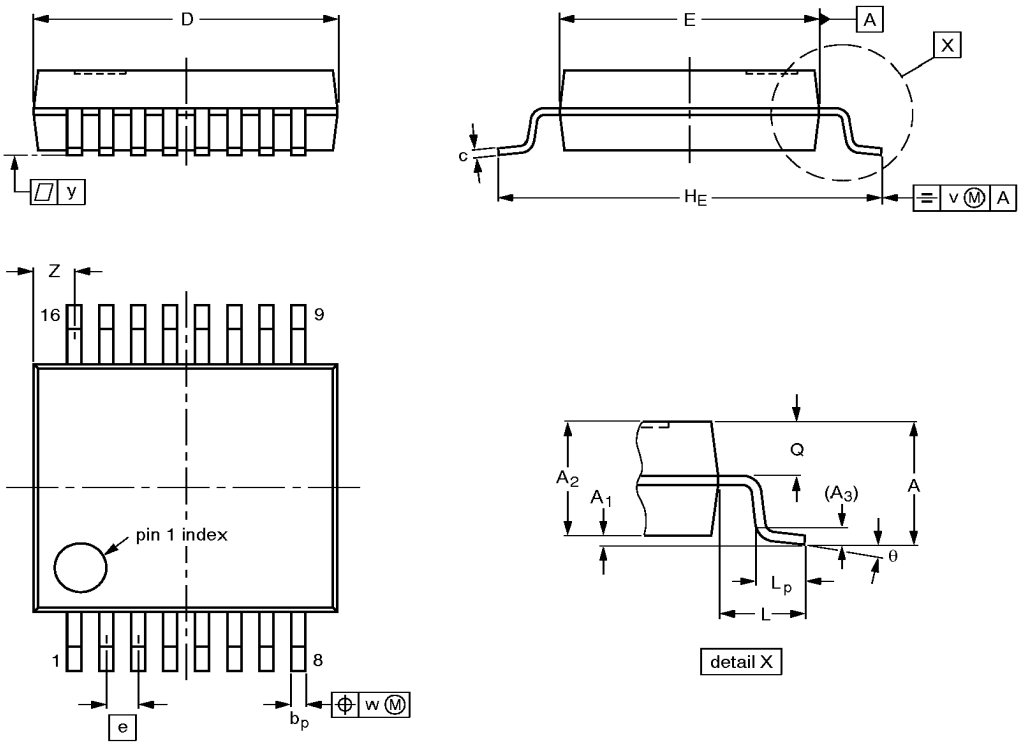
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

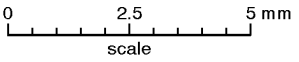
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**





DIMENSIONS (mm are the original dimensions)

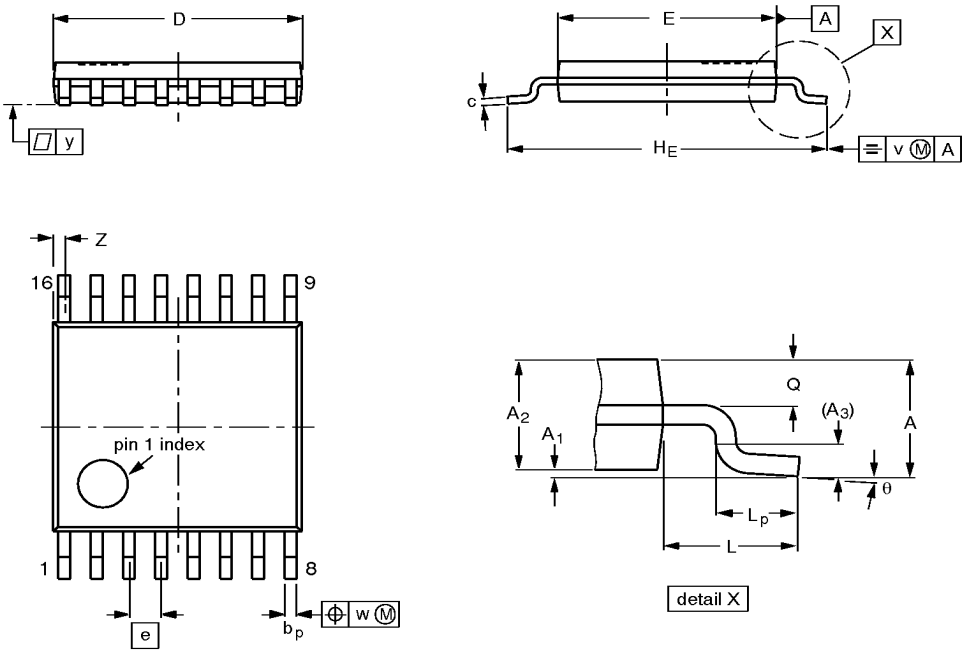
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

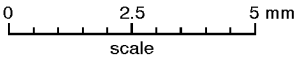
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04