Freescale Semiconductor

Technical Data

查询"MPVZ5004G6U"供应商

Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPVZ5004G series piezoresistive transducers are state-of-the-art monolithic silicon pressure sensors designed for the appliance, consumer, healthcare and industrial market. The analog output can be read directly into the A/D input of Freescale microcontrollers. This transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure. The axial port has been modified to accommodate industrial grade tubing.

Features

- 1.5% Maximum Error for 0 to 100 mm H₂O over +10° to +60°C with Auto Zero
- 2.5% Maximum Error for 100 to 400 mm H_2O over +10° to +60°C with Auto Zero
- 6.25% Maximum Error for 0 to 400 mm H₂O over +10° to +60°C without Auto Zero
- Temperature Compensated over +10° to +60°C
- Available in Surface Mount (SMT) or Through-hole (DIP) Configurations

Application Examples

- Washing Machine Water Level Measurement (Reference AN1950)
- · Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Appliance Liquid Level and Pressure Measurement
- · Respiratory Equipment

ORDERING INFORMATION							
Device Type	Case No.	MPVZ Series Order No.	Packing Options	Device Marking			
Surface Mount	1735-01	MPVZ5004GW6U	Rails	MZ5004GW			
Through-Hole	1560-02	MPVZ5004GW7U	Rails	MZ5004GW			
Surface Mount	482-01	MPVZ5004G6U	Rails	MZ5004G			
Surface Mount	482-01	MPVZ5004G6T1	Tape & Reel	MZ5004G			
Through-Hole	482B-03	MPVZ5004G7U	Rails	MZ5004G			

MPVZ5004G SERIES

INTEGRATED
PRESSURE SENSOR
0 to 3.92 kPA
(0 to 400 mm H₂O)
1.0 to 4.9 V OUTPUT

SMALL OUTLINE PACKAGE SURFACE MOUNT





MPVZ5004GW6U CASE 1735-01

MPVZ5004G6U/T1 CASE 482-01

SMALL OUTLINE PACKAGE THROUGH-HOLE





MPVZ5004GW7U CASE 1560-02

MPVZ5004G7U CASE 482B-03

PIN NUMBERS ⁽¹⁾				
1	N/C	5	N/C	
2	Vs	6	N/C	
3	GND	7	N/C	
4	V _{OUT}	8	N/C	

 Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.



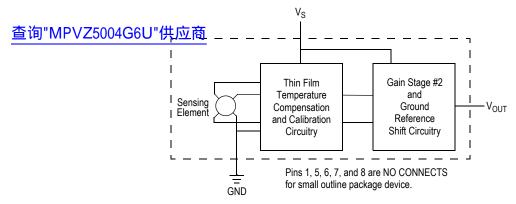


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings⁽¹⁾

Rating	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P _{MAX}	16	kPa
Storage Temperature	T _{STG}	-30 to +100	°C
Operating Temperature	T _A	0 to +85	°C

^{1.} Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Table 2. Operating Characteristics ($V_S = 5.0 V_{DC}$, $T_A = 25^{\circ}C$ unless otherwise noted, P1 > P2)

	Characteristic		Min	Тур	Max	Units
Pressure Range		P _{OP}	0	_	3.92 400	kPa mm H ₂ O
Supply Voltage ⁽¹⁾		V _S	4.75	5.0	5.25	V _{DC}
Supply Current		I _S	_	_	10	mAdc
Full Scale Span ⁽²⁾ @ V _S = 5.0 Volts		V _{FSS}	_	4.0	_	V
Offset ^{(3) (4)}		V _{OFF}	0.75	1.0	1.25	V
Sensitivity		V/P	_	1.0 9.8	_	V/kPa mV/mm H ₂ O
Accuracy ^{(4) (5)}	0 to 100 mm H ₂ O (10 to 60°C)	_	_	_	±1.5	%V _{FSS} with auto zero
	100 to 400 mm H ₂ O (10 to 60°C)	_	_	_	±2.5	%V _{FSS} with auto zero
	0 to 400 mm H ₂ O (10 to 60°C)	1	_	_	±6.25	%V _{FSS} without auto zero

- 1. Device is ratiometric within this specified excitation range.
- 2. Span is defined as the algebraic difference between the output voltage at specified pressure and the output voltage at the minimum rated pressure.
- 3. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
- 4. Accuracy (error budget) consists of the following:
 - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
 - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to
 - and from the minimum or maximum operating temperature points, with zero differential pressure applied.
 - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the
 - minimum or maximum rated pressure, at 25°C.
 - Offset Stability: Output deviation, after 1000 temperature cycles, -30 to 100°C, and 1.5 million pressure cycles, with minimum
 - rated pressure applied.
 - TcSpan: Output deviation over the temperature range of 10 to 60°C, relative to 25°C.
 - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 10 to 60°C, relative to 25°C.
 - $\bullet \ \ \text{Variation from Nominal:} \ \ \text{The variation from nominal values, for Offset or Full Scale Span, as a percent of V_{FSS}, at $25^{\circ}C$.}$
- 5. Auto Zero at Factory Installation: Due to the sensitivity of the MPVZ5004G, external mechanical stresses and mounting position can affect the zero pressure output reading. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. Reference AN1636 for specific information. The specified accuracy assumes a maximum temperature change of ± 5°C between autozero and measurement.

ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the Differential or Gauge configuration in the basic chip carrier (Case 482). A gel die coat isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPVZ5004G series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and

qualification test for dry air, and other media, are available from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the output of the MPVZ5004G to the A/D input of the microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 and Figure 5 shows the sensor output signal relative to pressure input. Typical, minimum and maximum output curves are shown for operation over a temperature range of 10°C to 60°C using the decoupling circuit shown in Figure 3 The output will saturate outside of the specified pressure range.

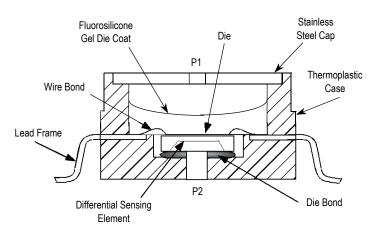


Figure 2. Cross-Sectional Diagram (Not to Scale)

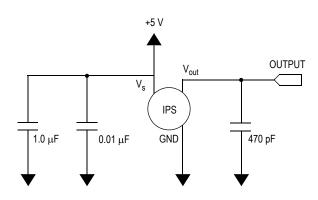


Figure 3. Recommended Power Supply Decoupling and Output Filtering.

(For additional output filtering, please refer to Application Note AN1646.)

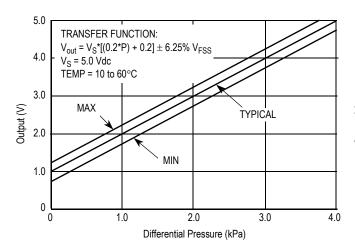


Figure 4. Output versus Pressure Differential at ±6.25% V_{FSS} (without auto zero, note 5 in Operating Characteristics)

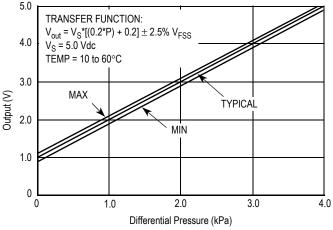


Figure 5. Output versus Pressure Differential at ±2.5% V_{FSS} (with auto zero, note 5 in Operating Characteristics)

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing a gel die coat which isolates the die from the environment. The

Freescale Semiconductor pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below.

Part Number	Case Type	Pressure (P1) Side Identifier
MPVZ5004GW6U	1735-01	Vertical Port Attached
MPVZ5004GW7U	1560-02	Vertical Port Attached
MPVZ5004G6U/T1	482-01	Stainless Steel Cap
MPVZ5004G7U	482B-03	Stainless Steel Cap

INFORMATION FOR USING THE SMALL OUTLINE PACKAGE (CASE 482)

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface

between the board and the package. With the correct footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

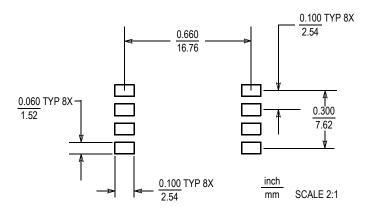
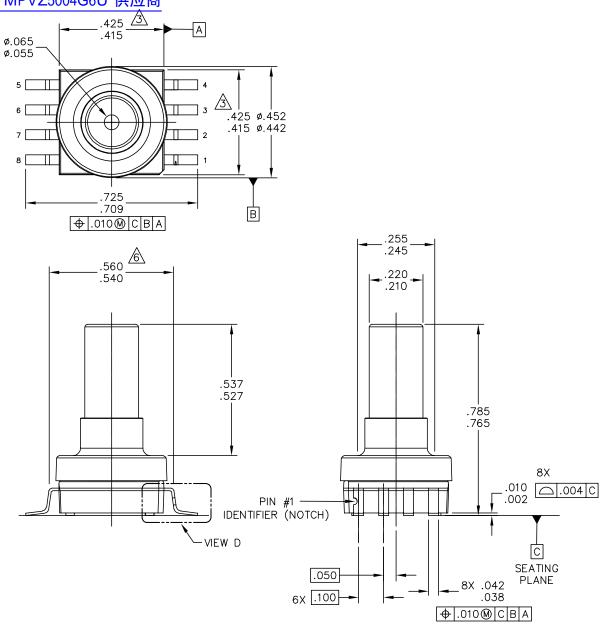


Figure 6. SOP Footprint (Case 482)

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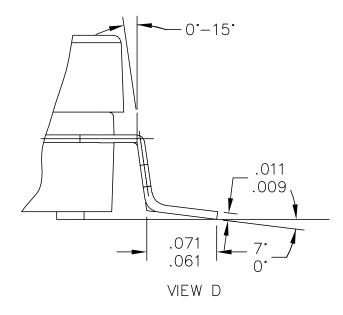


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TITLE:		DOCUMENT NO: 98ASA10686D		REV: A
SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		CASE NUMBER	R: 1735–01	16 AUG 2005
		STANDARD: NO	N-JEDEC	

PAGE 1 OF 3

CASE 1735-01 ISSUE A SMALL OUTLINE PACKAGE

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TITLE:	DOCUMENT NO): 98ASA10686D	REV: A	
SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		CASE NUMBER	2: 1735−01	18 AUG 2005
		STANDARD: NO	N-JEDEC	

PAGE 2 OF 3

CASE 1735-01 ISSUE A SMALL OUTLINE PACKAGE

查询"MPVZ5004G6U"供应商

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- 2. CONTROLLING DIMENSION: INCH.

DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.

- 4. MAXIMUM MOLD PROTRUSION IS .006.
- 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

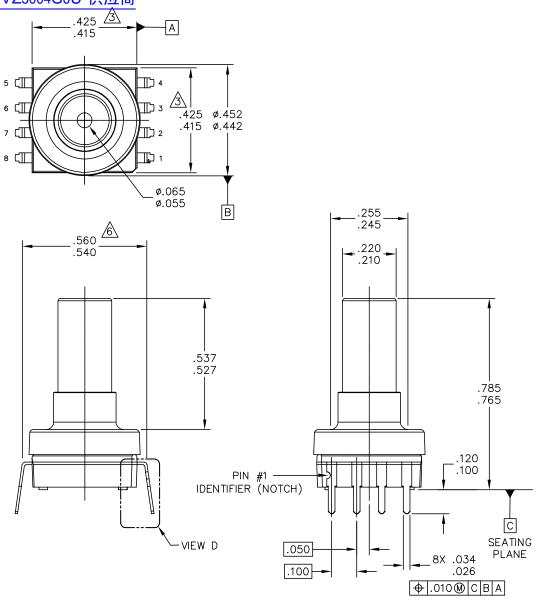
6 DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

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TITLE:		DOCUMENT NO): 98ASA10686D	REV: A
SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		CASE NUMBER	: 1735–01	18 AUG 2005
		STANDARD: NO	N-JEDEC	

PAGE 3 OF 3

CASE 1735-01 ISSUE A SMALL OUTLINE PACKAGE

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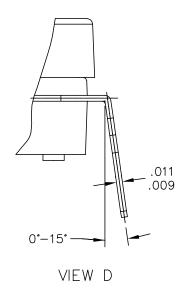


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TITLE:		DOCUMENT NO: 98ASA10611D		REV: C
SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		CASE NUMBER	2: 1560–02	26 MAY 2005
		STANDARD: NO	N-JEDEC	

PAGE 1 OF 3

CASE 1560-02 ISSUE C SMALL OUTLINE PACKAGE

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TITLE:	DOCUMENT NO): 98ASA10611D	REV: C	
SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		CASE NUMBER	2: 1560–02	26 MAY 2005
		STANDARD: NO	N-JEDEC	

PAGE 2 OF 3

CASE 1560-02 ISSUE C SMALL OUTLINE PACKAGE

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NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- 2. CONTROLLING DIMENSION: INCH.

A DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.

- 4. MAXIMUM MOLD PROTRUSION IS .006.
- 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

6 DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

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TITLE:		DOCUMENT NO: 98ASA10611D		REV: C
SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH		CASE NUMBER: 1560-02 26		26 MAY 2005
		STANDARD: NO	N-JEDEC	

PAGE 3 OF 3

CASE 1560-02 ISSUE C SMALL OUTLINE PACKAGE

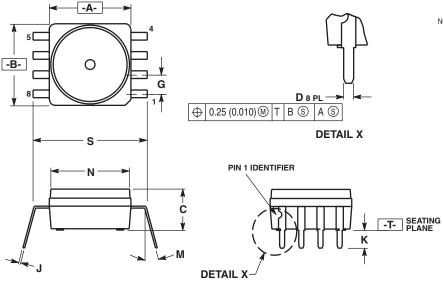
查询"MPVZ5004G6U"供应商 ⊕ 0.25 (0.010) M T B S A S -B-0 -14-3 G -1+-S -T-SEATING PLANE ∠PIN 1 IDENTIFIER

CASE 482-01 ISSUE O SMALL OUTLINE PACKAGE

NOTES:

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
C	0.212	0.230	5.38	5.84
D	0.038	0.042	0.96	1.07
G	0.100	BSC	2.54 BSC	
Н	0.002	0.010	0.05	0.25
7	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.405	0.415	10.29	10.54
S	0.709	0.725	18.01	18.41



CASE 482B-03 ISSUE B SMALL OUTLINE PACKAGE

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006).
- 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
 6. DIMENSION S TO CENTER OF LEAD WHEN
- FORMED PARALLEL
 - INCHES MILLIMETERS
 DIM
 MIN
 MAX
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 MAX

 A
 0.415
 0.425
 10.54
 10.79
 В 0.415 0.425 0.210 0.220 10.54 10.79 5.33 5.59 D 0.026 0.034 0.66 0.864 G 0.100 BSC 2.54 BSC J K M 0.009 0.011 0.23 0.28
 K
 0.100
 0.120
 2.54
 3.05

 M
 0°
 15°
 0°
 15°

 N
 0.405
 0.415
 10.29
 10.54

S 0.540 0.560 13.72 14.22

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